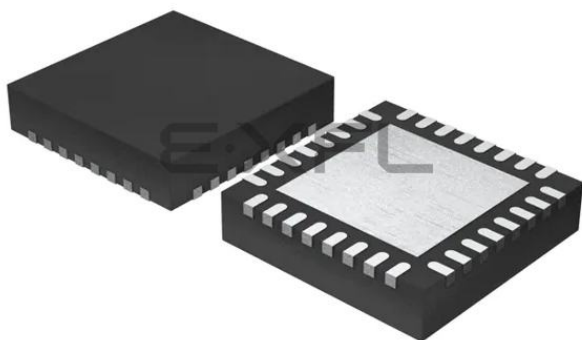




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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 3.8V
Data Converters	A/D 4x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg210f16-qfn32t

divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 μ DMA controller licensed from ARM.

2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32TG.

2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32TG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32TG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.8 Watchdog (WDOG)

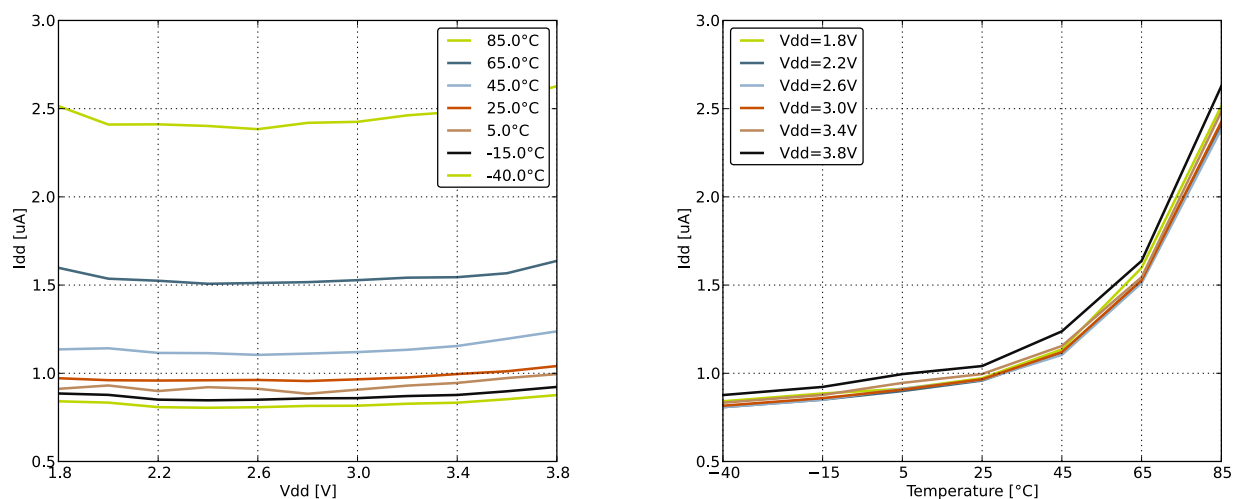
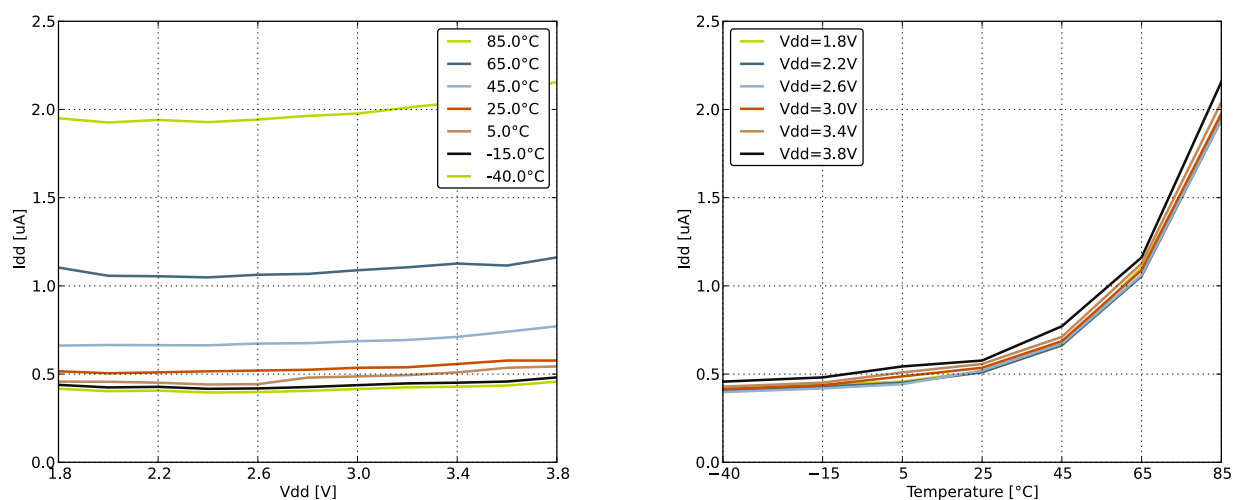
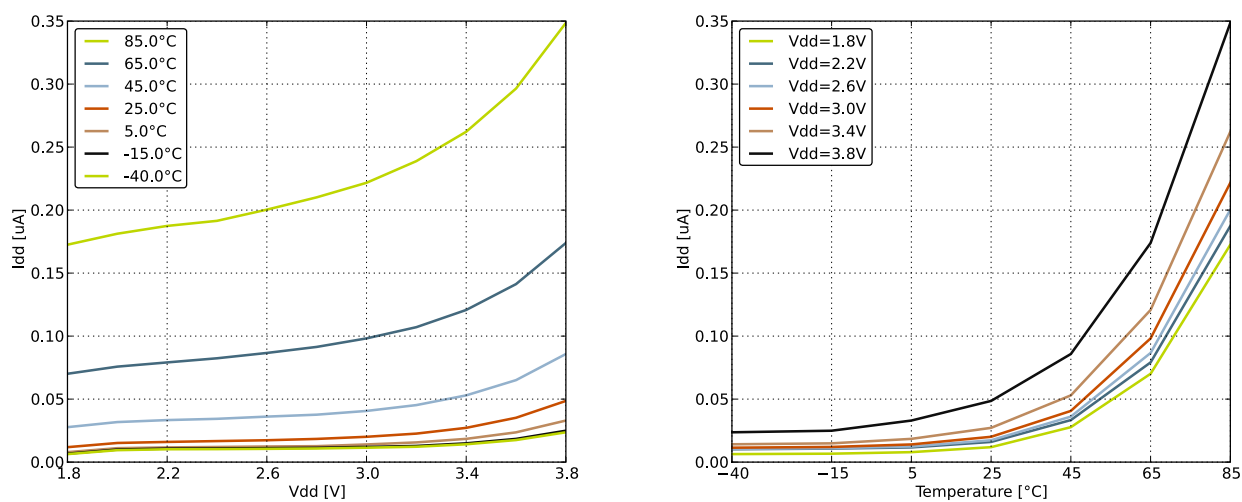
The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.10 Inter-Integrated Circuit Interface (I2C)

The I²C module provides an interface between the MCU and a serial I²C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I²C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

Figure 3.1. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.**Figure 3.2. EM3 current consumption.****Figure 3.3. EM4 current consumption.**

3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 3.4. Energy Modes Transitions

Symbol	Parameter	Min	Typ	Max	Unit
t_{EM10}	Transition time from EM1 to EM0		0		HF-CORE-CLK cycles
t_{EM20}	Transition time from EM2 to EM0		2		μs
t_{EM30}	Transition time from EM3 to EM0		2		μs
t_{EM40}	Transition time from EM4 to EM0		163		μs

3.6 Power Management

The EFM32TG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

Table 3.5. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{BODextthr-}$	BOD threshold on falling external supply voltage		1.74		1.96	V
$V_{BODextthr+}$	BOD threshold on rising external supply voltage			1.85	1.98	V
$V_{PORthr+}$	Power-on Reset (POR) threshold on rising external supply voltage				1.98	V
t_{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		μs
$C_{DECOUPLE}$	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		μF

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		$f_{\text{HFRCO}} = 14 \text{ MHz}$		104	120	μA
		$f_{\text{HFRCO}} = 11 \text{ MHz}$		94	110	μA
		$f_{\text{HFRCO}} = 6.6 \text{ MHz}$		63	90	μA
		$f_{\text{HFRCO}} = 1.2 \text{ MHz}$		22	32	μA
TUNESTEP _{H-FR} FRCO	Frequency step for LSB change in TUNING value			0.3 ³		%

¹For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

²For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

³The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

Figure 3.11. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature

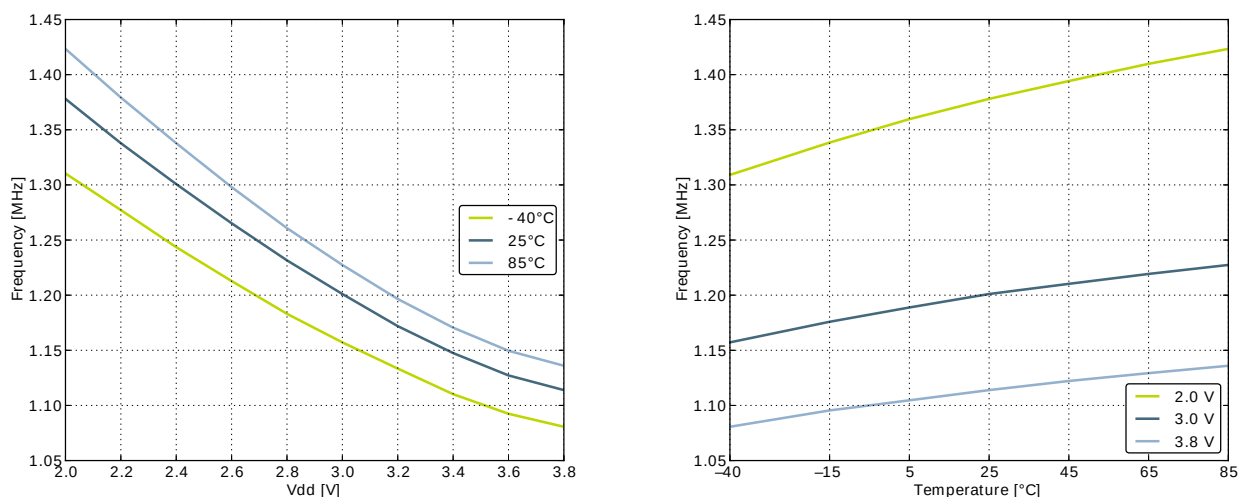
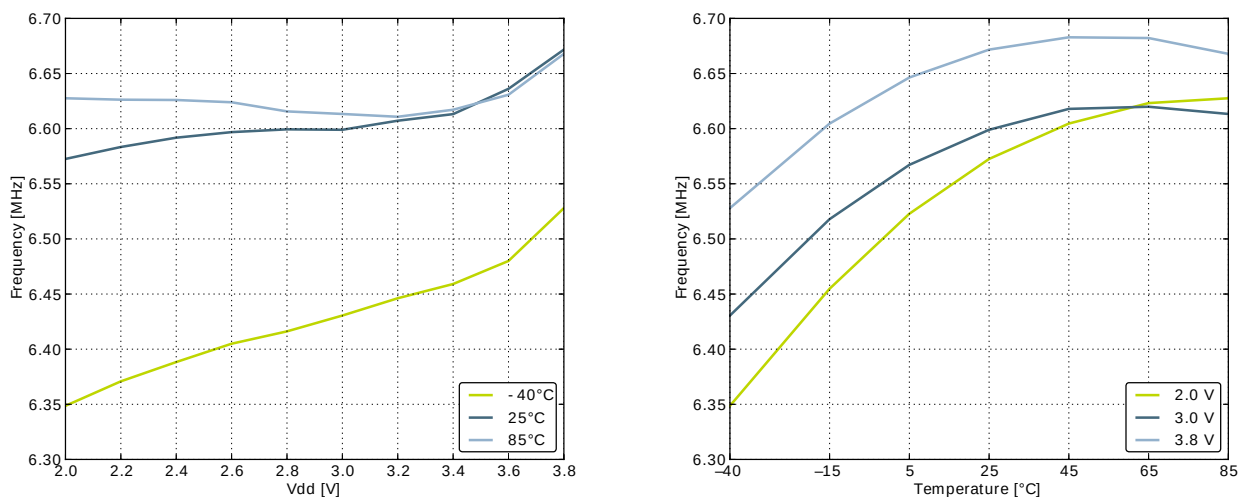


Figure 3.12. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature



3.10 Analog Digital Converter (ADC)

Table 3.14. ADC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{ADCIN}	Input voltage range	Single ended	0		V _{REF}	V
		Differential	-V _{REF} /2		V _{REF} /2	V
V _{ADCREFIN}	Input range of external reference voltage, single ended and differential		1.25		V _{DD}	V
V _{ADCREFIN_CH7}	Input range of external negative reference voltage on channel 7	See V _{ADCREFIN}	0		V _{DD} - 1.1	V
V _{ADCREFIN_CH6}	Input range of external positive reference voltage on channel 6	See V _{ADCREFIN}	0.625		V _{DD}	V
V _{ADCCMIN}	Common mode input range		0		V _{DD}	V
I _{ADCIN}	Input current	2pF sampling capacitors		<100		nA
CMRR _{ADC}	Analog input common mode rejection ratio			65		dB
I _{ADC}	Average active current	1 MSamples/s, 12 bit, external reference		377		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b00		67		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01		68		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10		71		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b11		244		μA
I _{ADCREF}	Current consumption of internal voltage reference	Internal voltage reference		65		μA
C _{ADCIN}	Input capacitance			2		pF
R _{ADCIN}	Input ON resistance		1			MΩ
R _{ADCFILT}	Input RC filter resistance			10		kΩ
C _{ADCFILT}	Input RC filter/de-coupling capacitance			250		fF

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference		69		dB
		200 kSamples/s, 12 bit, differential, $2 \times V_{DD}$ reference		70		dB
SINAD _{ADC}	Signal-to-Noise And Distortion-ratio (SINAD)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		62		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		64		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
		1 MSamples/s, 12 bit, differential, $2 \times V_{DD}$ reference		68		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		66		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	62	68		dB
		200 kSamples/s, 12 bit, differential, $2 \times V_{DD}$ reference		69		dB
SFDR _{ADC}	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc

at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

²Typical numbers given by $\text{abs}(\text{Mean}) / (85 - 25)$.

³Max number given by $(\text{abs}(\text{Mean}) + 3 \times \text{stddev}) / (85 - 25)$.

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.17 (p. 30) and Figure 3.18 (p. 30), respectively.

Figure 3.17. Integral Non-Linearity (INL)

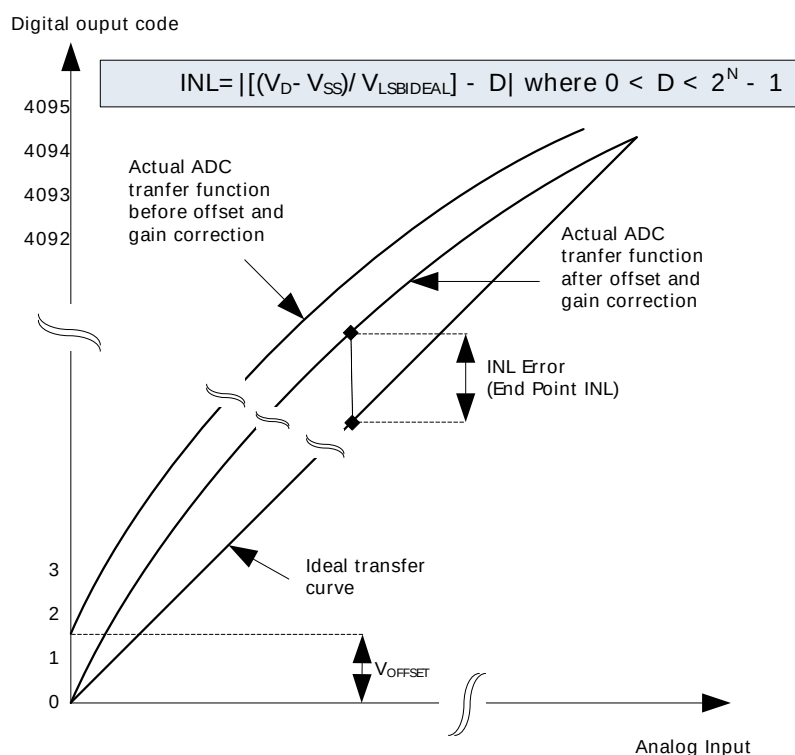
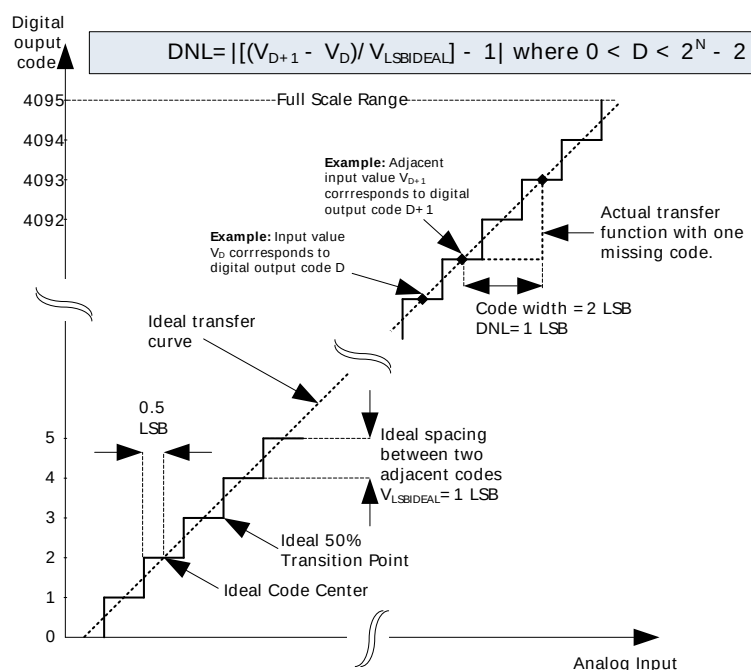
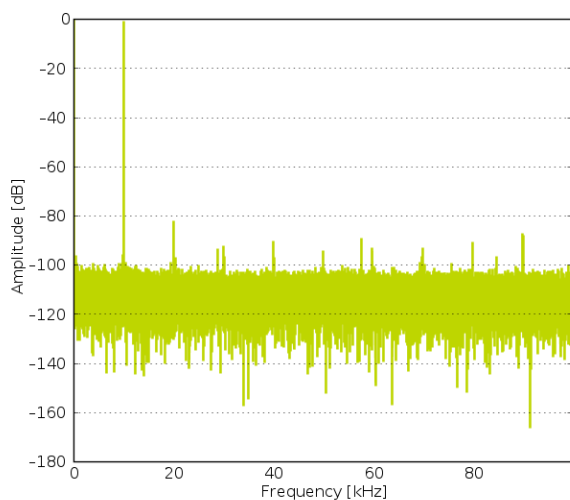


Figure 3.18. Differential Non-Linearity (DNL)

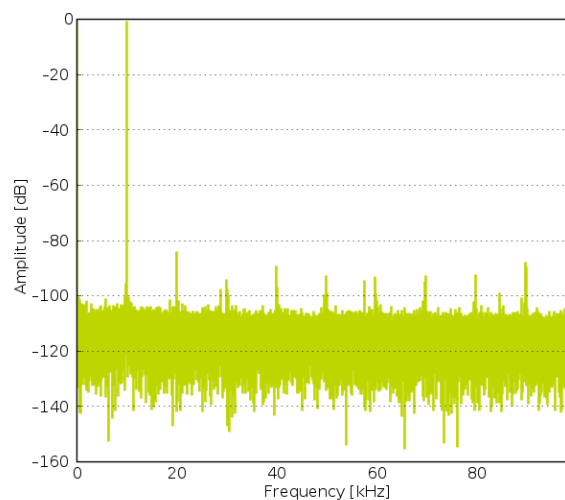


3.10.1 Typical performance

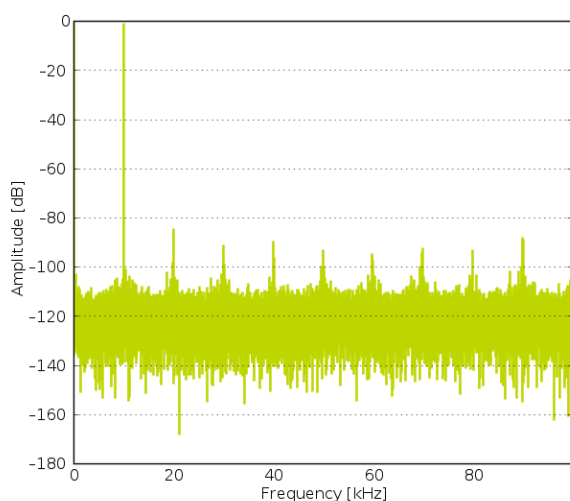
Figure 3.19. ADC Frequency Spectrum, $V_{dd} = 3V$, Temp = 25°C



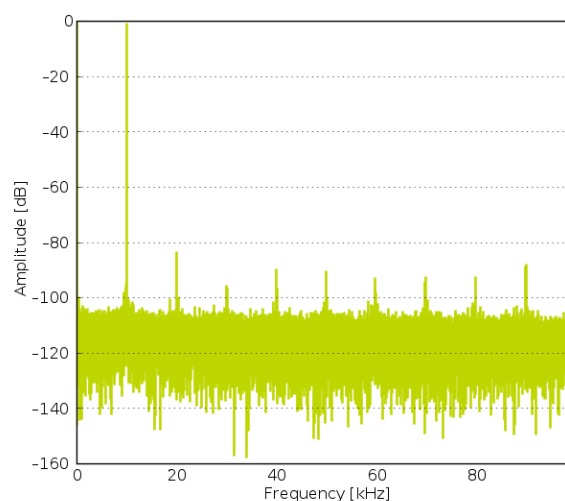
1.25V Reference



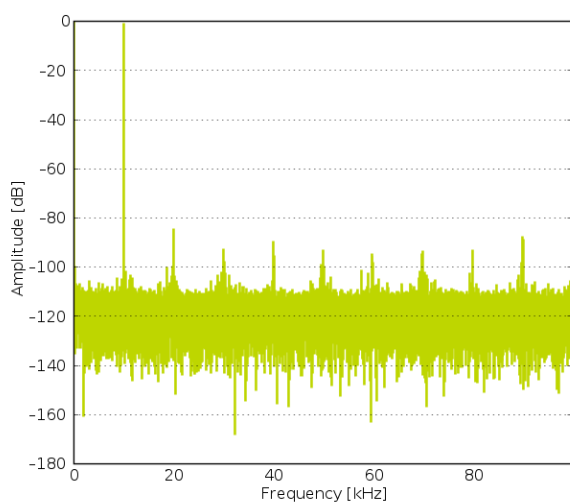
2.5V Reference



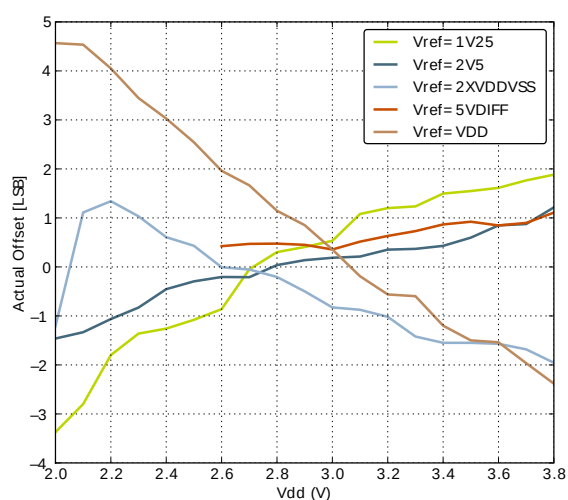
2XVDDVSS Reference



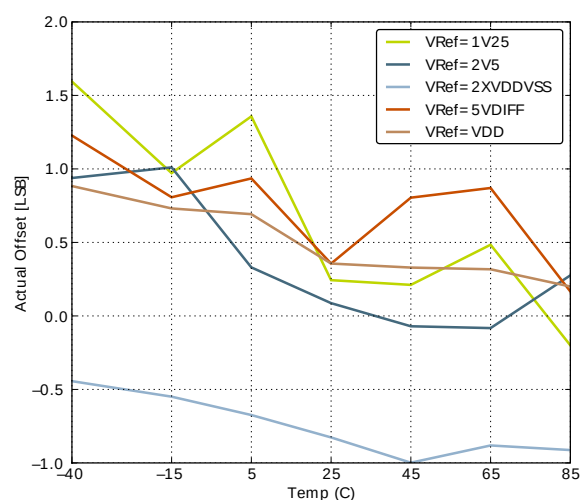
5VDIFF Reference



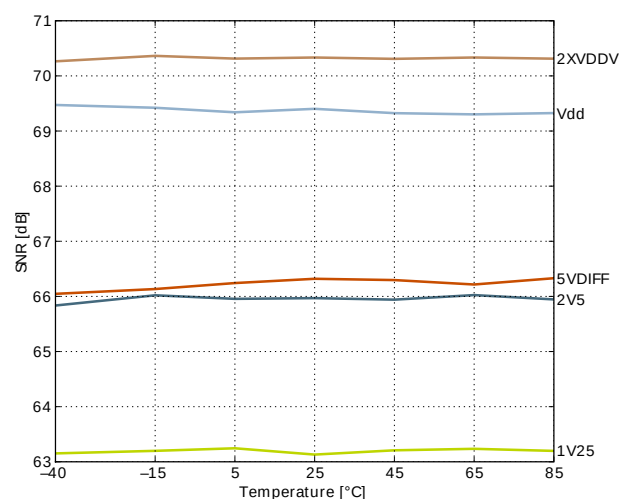
VDD Reference

Figure 3.22. ADC Absolute Offset, Common Mode = $V_{DD}/2$ 

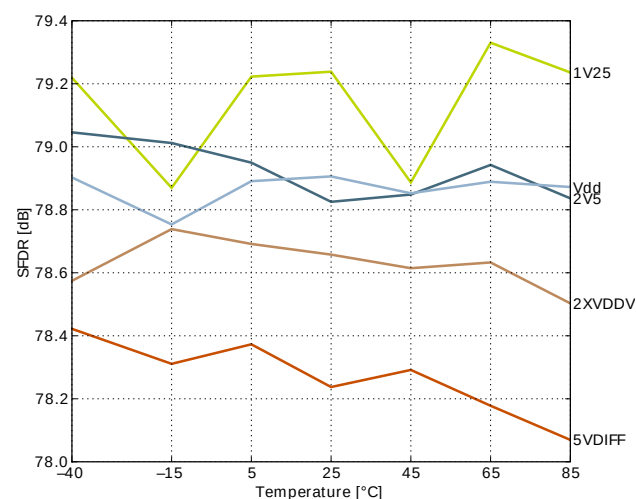
Offset vs Supply Voltage, Temp = 25°C



Offset vs Temperature, Vdd = 3V

Figure 3.23. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V

Signal to Noise Ratio (SNR)



Spurious-Free Dynamic Range (SFDR)

3.11 Digital Analog Converter (DAC)

Table 3.15. DAC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DACOUT}	Output voltage range	VDD voltage reference, single ended	0		V_{DD}	V
V_{DACCM}	Output common mode voltage range		0		V_{DD}	V
I_{DAC}	Active current including references for 2 channels	500 kSamples/s, 12bit		400	650	μA
		100 kSamples/s, 12 bit		200	250	μA
		1 kSamples/s 12 bit NORMAL		17	25	μA
SR_{DAC}	Sample rate				500	ksamples/s

Symbol	Parameter	Condition	Min	Typ	Max	Unit
GBW _{OPAMP}	Gain Bandwidth Product	OPA0/OPA1 BIASPROG=0xF, HALFBIAS=0x0		16.36		MHz
		OPA0/OPA1 BIASPROG=0x7, HALFBIAS=0x1		0.81		MHz
		OPA0/OPA1 BIASPROG=0x0, HALFBIAS=0x1		0.11		MHz
		OPA2 BIASPROG=0xF, HALFBIAS=0x0		2.11		MHz
		OPA2 BIASPROG=0x7, HALFBIAS=0x1		0.72		MHz
		OPA2 BIASPROG=0x0, HALFBIAS=0x1		0.09		MHz
PM _{OPAMP}	Phase Margin	BIASPROG=0xF, HALFBIAS=0x0, C _L =75 pF		64		°
		BIASPROG=0x7, HALFBIAS=0x1, C _L =75 pF		58		°
		BIASPROG=0x0, HALFBIAS=0x1, C _L =75 pF		58		°
R _{INPUT}	Input Resistance			100		Mohm
R _{LOAD}	Load Resistance	OPA0/OPA1	200			Ohm
		OPA2	2000			Ohm
I _{LOAD_DC}	Load Current	OPA0/OPA1			11	mA
		OPA2			1.5	mA
V _{INPUT}	Input Voltage	OPAxHCMDIS=0	V _{SS}		V _{DD}	V
		OPAxHCMDIS=1	V _{SS}		V _{DD} -1.2	V
V _{OUTPUT}	Output Voltage		V _{SS}		V _{DD}	V
V _{OFFSET}	Input Offset Voltage	Unity Gain, V _{SS} <V _{in} <V _{DD} , OPAxHCMDIS=0		6		mV
		Unity Gain, V _{SS} <V _{in} <V _{DD} -1.2, OPAxHCMDIS=1		1		mV
V _{OFFSET_DRIFT}	Input Offset Voltage Drift				0.02	mV/°C
SR _{OPAMP}	Slew Rate	OPA0/OPA1 BIASPROG=0xF, HALFBIAS=0x0		46.11		V/μs
		OPA0/OPA1 BIASPROG=0x7, HALFBIAS=0x1		1.21		V/μs
		OPA0/OPA1 BIASPROG=0x0, HALFBIAS=0x1		0.16		V/μs
		OPA2 BIASPROG=0xF, HALFBIAS=0x0		4.43		V/μs
		OPA2 BIASPROG=0x7, HALFBIAS=0x1		1.30		V/μs
		OPA2 BIASPROG=0x0, HALFBIAS=0x1		0.16		V/μs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
PU _{OPAMP}	Power-up Time	OPA0/OPA1 BIASPROG=0xF, HALFBIAS=0x0		0.09		μs
		OPA0/OPA1 BIASPROG=0x7, HALFBIAS=0x1		1.52		μs
		OPA0/OPA1 BIASPROG=0x0, HALFBIAS=0x1		12.74		μs
		OPA2 BIASPROG=0xF, HALFBIAS=0x0		0.09		μs
		OPA2 BIASPROG=0x7, HALFBIAS=0x1		0.13		μs
		OPA2 BIASPROG=0x0, HALFBIAS=0x1		0.17		μs
N _{OPAMP}	Voltage Noise	V _{out} =1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAX- HCMDIS=0		101		μV _{RMS}
		V _{out} =1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAX- HCMDIS=1		141		μV _{RMS}
		V _{out} =1V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAXHCMDIS=0		196		μV _{RMS}
		V _{out} =1V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAXHCMDIS=1		229		μV _{RMS}
		RESSEL=7, 0.1 Hz<f<10 kHz, OPAXHCMDIS=0		1230		μV _{RMS}
		RESSEL=7, 0.1 Hz<f<10 kHz, OPAXHCMDIS=1		2130		μV _{RMS}
		RESSEL=7, 0.1 Hz<f<1 MHz, OPAXHCMDIS=0		1630		μV _{RMS}
		RESSEL=7, 0.1 Hz<f<1 MHz, OPAXHCMDIS=1		2590		μV _{RMS}

Figure 3.24. OPAMP Common Mode Rejection Ratio

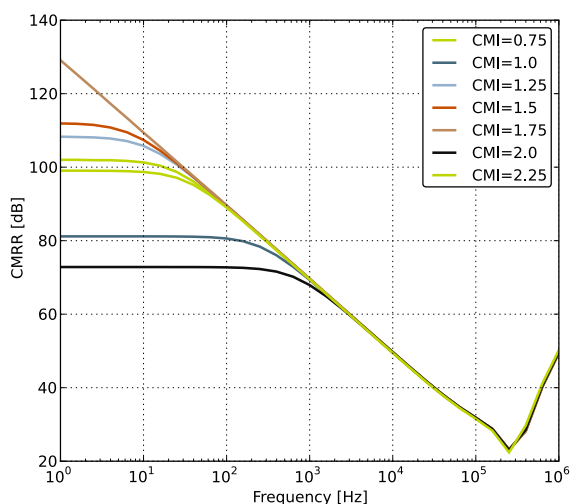
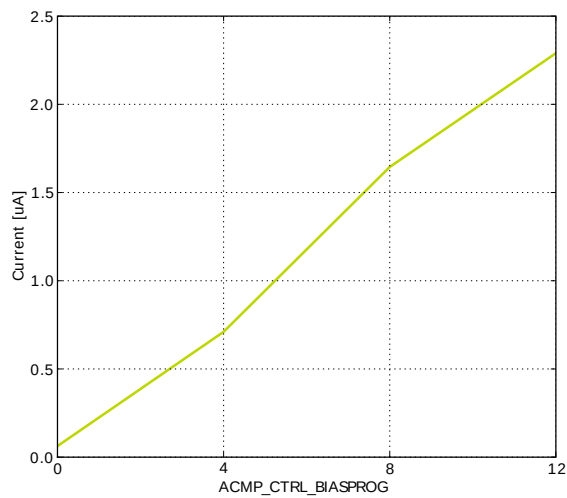
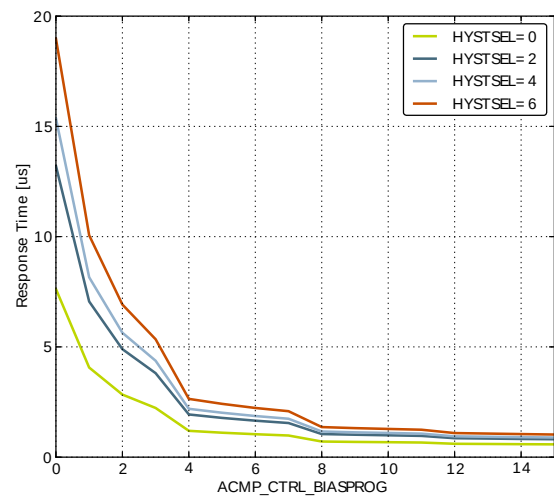


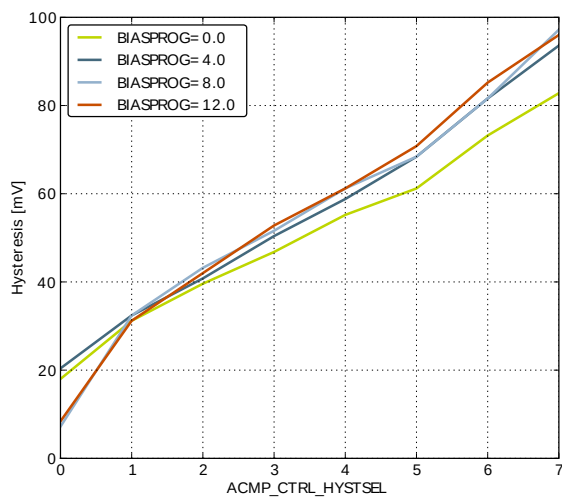
Figure 3.29. ACMP Characteristics, $V_{dd} = 3V$, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1



Current consumption, HYSTSEL = 4



Response time , $V_{cm} = 1.25V$, CP+ to CP- = 100mV



Hysteresis

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{RTC}	RTC current	RTC idle current, clock enabled		40		nA
I _{AES}	AES current	AES idle current, clock enabled		2.5		μA/ MHz
I _{GPIO}	GPIO current	GPIO idle current, clock enabled		5.31		μA/ MHz
I _{PRS}	PRS current	PRS idle current		2.81		μA/ MHz
I _{DMA}	DMA current	Clock enable		8.12		μA/ MHz

QFN32 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
28	IOVDD_5	Digital IO power supply 5.			
29	PE10		TIM1_CC0 #1	US0_TX #0	BOOT_TX
30	PE11		TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
31	PE12		TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
32	PE13			US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5

4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 47). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 4.2. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_O	PE13		PD6					Analog comparator ACMP0, digital output.
ACMP1_CH5	PC13							Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14							Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15							Analog comparator ACMP1, channel 7.
ACMP1_O	PF2		PD7					Analog comparator ACMP1, digital output.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11							Bootloader RX.
BOOT_TX	PE10							Bootloader TX.
CMU_CLK0	PA2		PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1		PE12					Clock Management Unit, clock output number 1.
DAC0_N1 / OPAMP_N1	PD7							Operational Amplifier 1 external negative input.
DAC0_OUT0 / OPAMP_OUT0	PB11							Digital to Analog Converter DAC0_OUT0 / OPAMP output channel number 0.
DAC0_OUT0ALT /	PC0	PC1						Digital to Analog Converter DAC0_OUT0ALT /

3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional

Table 4.4. QFN32 (Dimensions in mm)

Symbol	A	A1	A3	b	D	E	D2	E2	e	L	L1	aaa	bbb	ccc	ddd	eee
Min	0.80	0.00	0.203 REF	0.25	6.00 BSC	6.00 BSC	4.30	4.30	0.65 BSC	0.35	0.00	0.10	0.10	0.10	0.05	0.08
Nom	0.85	-		0.30			4.40	4.40		0.40						
Max	0.90	0.05		0.35			4.50	4.50		0.45	0.10					

The QFN32 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see:
<http://www.silabs.com/support/quality/pages/default.aspx>

5 PCB Layout and Soldering

5.1 Recommended PCB Layout

Figure 5.1. QFN32 PCB Land Pattern

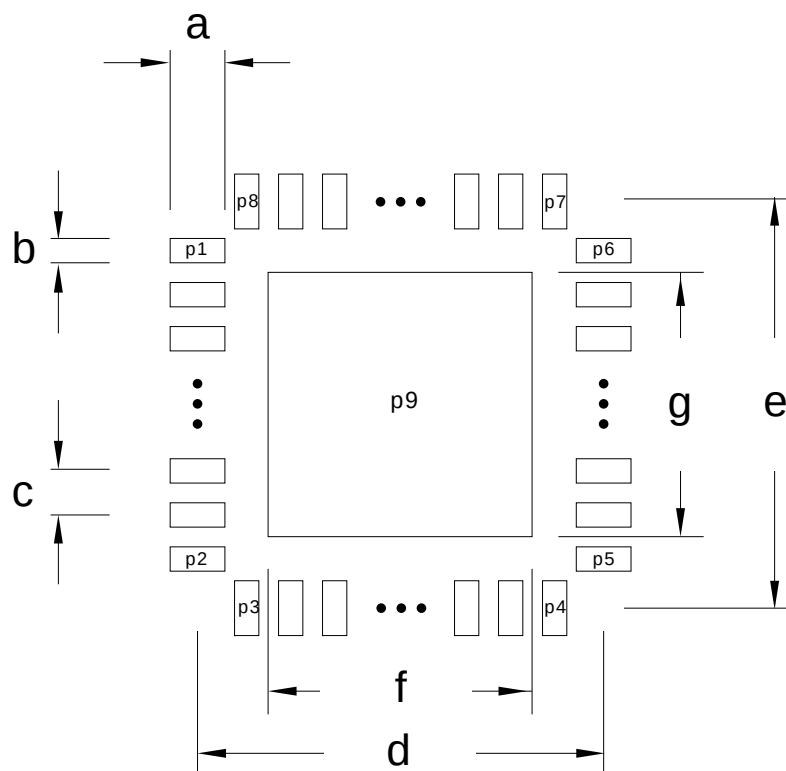
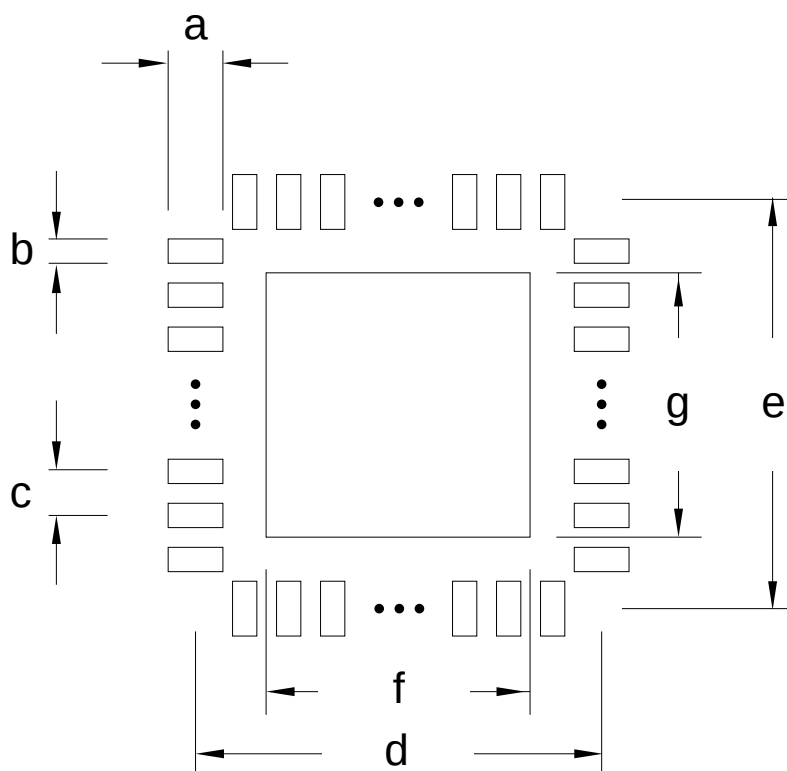
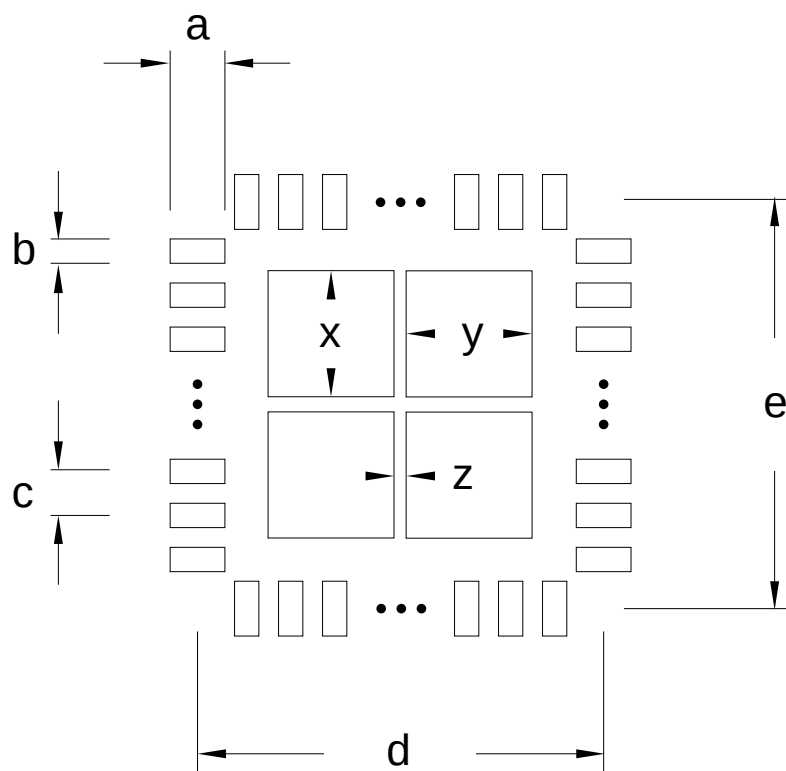


Table 5.1. QFN32 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin number	Symbol	Pin number
a	0.80	P1	1	P6	24
b	0.35	P2	8	P7	25
c	0.65	P3	26	P8	32
d	6.00	P4	16	P9	33
e	6.00	P5	17	-	-
f	4.40	-	-	-	-
g	4.40	-	-	-	-

Figure 5.2. QFN32 PCB Solder Mask**Table 5.2. QFN32 PCB Solder Mask Dimensions (Dimensions in mm)**

Symbol	Dim. (mm)
a	0.92
b	0.47
c	0.65
d	6.00
e	6.00
f	4.52
g	4.52

Figure 5.3. QFN32 PCB Stencil Design**Table 5.3. QFN32 PCB Stencil Design Dimensions (Dimensions in mm)**

Symbol	Dim. (mm)
a	0.70
b	0.25
c	0.65
d	6.00
e	6.00
x	1.30
y	1.30
z	0.50

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.3 (p. 50) .

5.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

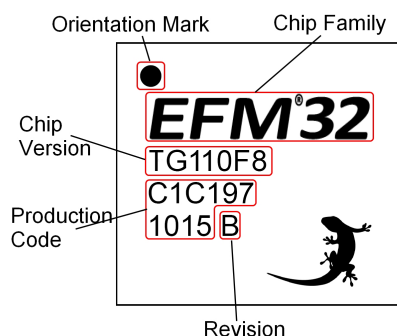
The packages have a Moisture Sensitivity Level rating of 3, please see the latest IPC/JEDEC J-STD-033 standard for MSL description and level 3 bake conditions. Place as many and as small as possible vias underneath each of the solder patches under the ground pad.

6 Chip Marking, Revision and Errata

6.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 6.1. Example Chip Marking (top view)



6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 55) .

6.3 Errata

Please see the errata document for EFM32TG210 for description and resolution of device erratas. This document is available in Simplicity Studio and online at:

<http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit>

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