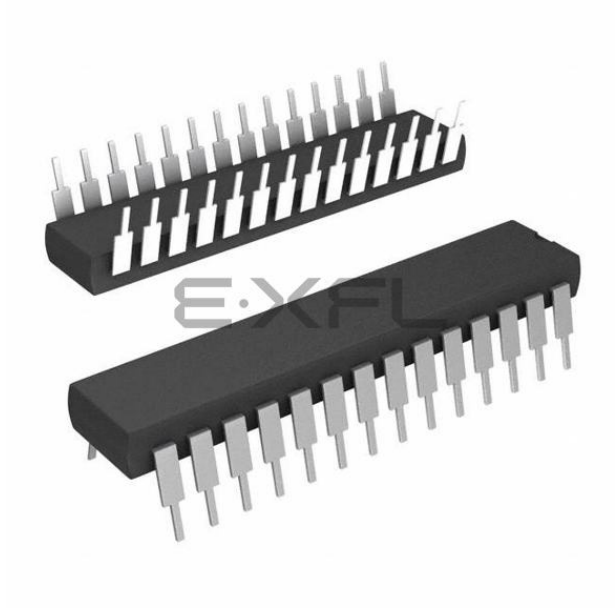

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f2410-i-sp

PIC18F2X1X/4X1X Data Sheet Errata

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39636**A**), the following clarifications and corrections should be noted. Any silicon issues related to the PIC18F2X1X/4X1X devices will be reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

1. Module: I/O Ports

The TRIS setting for the TX pin on PORTC in Table 9-5 of the Device Data Sheet was incorrectly stated as '1'.

The correct TRIS setting for the TX pin on PORTC is '0'.

2. Module: Resets

The PR2 initialization condition shown in Table 4-4 for $\overline{\text{MCLR}}$ Resets, WDT Reset, RESET Instruction, Stack Resets and Wake-up via WDT or Interrupt should read "uuuu uuuu" as shown in the following table (changes are shown in **bold** text):

TABLE 4-4: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Applicable Devices								Power-on Reset, Brown-out Reset	$\overline{\text{MCLR}}$ Resets, WDT Reset, RESET Instruction, Stack Resets	Wake-up via WDT or Interrupt
PR2	2410	2510	2515	2610	4410	4510	4515	4610	1111 1111	**uuuu uuuu**	**uuuu uuuu**

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

3. Module: DC Characteristics

In **Section 25.3 "DC Characteristics"** (page 326), the specifications for VIL parameters D033B and D034 have been clarified and now read as follows:

25.3 DC Characteristics: PIC18F2X1X/4X1X (Industrial, Extended) PIC18LF2X1X/4X1X (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial			
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**				
D033B		OSC1	VSS	0.3	V	XT, LP modes
D034		T13CKI	VSS	0.3	V	

4. Module: A/D Converter Characteristics

In Table 25-24: A/D Converter Characteristics (page 349), specification A40 has been added:

TABLE 25-24: A/D CONVERTER CHARACTERISTICS: PIC18F2X1X/4X1X (INDUSTRIAL, EXTENDED) PIC18LF2X1X/4X1X (INDUSTRIAL)

Param No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
A40	IAD	A/D Current from VDD	PIC18FXXXX	—	180	—	μA	Average current during conversion
			PIC18LFXXXX	—	90	—	μA	

5. Module: Instruction Set

In Table 23-2: PIC18FXXXX Instruction Set (page 261), the BTG instruction has been modified. The changes are shown in **bold** text:

TABLE 23-2: PIC18FXXXX INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	16-Bit Instruction Word		Status Affected	Notes
				MSb	LSb		
BIT-ORIENTED OPERATIONS							
BTG	f, **b**, a	Bit Toggle f	1	0111 bbba	ffff ffff	None	1, 2

Note 1: When a Port register is modified as a function of itself (e.g., MOVF PORTB, 1, 0), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and where applicable, 'd' = 1), the prescaler will be cleared if assigned.

6. Module: Timing Diagrams and Specifications

Table 25-6: External Clock Timing Requirements (page 333), has been revised (changes and additions are shown in **bold** text).

TABLE 25-6: EXTERNAL CLOCK TIMING REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
1A	FOSC	External CLKI Frequency(1)	DC	1	MHz	XT, RC Oscillator mode
			DC	**25**	**MHz**	**HS Oscillator mode**
			DC	31.25	kHz	LP Oscillator mode
			DC	**40**	**MHz**	**EC Oscillator mode**
		Oscillator Frequency(1)	DC	4	MHz	RC Oscillator mode
			0.1	4	MHz	XT Oscillator mode
			4	**25**	**MHz**	**HS Oscillator mode**
			4	**10**	**MHz**	**HS + PLL Oscillator mode**
			5	200	kHz	LP Oscillator mode
1	TOSC	External CLKI Period(1)	1000	—	ns	XT, RC Oscillator mode
			40	**—**	**ns**	**HS Oscillator mode**
			32	—	µs	LP Oscillator mode
			25	**—**	**ns**	**EC Oscillator mode**
		Oscillator Period(1)	250	—	ns	RC Oscillator mode
			250	1	µs	XT Oscillator mode
			40	**250**	**ns**	**HS Oscillator mode**
			100	**250**	**ns**	**HS + PLL Oscillator mode**
			5	**200**	µs	LP Oscillator mode

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period for all configurations except PLL. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.

7. Module: EUSART

The RX pin sampling information in **Section 17.1.2 "Sampling"** has changed. This section now reads as follows:

17.1.2 SAMPLING

The data on the RX pin is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RX pin when SYNC is clear or when BRG16 and BRGH are both not set.

The data on the RX pin is sampled once when SYNC is set or when BRGH16 and BRGH are both set.

8. Module: MSSP

In **Section 16.3.2 "Operation"**, the following note has been added:

Note:	The SSPBUF register cannot be used with read-modify-write instructions, such as `BCF, BTFSC, COMF`, etc.

9. Module: QFN

In the QFN pin diagrams on pages 3 and 4, and in Table 1-3: PIC18F2410/2510/2515/2610 Pinout I/O Descriptions, the following note has been added:

Note: It is recommended to connect the bottom pad of QFN package parts to VSS.

10. Module: Electrical Characteristics

Parameters D031A and D041A have been added to **Section 25-3 "DC Characteristics"**, as shown below:

25.3 DC Characteristics: PIC18F2X1X/4X1X (Industrial) PIC18LF2X1X/4X1X (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial			
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**				
		I/O ports:				
D031A		with SMBus buffer	VSS	0.8	V	
	VIH	**Input High Voltage**				
		I/O ports:				
D041A		with SMBus buffer	2.1	VDD	V	

11. Module: Electrical Characteristics

In Table 25-1: Memory Programming Requirements, parameters D132, D132A, D133 and D133A have been changed. The changes are shown in **bold** in the following table:

TABLE 25-7: MEMORY PROGRAMMING REQUIREMENTS

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Program Flash Memory					
D132	VIE	VDD for Block Erase	**3.0**	—	5.5	V	Using ICSP™ port, **25°C**
D132A	VIW	VDD for Externally Timed Erase or Write	4.5	—	5.5	V	Using ICSP port, **25°C**
D133	TIE	ICSP Block Erase Cycle Time	—	4	—	ms	**VDD ≥ 4.5V**
D133A	TIW	ICSP Erase or Write Cycle Time (externally timed)	1	—	—	ms	**VDD ≥ 4.5V, 25°C**
D133A	**TIW**	**Self-Timed Write Cycle Time**	**—**	**2**	**—**	**ms**	

REVISION HISTORY

Rev A Document (01/2005)
First revision of this document.

Data Sheet Clarification issues 1 (I/O Ports), 2 (Resets), 3 (DC Characteristics), 4 (A/D Converter Characteristics), 5 (Instruction Set) and 6 (Timing Diagrams and Specifications).

Rev B Document (09/2005)
Added Data Sheet Clarification issues 7 (EUSART), 8 (MSSP), 9 (QFN) and 10-11 (Electrical Characteristics).

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