Renesas Electronics America Inc - R8A77240D500BG#U0 Datasheet

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Understanding Embedded - Microprocessors

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	SH-4A
Number of Cores/Bus Width	-
Speed	500MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	449-FBGA
Supplier Device Package	449-FBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r8a77240d500bg-u0

No.	Location	Pin Name	Function (Multiplexed Functions Where Applicable)	I/O	I/O Buffer Type	I/O Buffer Power Supply	Handling when unused
432	AE8	MDQ7	MDQ7	IO		VCCQ_DDR	open
433	AE9	MA13	MA13	O		VCCQ_DDR	open
434	AE10	MA10	MA10	O		VCCQ_DDR	open
435	AE11	MBA0	MBA0	O		VCCQ_DDR	open
436	AE12	$\overline{\text{MWE}}$	$\overline{\text{MWE}}$	O		VCCQ_DDR	open
437	AE13	MODT	MODT	O		VCCQ_DDR	open
438	AE14	MA2	MA2	O		VCCQ_DDR	open
439	AE15	MA11	MA11	O		VCCQ_DDR	open
440	AE16	MDQ28	MDQ28	IO		VCCQ_DDR	open
441	AE17	MDQ30	MDQ30	IO		VCCQ_DDR	open
442	AE18	MDQM3	MDQM3	O		VCCQ_DDR	open
443	AE19	$\overline{\text{MDQS3}}$	$\overline{\text{MDQS3}}$	IO		VCCQ_DDR	open
444	AE20	MDQ31	MDQ31	IO		VCCQ_DDR	open
445	AE21	MDQ29	MDQ29	IO		VCCQ_DDR	open
446	AE22	VCCQ_DDR	VCCQ_DDR	—	—	—	—
447	AE23	D2	PTQ2 / D2	IO / IO	pull-down	VCCQ1	open
448	AE24	D4	PTQ4 / D4	IO / IO	pull-down	VCCQ1	open
449	AE25	VSS	VSS	—	—	—	—

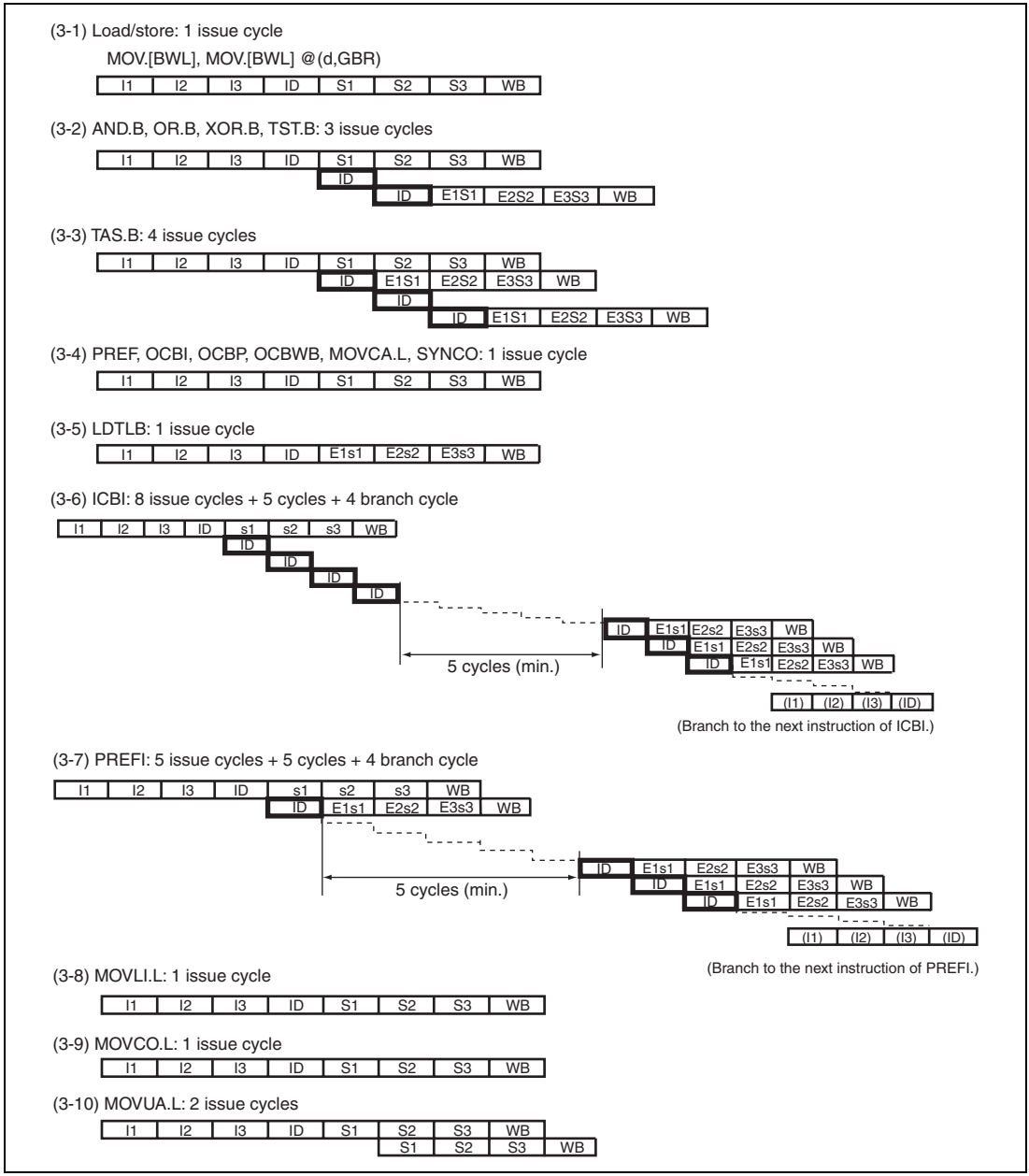


Figure 4.2 Instruction Execution Patterns (3)

8.3 Operand Cache Operation

8.3.1 Read Operation

When the Operand Cache (OC) is enabled (OCE = 1 in CCR) and data is read from a cacheable area, the cache operates as follows:

1. The tag, V bit, U bit, and LRU bits on each way are read from the cache line indexed by virtual address bits [12:5].
2. The tags read from the each way is compared with bits [28:10] of the physical address resulting from virtual address translation by the MMU:

- If there is a way whose tag matches and its V bit is 1, see No. 3.
- If there is no way whose tag matches and its V bit is 1 and the U bit of the way which is selected to replace using the LRU bits is 0, see No. 4.
- If there is no way whose tag matches and its V bit is 1 and the U bit of the way which is selected to replace using the LRU bits is 1, see No. 5.

3. Cache hit

   The data indexed by virtual address bits [4:0] is read from the data field of the cache line on the hitted way in accordance with the access size. Then the LRU bits are updated to indicate the hitted way is the latest one.

4. Cache miss (no write-back)

   Data is read into the cache line on the way, which is selected to replace, from the physical address space corresponding to the virtual address. Data reading is performed, using the wraparound method, in order from the quad-word data(8 bytes) including the cache-missed data. When the corresponding data arrives in the cache, the read data is returned to the CPU. While the remaining data on the cache line is being read, the CPU can execute the next processing. When reading of one line of data is completed, the tag corresponding to the physical address is recorded in the cache, 1 is written to the V bit and 0 is written to the U bit on the way. Then the LRU bit is updated to indicate the way is latest one.

5. Cache miss (with write-back)

   The tag and data field of the cache line on the way which is selected to replace are saved in the write-back buffer. Then data is read into the cache line on the way which is selected to replace from the physical address space corresponding to the virtual address. Data reading is performed, using the wraparound method, in order from the quad-word data (8 bytes) including the cache-missed data, and when the corresponding data arrives in the cache, the read data is returned to the CPU. While the remaining one cache line of data is being read, the CPU can execute the next processing. When reading of one line of data is completed, the tag corresponding to the physical address is recorded in the cache, 1 is written to the V bit, and 0 to the U bit. And the LRU bits are updated to indicate the way is latest one. The data in the write-back buffer is then written back to external memory.

Bit	Bit Name	Initial Value	R/W	Description
7 to 2	BKADB[5:0]	All 0	R/W	Address Location of Upper Bank Address (Valid when BKADM = B'01.) These bits specify the address location of the upper bank address. These bits are valid when the BKADM bit is set so that the bank addresses should be treated as non-contiguous addresses. The BA1 address location is set as the upper bank address. For 8-bank products, BA2 is treated as the upper address of BA1.When BKADP = B'000000, these bits are used as the upper address of BA0 and cannot be set. 000000: No setting 001101: Set address 13 to BA1 (Set address 14 to BA2) 001110: Set address 14 to BA1 (Set address 15 to BA2) 001111: Set address 15 to BA1 (Set address 16 to BA2) 010000: Set address 16 to BA1 (Set address 17 to BA2) Others: Setting prohibited
1, 0	BWIDTH[1:0]	00	R/W	SDRAM Bus Width Setting These bits set the external data bus width. 00: Setting prohibited 01: 16 bits 10: 32 bits 11: Setting prohibited

Note: 1. Supported memory configuration

(1) DDR2-SDRAM

- 16-bit bus configuration in which one 16-bit width SDRAM is connected, or two 8-bit SDRAMs are connected in parallel.
- 32-bit bus configuration in which one 32-bit width SDRAM is connected, or two 16-bit SDRAMs connected in parallel.

(2) Mobile-DDR-SDRAM

- 16-bit bus configuration in which one 16-bit width SDRAM is connected.
- 32-bit bus configuration in which one 32-bit width SDRAM is connected, or two 16-bit SDRAMs connected in parallel.

Bit	Bit Name	Initial Value	R/W	Description
1	RBSYTO	0	R/W*	Response Busy Timeout [Setting conditions] Response busy does not end [Clearing condition] Writing a 0 to this bit Note: The period for timeout detection is set in SRBSYTO[3:0] of CE_CLK_CTRL. The command sequence is not stopped even if RBSYTO is set.
0	RSPTO	0	R/W*	Response Timeout [Setting conditions] Response could not be received [Clearing condition] Writing a 0 to this bit Note: The period for timeout detection is set in SRSPTO[1:0] of CE_CLK_CTRL. The command sequence is not stopped even if RSPTO is set.

Note: * A 0 is the only value that can be written to these bits. Writing a 1 is ignored.

Register Name	Abbreviation	R/W	Address	Access Size
MSIOF1 FIFO control register	MSIOF1_SIFCTR	R/W	H'A4C50030	32
MSIOF1 Status register	MSIOF1_SISTR	R/W	H'A4C50040	32
MSIOF1 Interrupt enable register	MSIOF1_SIIER	R/W	H'A4C50044	32
MSIOF1 Transmit control data register 1	MSIOF1_SITDR1	W	H'A4C50048	32
MSIOF1 Transmit control data register 2	MSIOF1_SITDR2	W	H'A4C5004C	32
MSIOF1 Transmit FIFO data register	MSIOF1_SITFDR	W	H'A4C50050	32
MSIOF1 Receive control data register 1	MSIOF1_SIRDR1	R	H'A4C50058	32
MSIOF1 Receive control data register 2	MSIOF1_SIRDR2	R	H'A4C5005C	32
MSIOF1 Receive FIFO data register	MSIOF1_SIRFDR	R	H'A4C50060	32

Table 25.3 Register States in Each Operating Mode

Register Abbreviation	Power-On Reset	Manual Reset	Software Standby	Module Standby	R/U-Standby	Sleep
MSIOF0_SITMDR1	Initialized	Initialized	Retained	Retained	Initialized	Retained
MSIOF0_SITMDR2	Initialized	Initialized	Retained	Retained	Initialized	Retained
MSIOF0_SITMDR3	Initialized	Initialized	Retained	Retained	Initialized	Retained
MSIOF0_SIRMDR1	Initialized	Initialized	Retained	Retained	Initialized	Retained
MSIOF0_SIRMDR2	Initialized	Initialized	Retained	Retained	Initialized	Retained
MSIOF0_SIRMDR3	Initialized	Initialized	Retained	Retained	Initialized	Retained
MSIOF0_SITSCR	Initialized	Initialized	Retained	Retained	Initialized	Retained
MSIOF0_SIRSCR	Initialized	Initialized	Retained	Retained	Initialized	Retained
MSIOF0_SICTR	Initialized	Initialized	Retained	Retained	Initialized	Retained
MSIOF0_SIFCTR	Initialized	Initialized	Retained	Retained	Initialized	Retained
MSIOF0_SISTR	Initialized	Initialized	Retained	Retained	Initialized	Retained
MSIOF0_SIIER	Initialized	Initialized	Retained	Retained	Initialized	Retained
MSIOF0_SITDR1	Initialized	Initialized	Retained	Retained	Initialized	Retained
MSIOF0_SITDR2	Initialized	Initialized	Retained	Retained	Initialized	Retained
MSIOF0_SITFDR	Initialized	Initialized	Retained	Retained	Initialized	Retained
MSIOF0_SIRDR1	Initialized	Initialized	Retained	Retained	Initialized	Retained
MSIOF0_SIRDR2	Initialized	Initialized	Retained	Retained	Initialized	Retained
MSIOF0_SIRFDR	Undefined	Undefined	Retained	Retained	Initialized	Retained

Bit	Bit Name	Initial Value	R/W	Description
1, 0	CKE[1:0]	00	R/W	Clock Enable Select the SCIF clock source and enable or disable clock output from the SCK pin. Depending on CKE[1:0], the SCK pin can be used for serial clock output or serial clock input. CKE[1:0] must be set before selecting the operating mode of the SCIF by the SCSMR register. • Asynchronous mode 00: Internal clock; SCK pin is used as an input pin (input signal is ignored) 01: Setting prohibited 10: External clock; SCK pin used for clock input*[1] 11: Setting prohibited • Clock synchronous mode 00: Setting prohibited 01: Internal clock; SCK pin used for serial clock output*[2] 10: External clock; SCK pin used for serial clock input 11: Setting prohibited Notes: 1. The input clock frequency is 16 times the bit rate. 2. The output clock frequency is the same as the bit rate.

26.3.7 Serial Status Register (SCFSR)

SCFSR is a 16-bit register. The upper 8 bits indicate the number of receive errors in the receive FIFO data register (SCFRDR), and the lower 8 bits indicate the states of SCIF operation.

The CPU can always read the upper 8 bits of SCFSR and always read and write from/to the lower 8 bits. However, it cannot write 1 to the flags ER, TEND, TDFE, BRK, RDF, and DR. These flags can be cleared to 0 only after 1 has been read from them. The PER flag and FER flag are read-only and cannot be written to.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PERC[3:0]				FERC[3:0]				ER	TEND	TDFE	BRK	FER	PER	RDF	DR
Initial value:	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W*	R/W*	R/W*	R/W*	R	R	R/W*	R/W*

Note: * Only 0 can be written to clear the flag.

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	PERC[3:0]	0000	R	Number of Parity Errors Indicate the number of data bytes including a parity error in the received data stored in the receive FIFO data register (SCFRDR). After the ER bit in SCFSR is set, the value in PERC[3:0] indicates the number of parity errors in SCFRDR. When parity errors have been found in all bytes in the 16 bytes of received data in SCFRDR, PERC[3:0] shows 0000.
11 to 8	FERC[3:0]	0000	R	Number of Framing Errors Indicate the number of data bytes including a framing error in the received data stored in SCFRDR. After the ER bit in SCFSR is set, the value in FERC[3:0] indicates the number of framing errors in SCFRDR. When framing errors have been found in all bytes in the 16 bytes of received data in SCFRDR, FERC[3:0] shows 0000.

28.4.3 Reading Time

Figure 28.3 shows how to read the time.

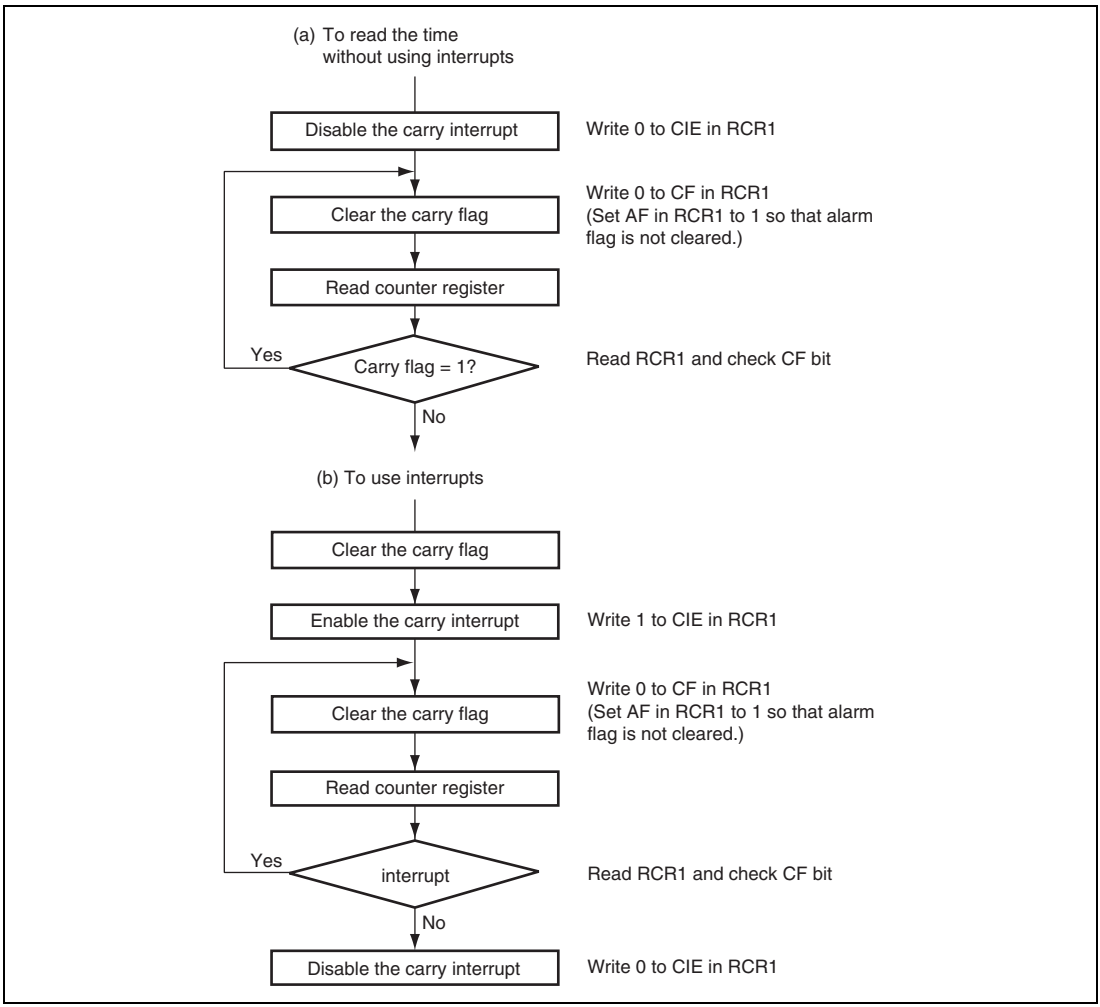


Figure 28.3 Reading Time

If a carry occurs while reading the time, the correct time will not be obtained, so it must be read again. Part (a) in Figure 28.3 shows the method of reading the time without using interrupts; part (b) in Figure 28.3 shows the method using carry interrupts. To keep programming simple, method (a) should normally be used.

31.4.9 Interrupts Enable Register 0 (INTENB0)

INTENB0 is a register that specifies the various interrupt masks. On detecting the interrupt corresponding to the bit in this register to which software has set 1, this module generates the USB interrupt.

This module sets 1 to each status bit in INTSTS0 when a detection condition of the corresponding interrupt source has been satisfied regardless of the set value in INTENB0 (regardless of whether the interrupt output is enabled or disabled).

While the status bit in INTSTS0 corresponding to the interrupt source indicates 1, this module generates the USB interrupt when software modifies the corresponding interrupt enable bit in INTENB0 from 0 to 1.

This register is initialized by a power-on reset.

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	NRDYE	BRDYE	—	—	—	—	—	—	—	—
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	VBSE	0	R/W	VBUS Interrupts Enable Enables or disables the USB interrupt output when the VBINT interrupt is detected. 0: Interrupt output disabled 1: Interrupt output enabled
14	RSME	0	R/W	Resume Interrupts Enable Enables or disables the USB interrupt output when the RESM interrupt is detected. 0: Interrupt output disabled 1: Interrupt output enabled
13	SOFE	0	R/W	Frame Number Update Interrupts Enable Enables or disables the USB interrupt output when the SOFR interrupt is detected. 0: Interrupt output disabled 1: Interrupt output enabled

31.4.32 Pipe Buffer Setting Register (PIPEBUF)

PIPEBUF is a register that specifies the buffer size and buffer number for PIPE1 to PIPE9.

This register is initialized by a power-on reset.

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	BUFSIZE[4:0]					—	—	BUFNMB[7:0]							
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

31.4.34 Pipe Timing Control Register (PIPEPERI)

PIPEPERI is a register that selects whether the buffer is flushed or not when an interval error occurred during isochronous IN transfer, and sets the interval error detection interval for PIPE1 to PIPE9.

This register is initialized by a power-on reset.

Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	IFIS	—	—	—	—	—	—	—	—	—	IITV[2:0]		
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W :	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	IFIS	0	R/W	Isochronous IN Buffer Flush Specifies whether to flush the buffer when the pipe selected by the PIPESEL bits (selected pipe) is used for isochronous IN transfers. 0: The buffer is not flushed. 1: The buffer is flushed. When the function controller function is selected and the selected pipe is for isochronous IN transfers, this module automatically clears the FIFO buffer when this module fails to receive the IN token from the USB host within the interval set by the IITV bits in terms of (μ) frames. In double buffer mode (DBLB = 1), this module only clears the data in the plane used earlier. This module clears the FIFO buffer on receiving the SOF packet immediately after the (μ) frame in which this module has expected to receive the IN token. Even if the SOF packet is corrupted, this module also clears the FIFO buffer at the right timing to receive the SOF packet by using the internal interpolation. When the host controller function is selected, set this bit to 0. When the selected pipe is not for the isochronous transfer, set this bit to 0.

(4) Input JPEG Coded Data

Markers to be processed in decoding are SOS, SOF0, SOS, DQT, DHT, DRI, RSTm, and EOI. Other markers except for the error markers shown below are ignored even if they are read.

(5) JPEG Decoding Errors

(a) Error Marker

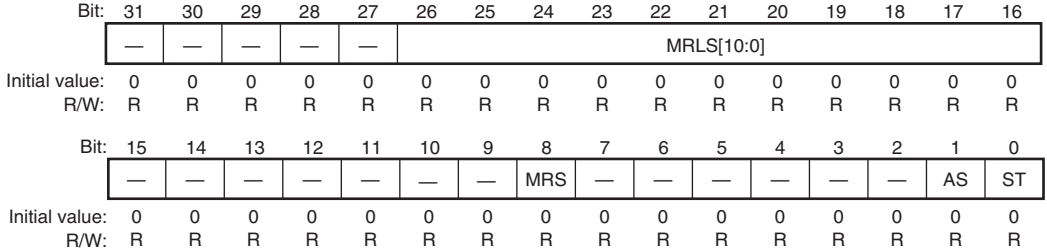
If an error marker is found while analyzing encoded data for decoding, identify the error type by the code and set the code (shown in Table 37.4) to ERR bits in JCDERR. When an error is detected, the JPU generates an interrupt signal and stops decoding. The stored code is 1010 (default value) at the start of processing for the next frame or after a bus reset.

Table 37.4 Decoding Error Codes

Code	Description
0000	Normal
0001	SIO not detected: SIO not detected until EOI detected
0010	SOF1 to SOFF detected
0011	Subsampling setting other than YCbCr 4:4:4 (H = 1:1:1, V = 1:1:1)/YCbCr 4:2:2 (H = 2:1:1, V = 1:1:1)/YCbCr 4:1:1 (H = 4:1:1, V = 1:1:1)/YCbCr 4:2:0 (H = 2:1:1, V = 2:1:1) detected
0100	SOF accuracy error: Other than 8 detected
0101	DQT accuracy error: Other than 0 detected
0110	Component error 1: The number of SOF0 header components detected is other than 1, 3, or 4
0111	Component error 2: The number of components differs between SOF0 header and SOS
1000	SOF0, DQT, and DHT not detected when SOS detected
1001	SOS not detected: SOS not detected until EOI detected
1010	EOI not detected (default)
1011	Restart interval data number error detected
1100	Image size error detected
1101	Last MCU data number error detected
1110	Block data number error detected

39.3.24 LCDC Status Register (LDSR)

LDSR indicates status related to the LCDC operations



Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0.
26 to 16	MRLS[10:0]	H'000	R	Memory Read Line Status These bits indicate the number of lines which have been read from external memory.
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	MRS	0	R	Main LCD Register Side Status Indicates the register side of the main LCD used by the LCDC. 0: Side A is used 1: Side B is used
7 to 2	—	All 0	R	Reserved These bits are always read as 0.
1	AS	0	R	SYS Interface Access Status Indicates the access status of the SYS interface. When the status indicates bus busy, do not issue the next transaction. Otherwise, operation is not guaranteed. 0: Bus idle 1: Bus busy (read or write access is being executed or is waiting)

42.2 Register Descriptions

Table 42.1 lists the registers used in the 2D-DMAC. Table 42.2 shows the register status in each processing mode.

Table 42.1 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
Interrupt status clear register	CHSTCLR	R/W	H'FEA0 0010	32
Channel priority switch register	CHPRI	R/W	H'FEA0 0014	32
CH0 control register	CH0CTRL	R/W	H'FEA0 0020	32
CH1 control register	CH1CTRL	R/W	H'FEA0 0024	32
CH2 control register	CH2CTRL	R/W	H'FEA0 0028	32
CH3 control register	CH3CTRL	R/W	H'FEA0 002C	32
CH4 control register	CH4CTRL	R/W	H'FEA0 0120	32
CH5 control register	CH5CTRL	R/W	H'FEA0 0124	32
CH6 control register	CH6CTRL	R/W	H'FEA0 0128	32
CH7 control register	CH7CTRL	R/W	H'FEA0 012C	32
CH0 input/output swap register	CH0SWAP	R/W	H'FEA0 0030	32
CH1 input/output swap register	CH1SWAP	R/W	H'FEA0 0034	32
CH2 input/output swap register	CH2SWAP	R/W	H'FEA0 0038	32
CH3 input/output swap register	CH3SWAP	R/W	H'FEA0 003C	32
CH4 input/output swap register	CH4SWAP	R/W	H'FEA0 0130	32
CH5 input/output swap register	CH5SWAP	R/W	H'FEA0 0134	32
CH6 input/output swap register	CH6SWAP	R/W	H'FEA0 0138	32
CH7 input/output swap register	CH7SWAP	R/W	H'FEA0 013C	32
CH0 source address register	CH0SAR	R/W	H'FEA0 0080	32
CH0 destination address register	CH0DAR	R/W	H'FEA0 0084	32
CH0 destination pixel register	CH0DPXL	R/W	H'FEA0 0088	32
CH0 source format register	CH0SFMT	R/W	H'FEA0 008C	32
CH0 destination format register	CH0DFMT	R/W	H'FEA0 0090	32
CH0 source line address register	CH0SARE	R	H'FEA0 0094	32
CH0 destination line address register	CH0DARE	R	H'FEA0 0098	32
CH0 destination pixel processing register	CH0DPXLE	R	H'FEA0 009C	32

45.3.3 Port A/B Output FIFO Status Register (A_DOFF_ST/B_DOFF_ST)

A_DOFF_ST/B_DOFF_ST is a 24-bit readable/writable register. It can be used to read the output FIFO states for serial ports A/B, the number of stored sample data, and the history of overflow and underflow errors.

The OF and UF bits clear the history when they are written to 0.

For clearing procedures for OF and UF bits, see section 45.6, FIFO Overflow/Underflow Specifications.

Bit:	23	22	21	20	19	18	17	16
	—	—	ST[1:0]		—	—	—	SZ[8]
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SZ[7:0]								—	—	—	OF	—	—	—	UF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/(W)*	R	R	R	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
23, 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21, 20	ST[1:0]	00	R	FIFO State 00: Empty state. 01: Less than half of data areas are occupied. 10: More than half of data areas are occupied. 11: Full state.
19 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

(a) Transmit Descriptor 0 (TD0)

TD0 indicates the transmit frame status informing frame transmission status.

(The underlined bits are subject to write-back in the table below.)

Bit	Bit Name	Initial Value	R/W	Description
31	TACT	0	R/W	Transmit Descriptor Valid Indicates that the corresponding descriptor is valid. This bit is set to 1 by software. This bit is cleared to 0 by hardware when a transmit frame has been completely transferred or when transmission has been aborted due to some cause.
30	TDLE	0	R/W	Transmit Descriptor Ring End When set to 1, this bit indicates that the corresponding descriptor is the last one of the descriptor ring.
29 28	TFP1 TFP0	0 0	R/W R/W	Transmit Frame Positions 1 and 0 These bits relate the transmit buffer to the transmit frame. The settings of these bits and the TBL bits should be logically correct in the consecutive descriptors. 00: Transmission of the frame of the transmit buffer specified by this descriptor is continued. (The frame is incomplete.) 01: The transmit buffer specified by this descriptor contains the end of the frame (The frame is complete.) 10: The transmit buffer specified by this descriptor is the start of the frame (The frame is incomplete.) 11: The contents in the transmit buffer specified by this descriptor correspond to one frame (single-frame/single-buffer).
27	TFE	0	R/W	Transmit Frame Error When set to 1, this bit indicates that an error is indicated by any of the TFS bits. (By so setting TRSCER, it is possible to prevent this bit from being set by an event indicated by TFS7 to TFS0. It is impossible, however, if an event indicated by TFS7 to TFS0 also causes TFS8 to be set.) 1: Frame transmission has been aborted.
26	TWBI	0	R/W	Write-Back Completion Interrupt Notification (This bit is valid when TRIMD is set so.) 0: nop 1: An interrupt is generated upon completion of write-back to this descriptor.

Notes: 1. This pin is pulled up in this LSI. When designing a board emulator is available or using interrupts or resets via the H-UDI or emulator, the use of external pull-up resistors will not cause any problem.

2. When designing a board emulator is available or using interrupts or resets via the H-UDI or emulator, the $\overline{\text{TRST}}$ pin should be designed so that it can be controlled independently and can be controlled to retain low level while the $\overline{\text{RESET}}$ pin is asserted at a power-on reset.

3. This pin should be connected to ground. However, when connected to a ground pin, the following problem occurs. Since the $\overline{\text{TRST}}$ pin is pulled up within this LSI, a weak current flows when the pin is externally connected to a ground pin. The value of the current is determined by a resistance of the pull-up MOS for the port pin. Although this current does not affect the operation of this LSI, it consumes unnecessary power. Pulling up the $\overline{\text{TRST}}$ pin can be disabled by the pull-down control register (PULCR) of the pin function controller (PFC). For details, see section 48, Pin Function Controller (PFC).

The TCK clock or the CPG of this LSI should be set to ensure that the frequency of the TCK clock is less than the peripheral-clock frequency of this LSI.

Register Name	Abbreviation	R/W	Address	Module	Access Size
CH1 control register	CH1CTRL	R/W	H'FEA0 0024	2D-DMAC	32
CH2 control register	CH2CTRL	R/W	H'FEA0 0028		32
CH3 control register	CH3CTRL	R/W	H'FEA0 002C		32
CH4 control register	CH4CTRL	R/W	H'FEA0 0120		32
CH5 control register	CH5CTRL	R/W	H'FEA0 0124		32
CH6 control register	CH6CTRL	R/W	H'FEA0 0128		32
CH7 control register	CH7CTRL	R/W	H'FEA0 012C		32
CH0 input/output swap register	CH0SWAP	R/W	H'FEA0 0030		32
CH1 input/output swap register	CH1SWAP	R/W	H'FEA0 0034		32
CH2 input/output swap register	CH2SWAP	R/W	H'FEA0 0038		32
CH3 input/output swap register	CH3SWAP	R/W	H'FEA0 003C		32
CH4 input/output swap register	CH4SWAP	R/W	H'FEA0 0130		32
CH5 input/output swap register	CH5SWAP	R/W	H'FEA0 0134		32
CH6 input/output swap register	CH6SWAP	R/W	H'FEA0 0138		32
CH7 input/output swap register	CH7SWAP	R/W	H'FEA0 013C		32
CH0 source address register	CH0SAR	R/W	H'FEA0 0080		32
CH0 destination address register	CH0DAR	R/W	H'FEA0 0084		32
CH0 destination pixel register	CH0DPXL	R/W	H'FEA0 0088		32
CH0 source format register	CH0SFMT	R/W	H'FEA0 008C		32
CH0 destination format register	CH0DFMT	R/W	H'FEA0 0090		32
CH0 source line address register	CH0SARE	R	H'FEA0 0094		32
CH0 destination line address register	CH0DARE	R	H'FEA0 0098		32
CH0 destination pixel processing register	CH0DPXLE	R	H'FEA0 009C		32
CH1 source address register	CH1SAR	R/W	H'FEA0 00A0		32
CH1 destination address register	CH1DAR	R/W	H'FEA0 00A4		32
CH1 destination pixel register	CH1DPXL	R/W	H'FEA0 00A8		32
CH1 source format register	CH1SFMT	R/W	H'FEA0 00AC		32
CH1 destination format register	CH1DFMT	R/W	H'FEA0 00B0		32
CH1 source line address register	CH1SARE	R	H'FEA0 00B4		32
CH1 destination line address register	CH1DARE	R	H'FEA0 00B8		32
CH1 destination pixel processing register	CH1DPXLE	R	H'FEA0 00BC		32
CH2 source address register	CH2SAR	R/W	H'FEA0 00C0		32