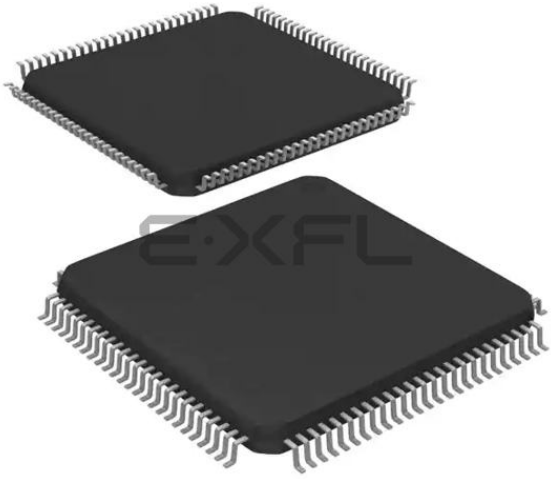

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	85
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32wg280f64-qfp100

Figure 2.2. EFM32WG280 Memory Map with largest RAM and Flash sizes

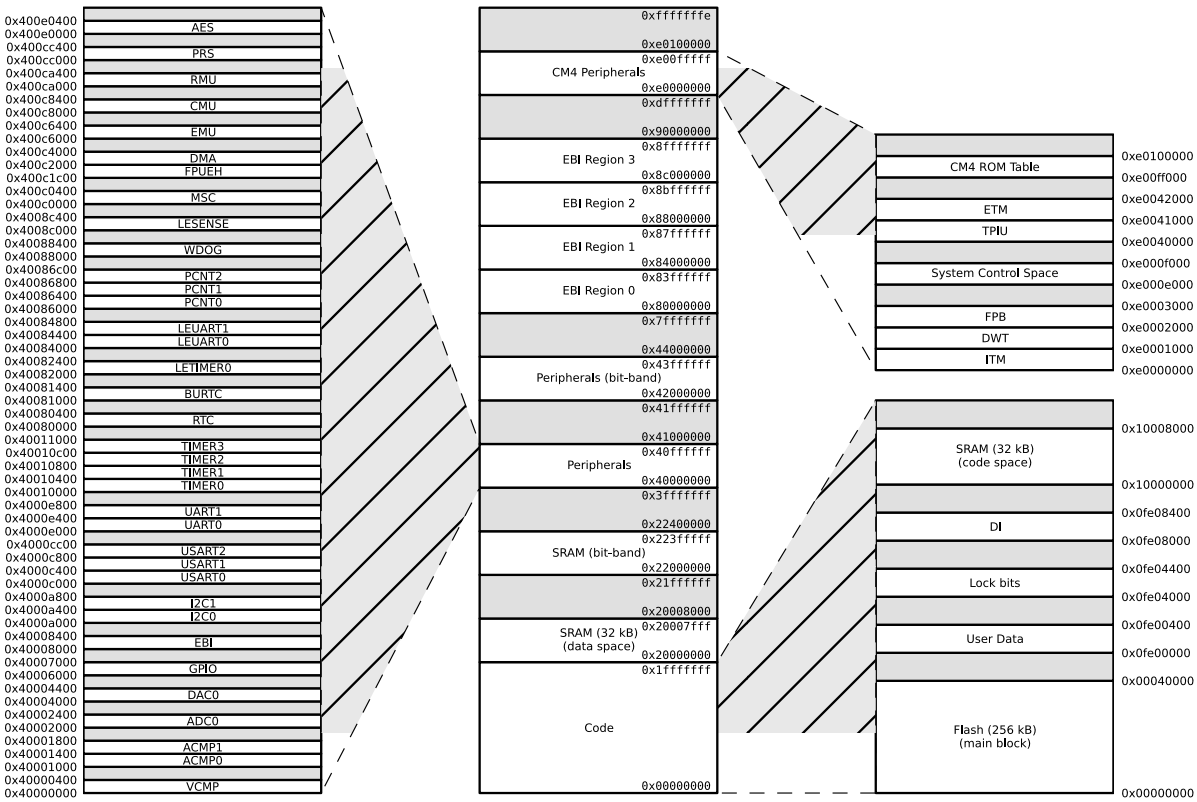


Figure 3.5. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11MHz

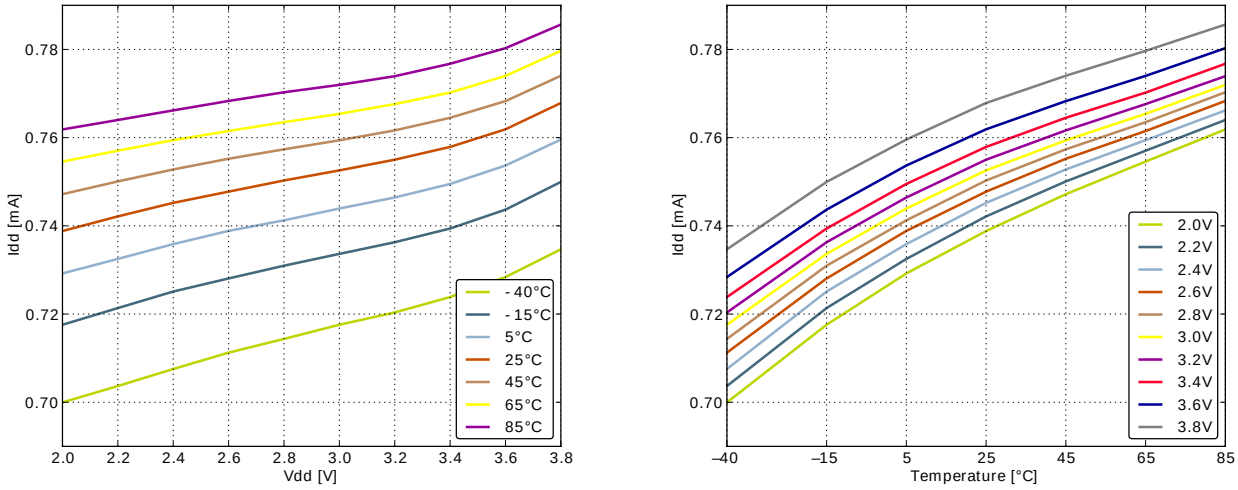


Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 6.6MHz

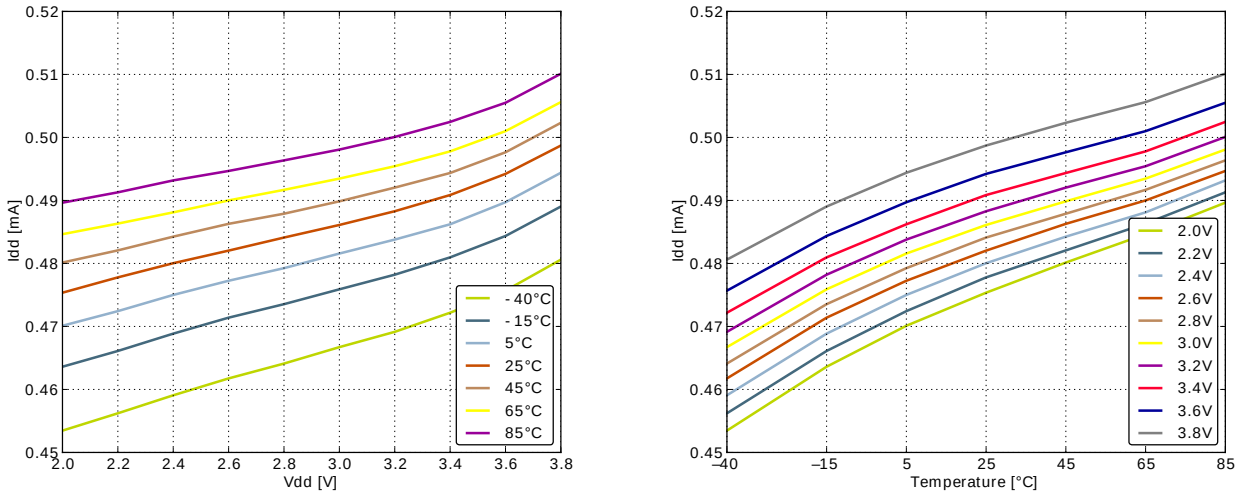
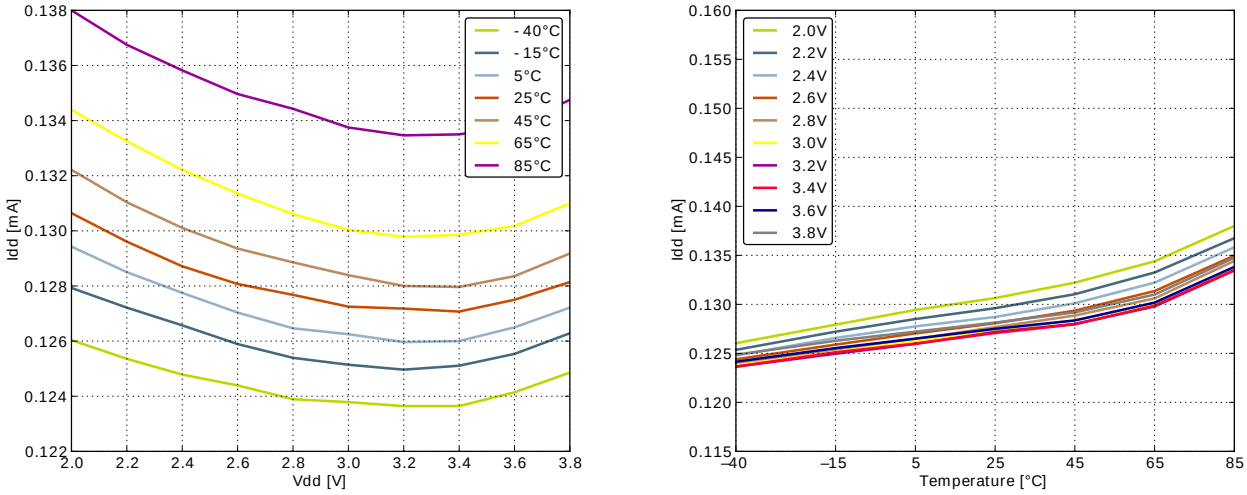
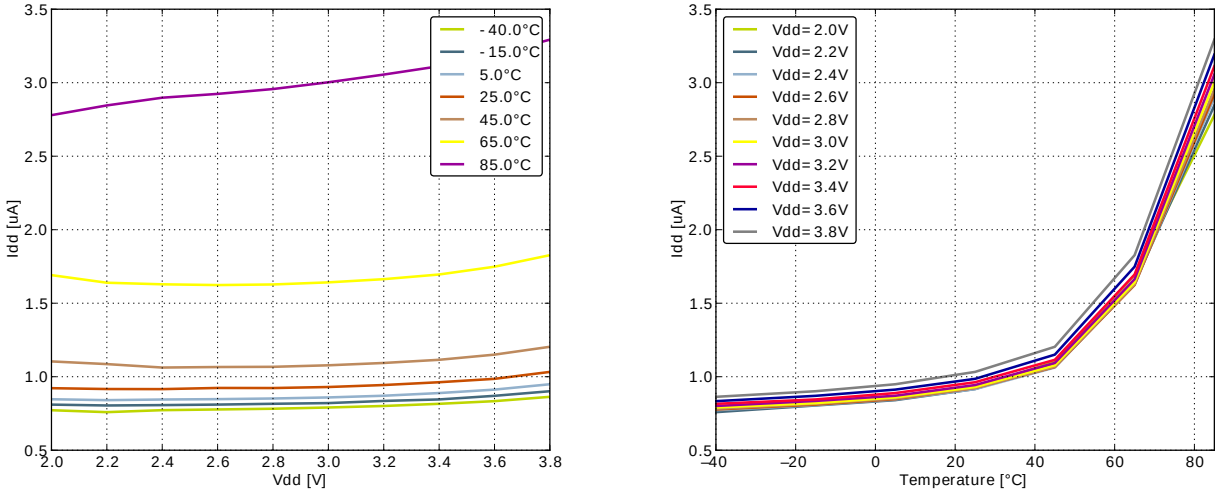


Figure 3.7. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 1.2MHz



3.4.2 EM2 Current Consumption

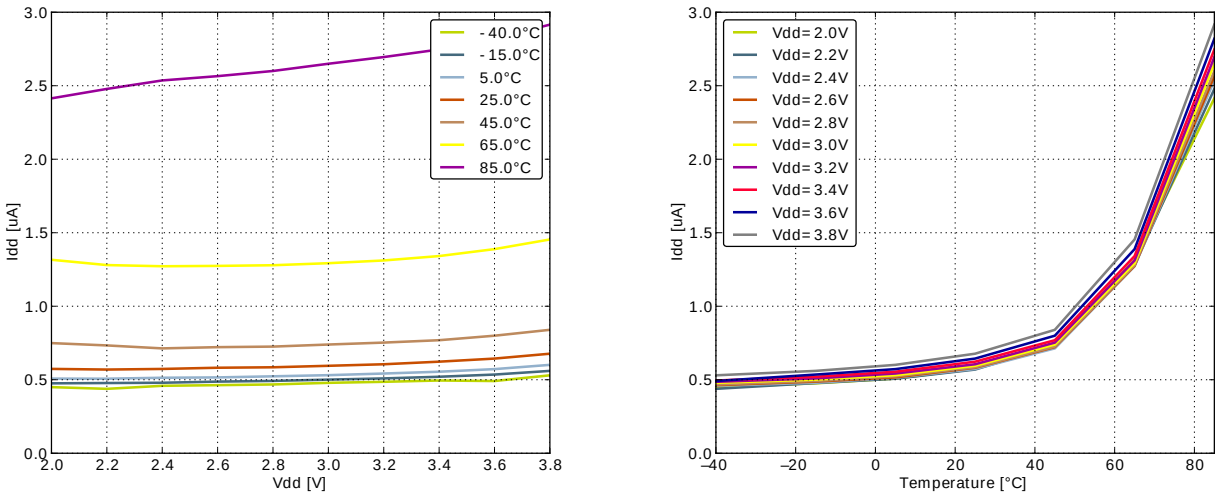
Figure 3.8. EM2 current consumption. RTC[1] prescaled to 1kHz, 32.768 kHz LFRCO.



[1]Using backup RTC.

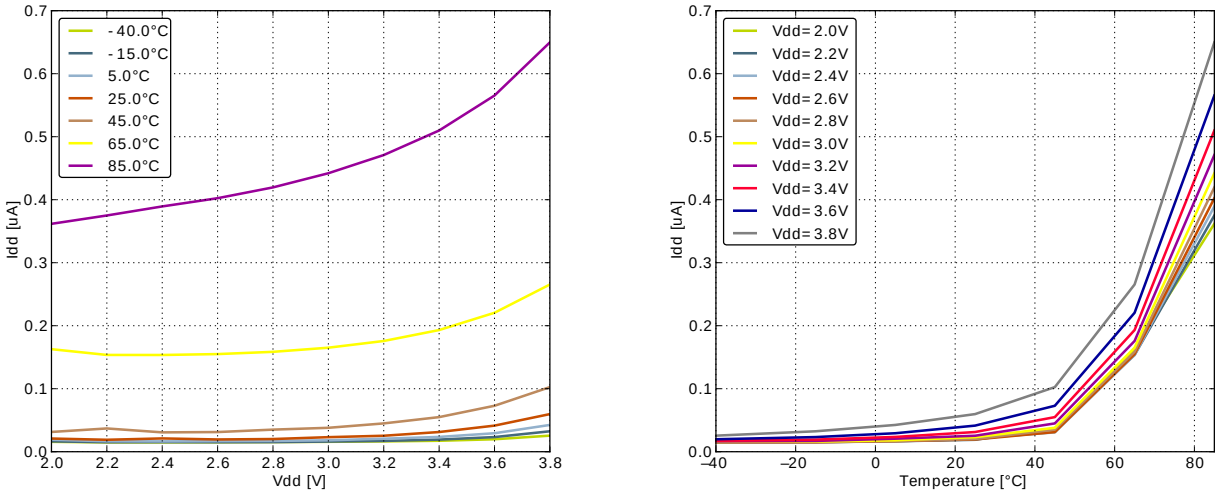
3.4.3 EM3 Current Consumption

Figure 3.9. EM3 current consumption.



3.4.4 EM4 Current Consumption

Figure 3.10. EM4 current consumption.



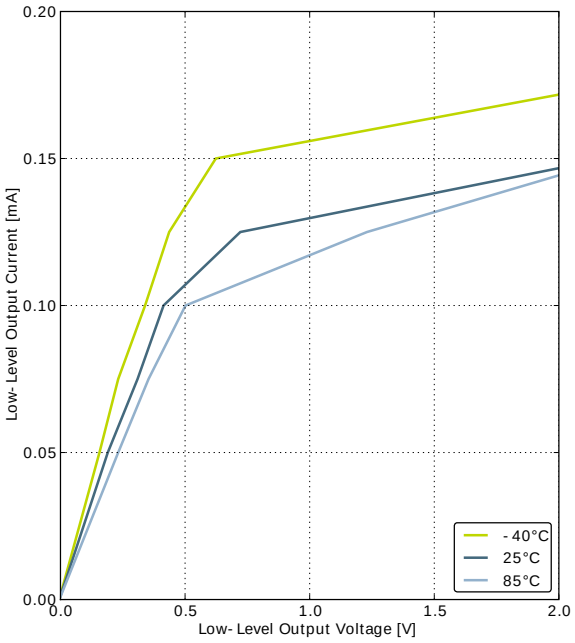
3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

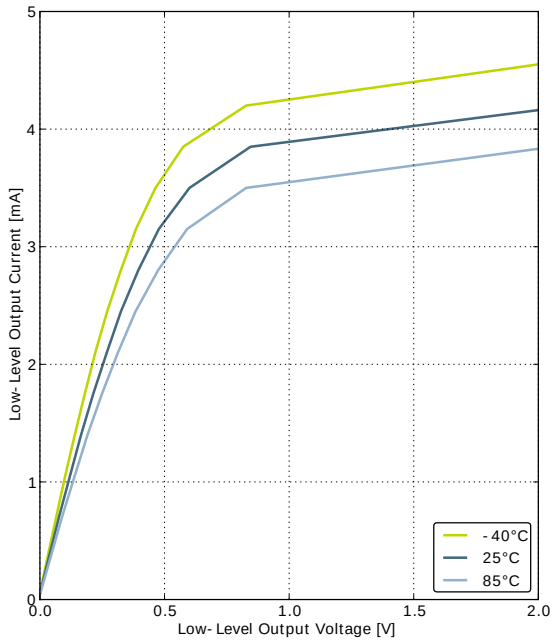
Table 3.5. Energy Modes Transitions

Symbol	Parameter	Min	Typ	Max	Unit
t_{EM10}	Transition time from EM1 to EM0		0		HF-CORE-CLK cycles
t_{EM20}	Transition time from EM2 to EM0		2		µs
t_{EM30}	Transition time from EM3 to EM0		2		µs
t_{EM40}	Transition time from EM4 to EM0		163		µs

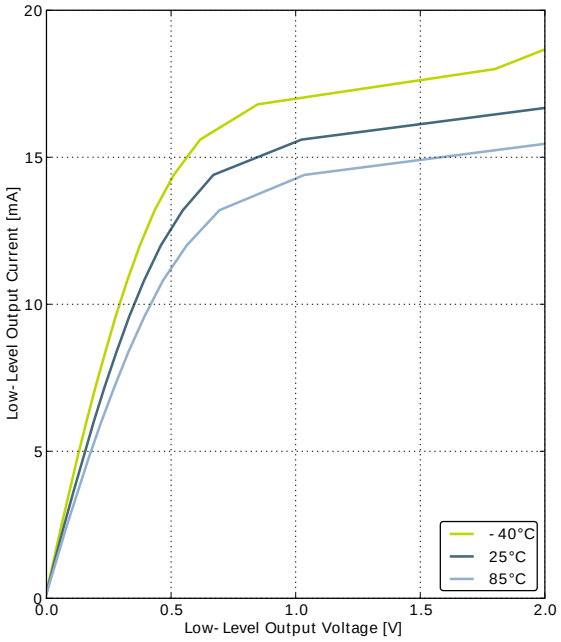
Figure 3.11. Typical Low-Level Output Current, 2V Supply Voltage



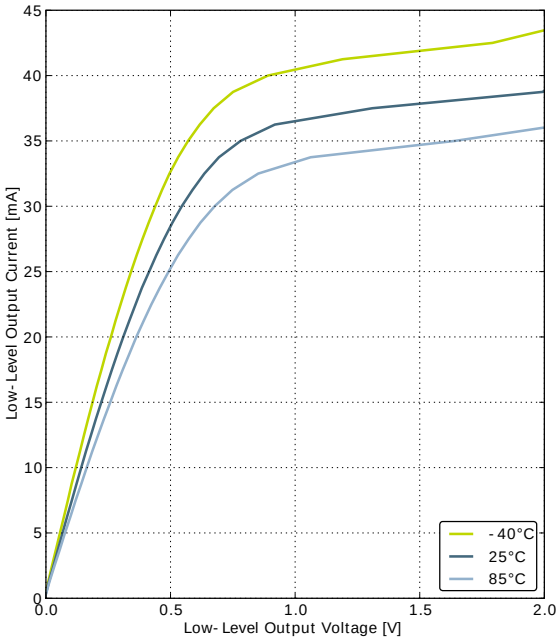
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

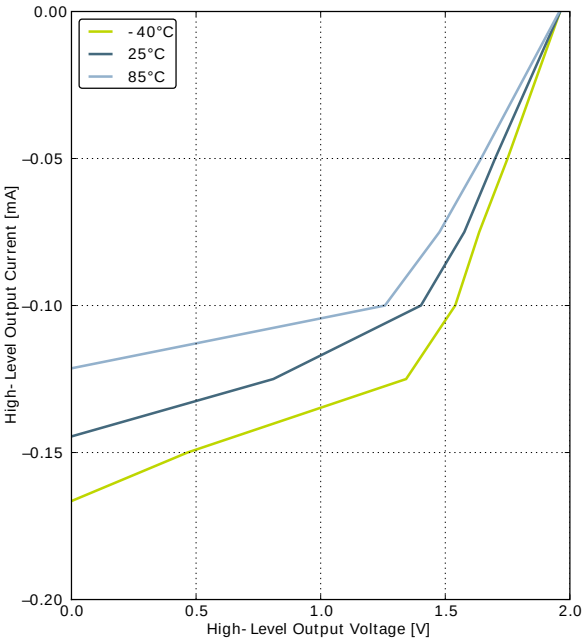


GPIO_Px_CTRL DRIVEMODE = STANDARD

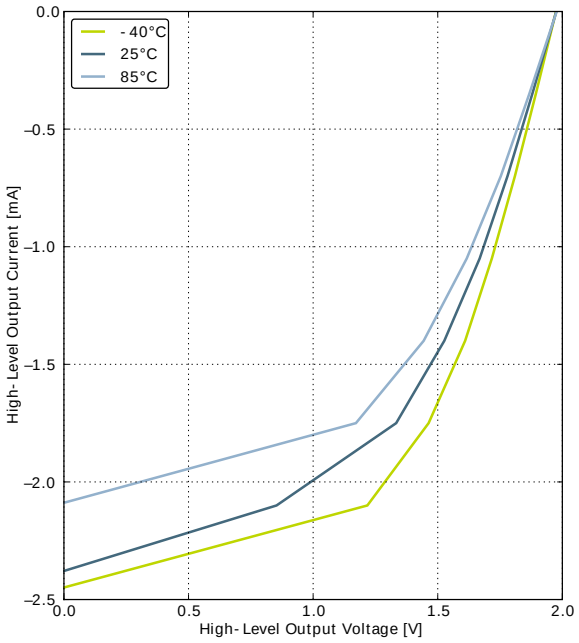


GPIO_Px_CTRL DRIVEMODE = HIGH

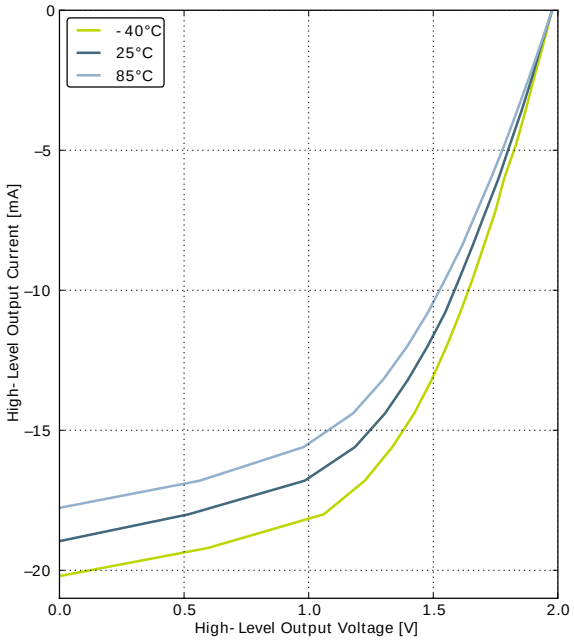
Figure 3.12. Typical High-Level Output Current, 2V Supply Voltage



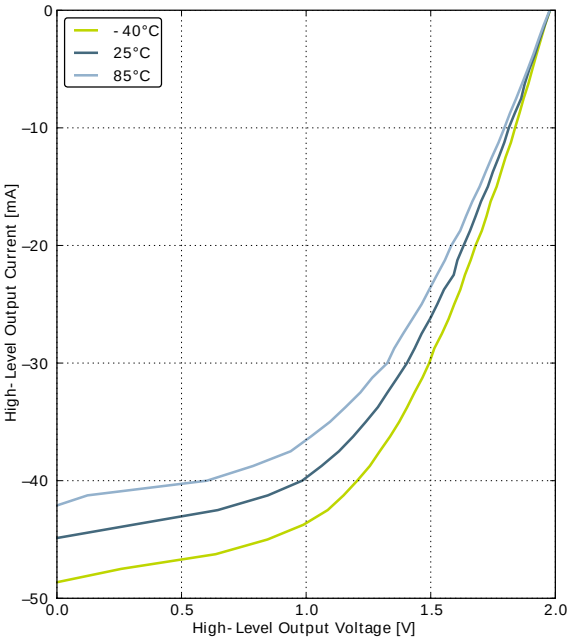
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

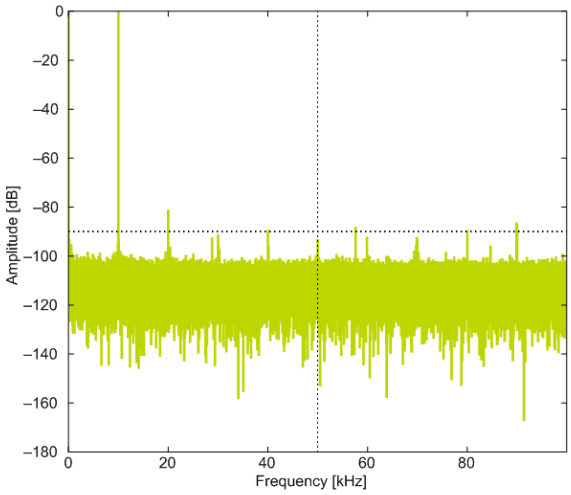


GPIO_Px_CTRL DRIVEMODE = HIGH

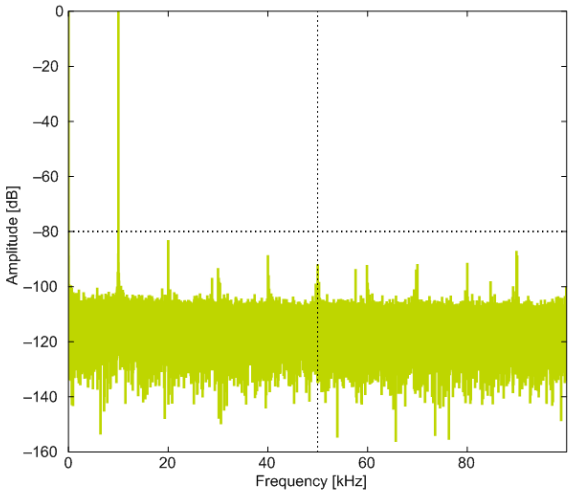
Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
		1 MSamples/s, 12 bit, differential, 2xV_{DD} reference		68		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		66		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	62	66		dB
		200 kSamples/s, 12 bit, differential, 2xV_{DD} reference		69		dB
$SFDR_{ADC}$	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differential, V_{DD} reference		76		dBc
		1 MSamples/s, 12 bit, differential, 2xV_{DD} reference		75		dBc
		1 MSamples/s, 12 bit, differential, 5V reference		69		dBc
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		76		dBc

3.10.1 Typical performance

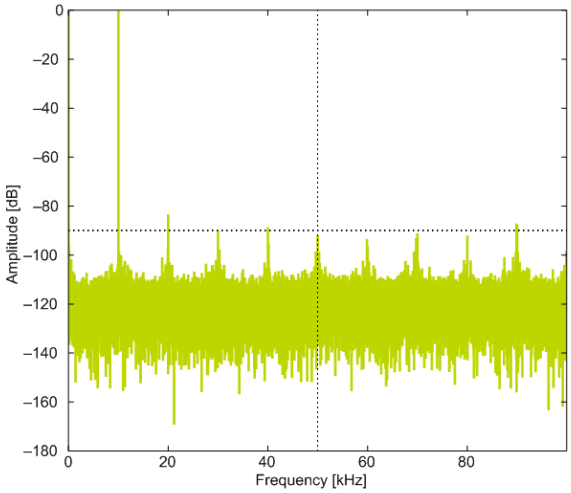
Figure 3.26. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°C



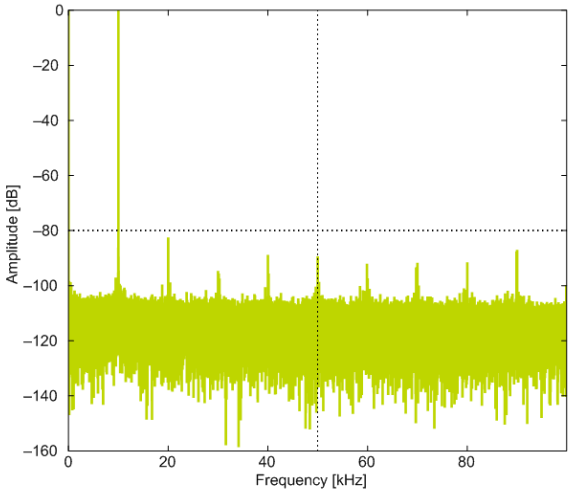
1.25V Reference



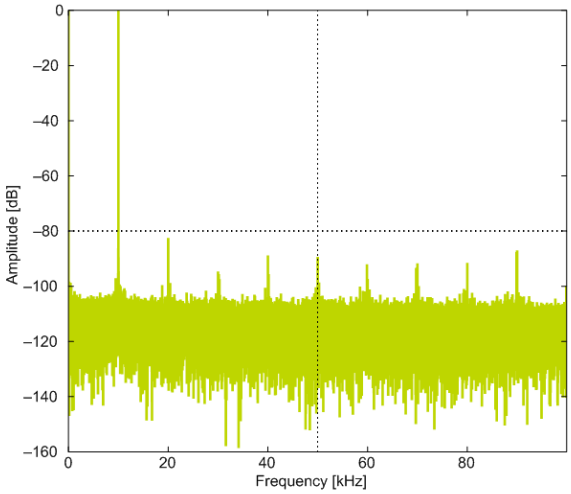
2.5V Reference



2XVDDVSS Reference



5VDIFF Reference



VDD Reference

Figure 3.34. OPAMP Negative Power Supply Rejection Ratio

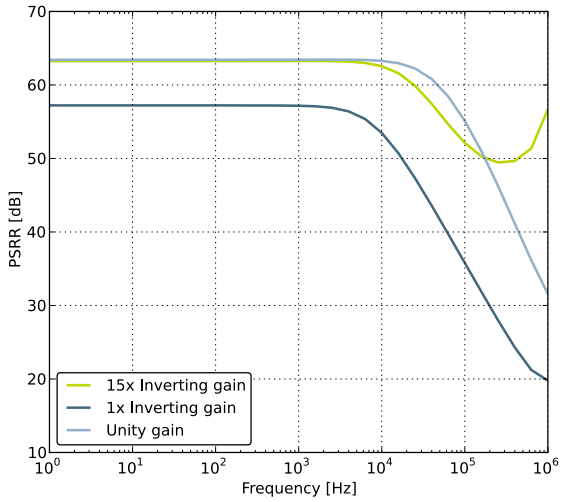


Figure 3.35. OPAMP Voltage Noise Spectral Density (Unity Gain) V_{out}=1V

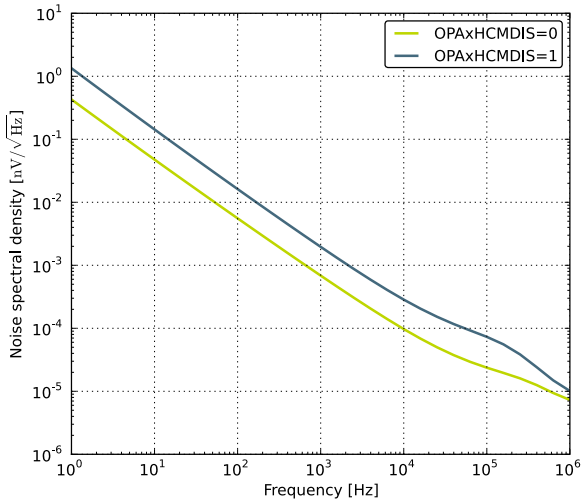
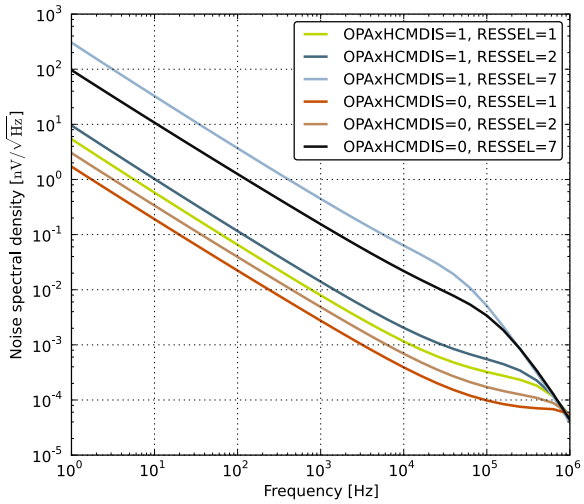


Figure 3.36. OPAMP Voltage Noise Spectral Density (Non-Unity Gain)



3.13 Analog Comparator (ACMP)

Table 3.18. ACMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ACMPIN}	Input voltage range		0		V_{DD}	V
V_{ACMPCM}	ACMP Common Mode voltage range		0		V_{DD}	V
I_{ACMP}	Active current	BIASPROG=0b0000, FULLBIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		0.1	0.4	µA
		BIASPROG=0b1111, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.87	15	µA
		BIASPROG=0b1111, FULLBIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		195	520	µA
$I_{ACMPREF}$	Current consumption of internal voltage reference	Internal voltage reference off. Using external voltage reference		0		µA
		Internal voltage reference		5		µA
$V_{ACMPOFFSET}$	Offset voltage	BIASPROG= 0b1010, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register	-12	0	12	mV
$V_{ACMPHYST}$	ACMP hysteresis	Programmable		17		mV
R_{CSRES}	Capacitive Sense Internal Resistance	CSRESSEL=0b00 in ACMPn_INPUTSEL		39		kOhm
		CSRESSEL=0b01 in ACMPn_INPUTSEL		71		kOhm
		CSRESSEL=0b10 in ACMPn_INPUTSEL		104		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		136		kOhm
$t_{ACMPSTART}$	Startup time				10	µs

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 47) . $I_{ACMPREF}$ is zero if an external voltage reference is used.

Total ACMP Active Current

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \quad (3.1)$$

3.14 Voltage Comparator (VCMP)

Table 3.19. VCMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{VCMPIN}	Input voltage range			V_{DD}		V
V_{VCMPCM}	VCMP Common Mode voltage range			V_{DD}		V
I_{VCMP}	Active current	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register		0.3	0.6	µA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0.		22	35	µA
$t_{VCMPREF}$	Startup time reference generator	NORMAL		10		µs
$V_{VCMPOFFSET}$	Offset voltage	Single ended		10		mV
		Differential		10		mV
$V_{VCMPHYST}$	VCMP hysteresis			61	210	mV
$t_{VCMPSTART}$	Startup time				10	µs

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

VCMP Trigger Level as a Function of Level Setting

$$V_{DD\ Trigger\ Level}=1.667V+0.034 \times TRIGLEVEL \quad (3.2)$$

3.15 EBI

Figure 3.38. EBI Write Enable Timing

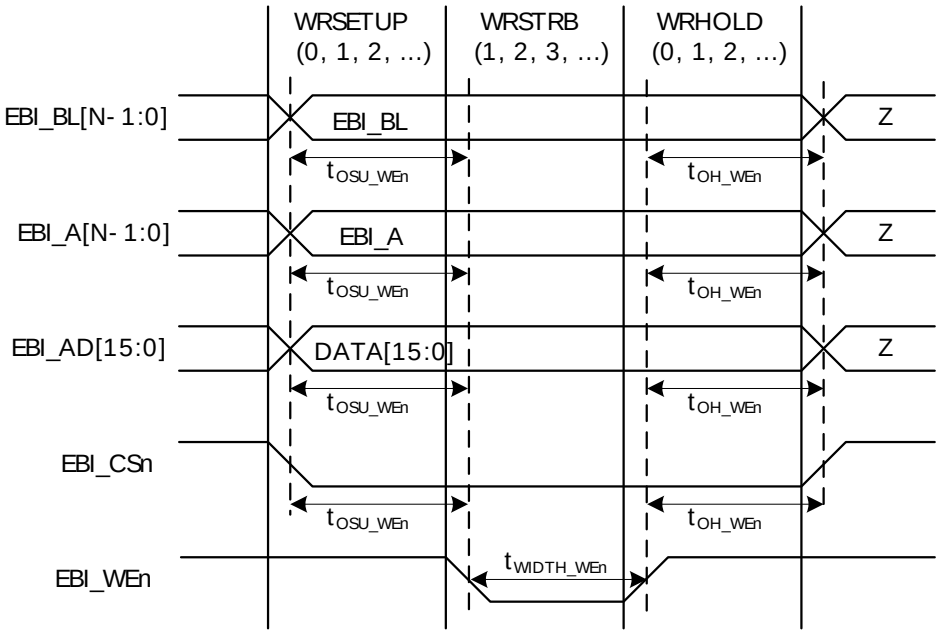


Figure 3.41. EBI Read Enable Related Timing Requirements

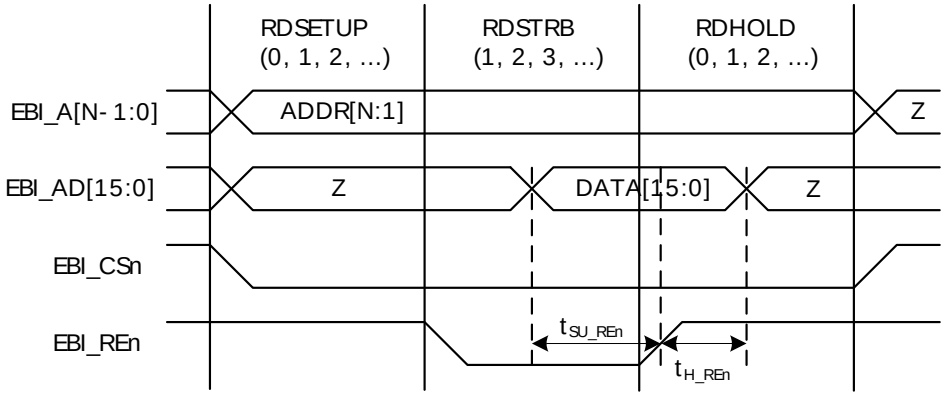


Table 3.23. EBI Read Enable Related Timing Requirements

Symbol	Parameter	Min	Typ	Max	Unit
t_{SU_REn} [1 2 3 4]	Setup time, from EBI_AD valid to trailing EBI_REn edge	37			ns
t_{H_Ren} [1 2 3 4]	Hold time, from trailing EBI_REn edge to EBI_AD invalid	-1			ns

[1]Applies for all addressing modes (figure only shows D16A8).
[2]Applies for both EBI_REn and EBI_NANDREn (figure only shows EBI_REn)
[3]Applies for all polarities (figure only shows active low signals)
[4]Measurement done at 10% and 90% of V_{DD} (figure shows 50% of $_{VDD}$)

Figure 3.42. EBI Ready/Wait Related Timing Requirements

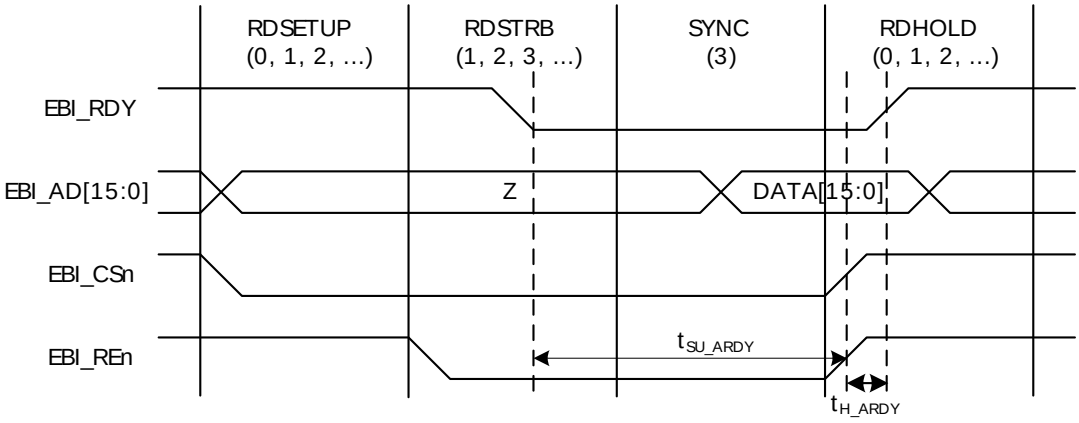


Table 3.24. EBI Ready/Wait Related Timing Requirements

Symbol	Parameter	Min	Typ	Max	Unit
t_{SU_ARDY} [1 2 3 4]	Setup time, from EBI_ARDY valid to trailing EBI_REn, EBI_WEn edge	37 + (3 * $t_{HFCORECLK}$)			ns

Table 3.27. I2C Fast-mode Plus (Fm+)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		1000[1]	kHz
t_{LOW}	SCL clock low time	0.5			µs
t_{HIGH}	SCL clock high time	0.26			µs
$t_{SU,DAT}$	SDA set-up time	50			ns
$t_{HD,DAT}$	SDA hold time	8			ns
$t_{SU,STA}$	Repeated START condition set-up time	0.26			µs
$t_{HD,STA}$	(Repeated) START condition hold time	0.26			µs
$t_{SU,STO}$	STOP condition set-up time	0.26			µs
t_{BUF}	Bus free time between a STOP and a START condition	0.5			µs

[1]For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32WG Reference Manual.

3.17 USART SPI

Figure 3.43. SPI Master Timing

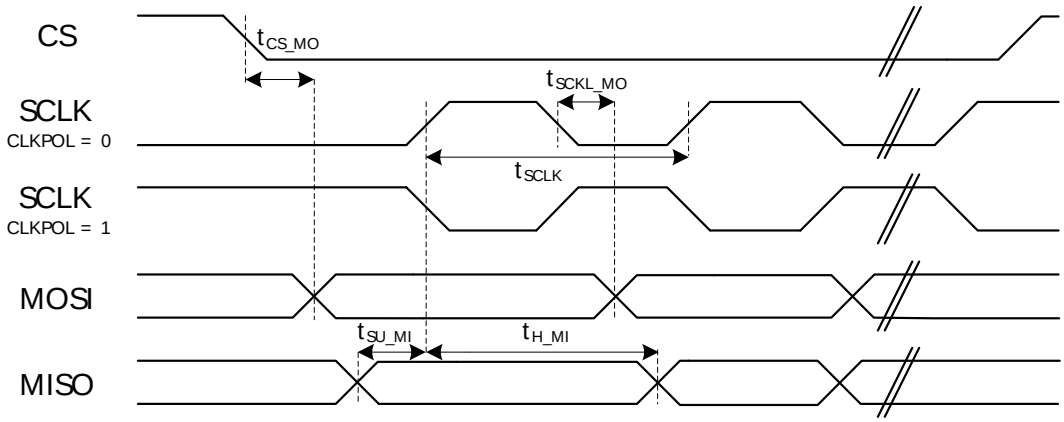


Table 3.28. SPI Master Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{SCLK} [1] [2]	SCLK period		2 * $t_{HFPERCLK}$			ns
t_{CS_MO} [1] [2]	CS to MOSI		-2.00		2.00	ns
t_{SCLK_MO} [1] [2]	SCLK to MOSI		-1.00		3.00	ns
t_{SU_MI} [1] [2]	MISO setup time	IOVDD = 3.0 V	36.00			ns
t_{H_MI} [1] [2]	MISO hold time		-6.00			ns

[1]Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

[2]Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

Table 3.29. SPI Master Timing with SSSEARLY and SMSDELAY

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{SCLK} [1] [2]	SCLK period		2 * $t_{HFPER-CLK}$			ns
t_{CS_MO} [1] [2]	CS to MOSI		-2.00		2.00	ns
t_{SCLK_MO} [1] [2]	SCLK to MOSI		-1.00		3.00	ns
t_{SU_MI} [1] [2]	MISO setup time	IOVDD = 3.0 V	-32.00			ns
t_{H_MI} [1] [2]	MISO hold time		63.00			ns

[1]Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
[2]Measurement done at 10% and 90% of V_{DD} (figure shows 50% of $_{VDD}$)

Figure 3.44. SPI Slave Timing

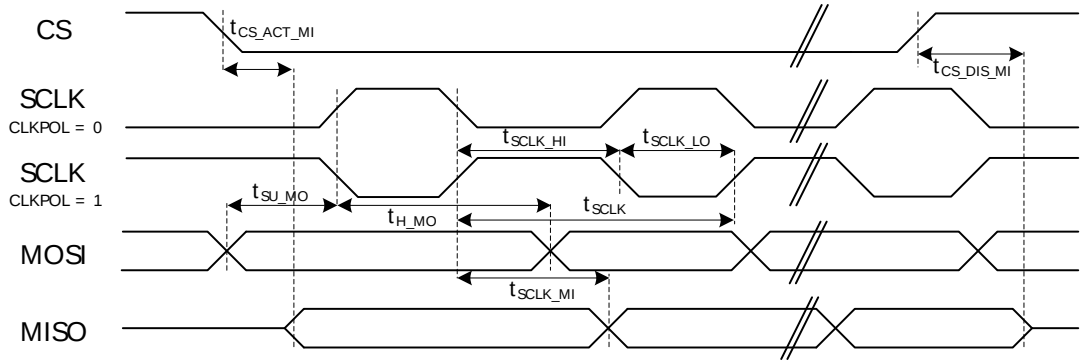


Table 3.30. SPI Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{SCLK_sl} [1] [2]	SCKL period	6 * $t_{HFPER-CLK}$			ns
t_{SCLK_hi} [1] [2]	SCLK high period	3 * $t_{HFPER-CLK}$			ns
t_{SCLK_lo} [1] [2]	SCLK low period	3 * $t_{HFPER-CLK}$			ns
$t_{CS\_ACT\_MI}$ [1] [2]	CS active to MISO	5.00		35.00	ns
$t_{CS\_DIS\_MI}$ [1] [2]	CS disable to MISO	5.00		35.00	ns
t_{SU_MO} [1] [2]	MOSI setup time	5.00			ns
t_{H_MO} [1] [2]	MOSI hold time	2 + 2 * $t_{HF-PERCLK}$			ns
t_{SCLK_MI} [1] [2]	SCLK to MISO	7 + $t_{HFPER-CLK}$		42 + 2 * $t_{HFPERCLK}$	ns

[1]Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
[2]Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

Table 3.31. SPI Slave Timing with SSSEARLY and SMSDELAY

Symbol	Parameter	Min	Typ	Max	Unit
t_{SCLK_sl} [1] [2]	SCKL period	6 * $t_{HFPER-CLK}$			ns

Symbol	Parameter	Min	Typ	Max	Unit
t_{SCLK_hi} [1][2]	SCLK high period	3 * $t_{HFPER-CLK}$			ns
t_{SCLK_lo} [1][2]	SCLK low period	3 * $t_{HFPER-CLK}$			ns
$t_{CS\_ACT\_MI}$ [1][2]	CS active to MISO	5.00		35.00	ns
$t_{CS\_DIS\_MI}$ [1][2]	CS disable to MISO	5.00		35.00	ns
t_{SU_MO} [1][2]	MOSI setup time	5.00			ns
t_{H_MO} [1][2]	MOSI hold time	2 + 2 * $t_{HF-PERCLK}$			ns
t_{SCLK_MI} [1][2]	SCLK to MISO	-264 + $t_{HF-PERCLK}$		-234 + 2 * $t_{HFPERCLK}$	ns

[1]Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
[2]Measurement done at 10% and 90% of V_{DD} (figure shows 50% of $_{VDD}$)

3.18 Digital Peripherals

Table 3.32. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{USART}	USART current	USART idle current, clock enabled		4.0		µA/MHz
I_{UART}	UART current	UART idle current, clock enabled		3.8		µA/MHz
I_{LEUART}	LEUART current	LEUART idle current, clock enabled		194.0		nA
I_{I2C}	I2C current	I2C idle current, clock enabled		7.6		µA/MHz
I_{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		6.5		µA/MHz
$I_{LETIMER}$	LETIMER current	LETIMER idle current, clock enabled		85.8		nA
I_{PCNT}	PCNT current	PCNT idle current, clock enabled		91.4		nA
I_{RTC}	RTC current	RTC idle current, clock enabled		54.6		nA
I_{AES}	AES current	AES idle current, clock enabled		1.8		µA/MHz
I_{GPIO}	GPIO current	GPIO idle current, clock enabled		3.4		µA/MHz
I_{EBI}	EBI current	EBI idle current, clock enabled		6.5		µA/MHz
I_{PRS}	PRS current	PRS idle current		3.9		µA/MHz
I_{DMA}	DMA current	Clock enable		10.9		µA/MHz

4 Pinout and Package

Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32WG280.

4.1 Pinout

The *EFM32WG280* pinout is shown in Figure 4.1 (p. 57) and Table 4.1 (p. 57). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 4.1. EFM32WG280 Pinout (top view, not to scale)

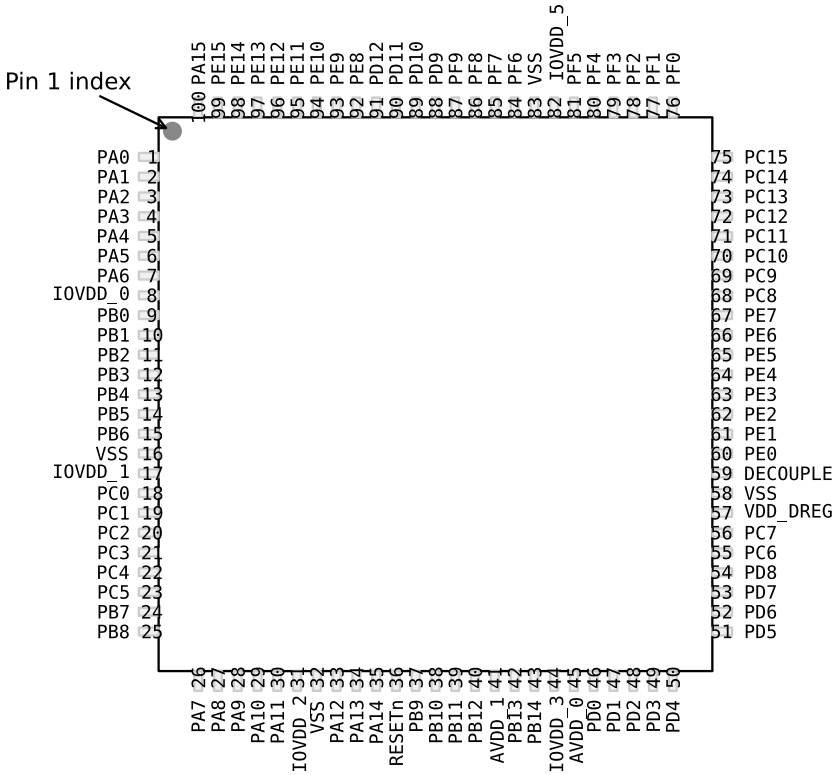


Table 4.1. Device Pinout

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
1	PA0		EBI_AD09 #0/1/2	TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
2	PA1		EBI_AD10 #0/1/2	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
3	PA2		EBI_AD11 #0/1/2	TIM0_CC2 #0/1		CMU_CLK0 #0

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_A00	PA12	PA12	PA12					External Bus Interface (EBI) address output pin 00.
EBI_A01	PA13	PA13	PA13					External Bus Interface (EBI) address output pin 01.
EBI_A02	PA14	PA14	PA14					External Bus Interface (EBI) address output pin 02.
EBI_A03	PB9	PB9	PB9					External Bus Interface (EBI) address output pin 03.
EBI_A04	PB10	PB10	PB10					External Bus Interface (EBI) address output pin 04.
EBI_A05	PC6	PC6	PC6					External Bus Interface (EBI) address output pin 05.
EBI_A06	PC7	PC7	PC7					External Bus Interface (EBI) address output pin 06.
EBI_A07	PE0	PE0	PE0					External Bus Interface (EBI) address output pin 07.
EBI_A08	PE1	PE1	PE1					External Bus Interface (EBI) address output pin 08.
EBI_A09	PE2	PC9	PC9					External Bus Interface (EBI) address output pin 09.
EBI_A10	PE3	PC10	PC10					External Bus Interface (EBI) address output pin 10.
EBI_A11	PE4	PE4	PE4					External Bus Interface (EBI) address output pin 11.
EBI_A12	PE5	PE5	PE5					External Bus Interface (EBI) address output pin 12.
EBI_A13	PE6	PE6	PE6					External Bus Interface (EBI) address output pin 13.
EBI_A14	PE7	PE7	PE7					External Bus Interface (EBI) address output pin 14.
EBI_A15	PC8	PC8	PC8					External Bus Interface (EBI) address output pin 15.
EBI_A16	PB0	PB0	PB0					External Bus Interface (EBI) address output pin 16.
EBI_A17	PB1	PB1	PB1					External Bus Interface (EBI) address output pin 17.
EBI_A18	PB2	PB2	PB2					External Bus Interface (EBI) address output pin 18.
EBI_A19	PB3	PB3	PB3					External Bus Interface (EBI) address output pin 19.
EBI_A20	PB4	PB4	PB4					External Bus Interface (EBI) address output pin 20.
EBI_A21	PB5	PB5	PB5					External Bus Interface (EBI) address output pin 21.
EBI_A22	PB6	PB6	PB6					External Bus Interface (EBI) address output pin 22.
EBI_A23	PC0	PC0	PC0					External Bus Interface (EBI) address output pin 23.
EBI_A24	PC1	PC1	PC1					External Bus Interface (EBI) address output pin 24.
EBI_A25	PC2	PC2	PC2					External Bus Interface (EBI) address output pin 25.
EBI_A26	PC4	PC4	PC4					External Bus Interface (EBI) address output pin 26.
EBI_A27	PD2	PD2	PD2					External Bus Interface (EBI) address output pin 27.
EBI_AD00	PE8	PE8	PE8					External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9	PE9	PE9					External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10	PE10	PE10					External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11	PE11	PE11					External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12	PE12	PE12					External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13	PE13	PE13					External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14	PE14	PE14					External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15	PE15	PE15					External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15	PA15	PA15					External Bus Interface (EBI) address and data input / output pin 08.

Updated the EM0 and EM1 current consumption numbers. Updated the the EM1 plots and removed the EM0 plots.

Updated Environmental information.

Updated trademark, disclaimer and contact information.

Other minor corrections.

7.4 Revision 1.20

June 28th, 2013

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

7.5 Revision 1.10

May 6th, 2013

Updated current consumption table and figures in Electrical characteristics section.

Other minor corrections.

7.6 Revision 1.00

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

Other minor corrections.

7.7 Revision 0.95

May 3rd, 2012

Updated EM2/EM3 current consumption at 85°C.

7.8 Revision 0.90

February 27th, 2012

Initial preliminary release.

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List of Figures