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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, Serial Port
Clock Rate	80MHz
Non-Volatile Memory	External
On-Chip RAM	80kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.80V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2185nkstz-320

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REVISION HISTORY

8/06—Rev. 0 to Rev. A

Miscellaneous Format Updates..... Universal

Applied Corrections or Additional Information to:

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting ADSP-218xN series members to fetch two operands in a single cycle, one from program memory and one from data memory. ADSP-218xN series members can fetch an operand from program memory and the next instruction in the same cycle.

In lieu of the address and data bus for external memory connection, ADSP-218xN series members may be configured for 16-bit Internal DMA port (IDMA port) connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSP's on-chip program and data RAM.

An interface to low-cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals ($\overline{BR}$, $\overline{BGH}$, and $\overline{BG}$). One execution mode (Go Mode) allows the ADSP-218xN to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

ADSP-218xN series members can respond to eleven interrupts. There can be up to six external interrupts (one edge-sensitive, two level-sensitive, and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORT), the BDMA port, and the power-down circuitry. There is also a master $\overline{RESET}$ signal. The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation.

Each port can generate an internal programmable serial clock or accept an external serial clock.

ADSP-218xN series members provide up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, eight flags are programmable as inputs or outputs, and three flags are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) decrements every n processor cycle, where n is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

ADSP-218xN series members incorporate two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Following is a brief list of the capabilities of the ADSP-218xN SPORTs. For additional information on Serial Ports, refer to the *ADSP-218x DSP Hardware Reference*.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulsewidths and timings.
- SPORTs support serial data word lengths from 3 bits to 16 bits and provide optional A-law and μ-law companding, according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24 word or 32-word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts ($\overline{IRQ0}$ and $\overline{IRQ1}$) and the FI and FO signals. The internally generated serial clock may still be used in this configuration.

MODES OF OPERATION

The ADSP-218xN series modes of operation appear in Table 2.

Table 2. Modes of Operation

Mode D	Mode C	Mode B	Mode A	Booting Method
X	0	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Full Memory Mode.[1]
X	0	1	0	No automatic boot operations occur. Program execution starts at external memory location 0. Chip is configured in Full Memory Mode. BDMA can still be used, but the processor does not automatically use or wait for these operations.
0	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode. $\overline{\text{IACK}}$ has active pull-down. (Requires additonal hardware.)
0	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until the host writes to internal program memory location 0. Chip is configured in Host Mode. $\overline{\text{IACK}}$ has active pull-down.[1]
1	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode; $\overline{\text{IACK}}$ requires external pull-down. (Requires additonal hardware.)
1	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until the host writes to internal program memory location 0. Chip is configured in Host Mode. $\overline{\text{IACK}}$ requires external pull-down.[1]

[1] Considered as standard operating settings. Using these configurations allows for easier design and better memory management.

Setting Memory Mode

Memory Mode selection for the ADSP-218xN series is made during chip reset through the use of the Mode C pin. This pin is multiplexed with the DSP's PF2 pin, so care must be taken in how the mode selection is made. The two methods for selecting the value of Mode C are active and passive.

Passive Configuration

Passive Configuration involves the use of a pull-up or pull-down resistor connected to the Mode C pin. To minimize power consumption, or if the PF2 pin is to be used as an output in the DSP application, a weak pull-up or pull-down resistance, on the order of 10 kΩ, can be used. This value should be sufficient to pull the pin to the desired level and still allow the pin to operate as a programmable flag output without undue strain on the processor's output driver. For minimum power consumption during power-down, reconfigure PF2 to be an input, as the pull-up or pull-down resistance will hold the pin in a known state, and will not switch.

Active Configuration

Active Configuration involves the use of a three-statable external driver connected to the Mode C pin. A driver's output enable should be connected to the DSP's $\overline{\text{RESET}}$ signal such that it only drives the PF2 pin when $\overline{\text{RESET}}$ is active (low). When $\overline{\text{RESET}}$ is deasserted, the driver should be three-state, thus allowing full use of the PF2 pin as either an input or output. To minimize power consumption during power-down, configure the programmable flag as an output when connected to a three-stated buffer. This ensures that the pin will be held at a constant level, and will not oscillate should the three-state driver's level hover around the logic switching point.

IDMA ACK Configuration

Mode D = 0 and in host mode: $\overline{\text{IACK}}$ is an active, driven signal and cannot be "wire-OR'ed." Mode D = 1 and in host mode: $\overline{\text{IACK}}$ is an open drain and requires an external pull-down, but multiple $\overline{\text{IACK}}$ pins can be "wire-OR'ed" together.

INTERRUPTS

The interrupt controller allows the processor to respond to the eleven possible interrupts and reset with minimum overhead. ADSP-218xN series members provide four dedicated external interrupt input pins: $\overline{\text{IRQ2}}$, $\overline{\text{IRQL0}}$, $\overline{\text{IRQL1}}$, and $\overline{\text{IRQE}}$ (shared with the PF7–4 pins). In addition, SPORT1 may be reconfigured for $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, FI, and FO, for a total of six external interrupts. The ADSP-218xN also supports internal interrupts from the timer, the byte DMA port, the two serial ports, software, and the power-down control circuit. The interrupt levels are internally prioritized and individually maskable (except power-down and reset). The $\overline{\text{IRQ2}}$, $\overline{\text{IRQ0}}$, and $\overline{\text{IRQ1}}$ input pins can be programmed to be either level- or edge-sensitive. $\overline{\text{IRQL0}}$ and $\overline{\text{IRQL1}}$ are level-sensitive and $\overline{\text{IRQE}}$ is edge-sensitive. The priorities and vector addresses of all interrupts are shown in Table 3.

Table 3. Interrupt Priority and Interrupt Vector Addresses

Source Of Interrupt	Interrupt Vector Address (Hex)
Reset (or Power-Up with PUCR = 1)	0x0000 (Highest Priority)
Power-Down (Nonmaskable)	0x002C
$\overline{\text{IRQ2}}$	0x0004
$\overline{\text{IRQL1}}$	0x0008
$\overline{\text{IRQL0}}$	0x000C
SPORT0 Transmit	0x0010
SPORT0 Receive	0x0014
$\overline{\text{IRQE}}$	0x0018
BDMA Interrupt	0x001C
SPORT1 Transmit or $\overline{\text{IRQ1}}$	0x0020
SPORT1 Receive or $\overline{\text{IRQ0}}$	0x0024
Timer	0x0028 (Lowest Priority)

Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially. Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The power-down interrupt is nonmaskable.

ADSP-218xN series members mask all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect serial port autobuffering or DMA transfers.

The interrupt control register, ICNTL, controls interrupt nesting and defines the $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ external interrupts to be either edge- or level-sensitive. The $\overline{\text{IRQE}}$ pin is an external edge-sensitive interrupt and can be forced and cleared. The $\overline{\text{IRQL0}}$ and $\overline{\text{IRQL1}}$ pins are external level sensitive interrupts.

The IFC register is a write-only register used to force and clear interrupts. On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are 12 levels deep to allow interrupt, loop, and subroutine nesting. The following instructions allow global enable or disable servicing of the interrupts (including power-down), regardless of the state of IMASK:

```
ENA INTS;
DIS INTS;
```

Disabling the interrupts does not affect serial port autobuffering or DMA. When the processor is reset, interrupt servicing is enabled.

LOW-POWER OPERATION

ADSP-218xN series members have three low-power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

Power-Down

ADSP-218xN series members have a low-power feature that lets the processor enter a very low-power dormant state through hardware or software control. Following is a brief list of power-down features. Refer to the *ADSP-218x DSP Hardware Reference*, "System Interface" chapter, for detailed information about the power-down feature.

- Quick recovery from power-down. The processor begins executing instructions in as few as 200 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the lowest power rating and 200 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits approximately 4096 CLKIN cycles for the crystal oscillator to start or stabilize), and letting the oscillator run to allow 200 CLKIN cycle start-up.
- Power-down is initiated by either the power-down pin ($\overline{\text{PWD}}$) or the software power-down force bit. Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt also can be used as a nonmaskable, edge-sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{\text{RESET}}$ pin also can be used to terminate power-down.
- Power-down acknowledge pin (PWDACK) indicates when the processor has entered power-down.

Idle

When the ADSP-218xN is in the Idle Mode, the processor waits indefinitely in a low-power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. In Idle mode IDMA, BDMA, and autobuffer cycle steals still occur.

Slow Idle

The IDLE instruction is enhanced on ADSP-218xN series members to let the processor's internal clock signal be slowed, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the IDLE instruction.

The format of the instruction is:

```
IDLE (n);
```

where n = 16, 32, 64, or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals,

such as SCLK, CLKOUT, and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard IDLE instruction.

When the IDLE (n) instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts. The one-cycle response time of the standard idle state is increased by n, the clock divisor. When an enabled interrupt is received, ADSP-218xN series members remain in the idle state for up to a maximum of n processor cycles (n = 16, 32, 64, or 128) before resuming normal operation.

When the IDLE (n) instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of n processor cycles).

SYSTEM INTERFACE

Figure 2 shows typical basic system configurations with the ADSP-218xN series, two serial devices, a byte-wide EPROM, and optional external program and data overlay memories (mode-selectable). Programmable wait state generation allows the processor to connect easily to slow peripheral devices. ADSP-218xN series members also provide four external interrupts and two serial ports or six external interrupts and one serial port. Host Memory Mode allows access to the full external data bus, but limits addressing to a single address bit (A0). Through the use of external hardware, additional system peripherals can be added in this mode to generate and latch address signals.

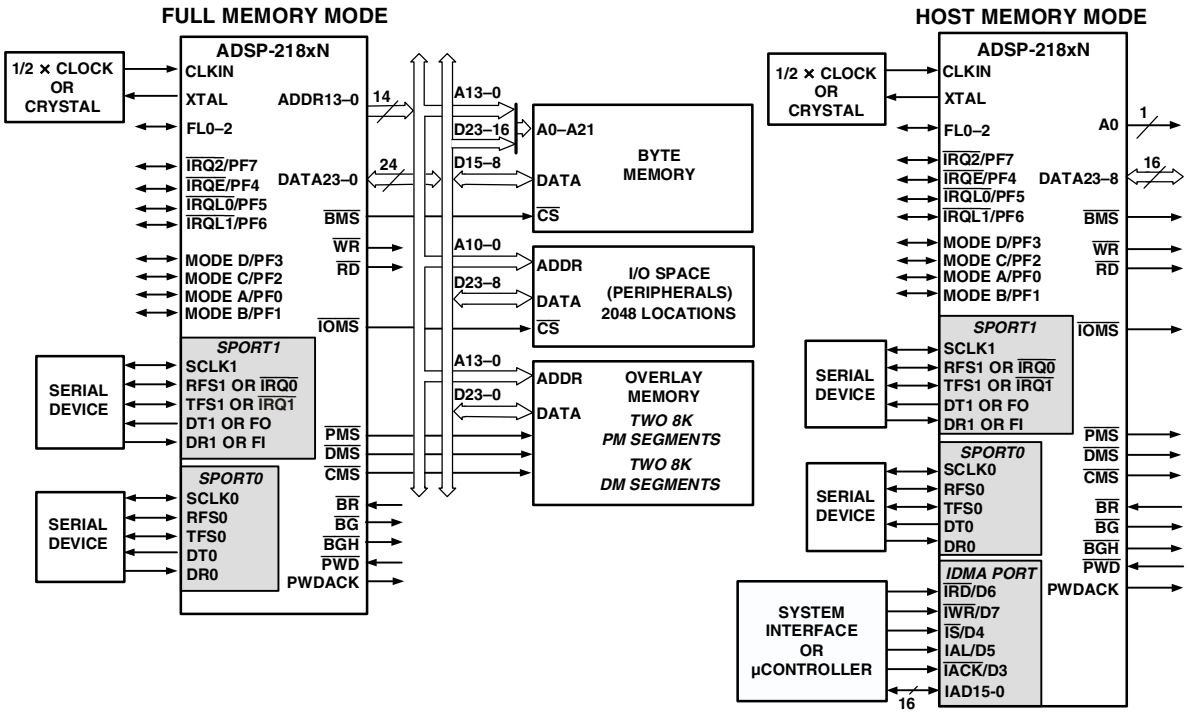

Figure 2. Basic System Interface

PIN DESCRIPTIONS

ADSP-218xN series members are available in a 100-lead LQFP package and a 144-ball BGA package. In order to maintain maximum functionality and reduce package size and pin count, some serial port, programmable flag, interrupt and external bus pins have dual, multiplexed functionality. The external bus pins are configured during $\overline{\text{RESET}}$ only, while serial port pins are software configurable during program execution. Flag and interrupt functionality is retained concurrently on multiplexed pins. In cases where pin functionality is reconfigurable, the default state is shown in plain text in Table 9, while alternate functionality is shown in *italics*.

Table 9. Common-Mode Pins

Pin Name	No. of Pins	I/O	Function
$\overline{\text{RESET}}$	1	I	Processor Reset Input
$\overline{\text{BR}}$	1	I	Bus Request Input
$\overline{\text{BG}}$	1	O	Bus Grant Output
$\overline{\text{BGH}}$	1	O	Bus Grant Hung Output
$\overline{\text{DMS}}$	1	O	Data Memory Select Output
$\overline{\text{PMS}}$	1	O	Program Memory Select Output
$\overline{\text{IOMS}}$	1	O	Memory Select Output
$\overline{\text{BMS}}$	1	O	Byte Memory Select Output
$\overline{\text{CMS}}$	1	O	Combined Memory Select Output
$\overline{\text{RD}}$	1	O	Memory Read Enable Output
$\overline{\text{WR}}$	1	O	Memory Write Enable Output
$\overline{\text{IRQ2}}$	1	I	Edge- or Level-Sensitive Interrupt Request[1]
PF7		I/O	Programmable I/O Pin
$\overline{\text{IRQL1}}$	1	I	Level-Sensitive Interrupt Requests[1]
PF6		I/O	Programmable I/O Pin
$\overline{\text{IRQL0}}$	1	I	Level-Sensitive Interrupt Requests[1]
PF5		I/O	Programmable I/O Pin
$\overline{\text{IRQE}}$	1	I	Edge-Sensitive Interrupt Requests[1]
PF4		I/O	Programmable I/O Pin
Mode D	1	I	Mode Select Input—Checked Only During $\overline{\text{RESET}}$
PF3		I/O	Programmable I/O Pin During Normal Operation
Mode C	1	I	Mode Select Input—Checked Only During $\overline{\text{RESET}}$
PF2		I/O	Programmable I/O Pin During Normal Operation
Mode B	1	I	Mode Select Input—Checked Only During $\overline{\text{RESET}}$
PF1		I/O	Programmable I/O Pin During Normal Operation
Mode A	1	I	Mode Select Input—Checked Only During $\overline{\text{RESET}}$
PF0		I/O	Programmable I/O Pin During Normal Operation
CLKIN	1	I	Clock Input
XTAL	1	O	Quartz Crystal Output
CLKOUT	1	O	Processor Clock Output
SPORT0	5	I/O	Serial Port I/O Pins
SPORT1	5	I/O	Serial Port I/O Pins
$\overline{\text{IRQ1–0}}$, FI, FO			Edge- or Level-Sensitive Interrupts, FI, FO[2]
$\overline{\text{PWD}}$	1	I	Power-Down Control Input
PWDACK	1	O	Power-Down Acknowledge Control Output
FL0, FL1, FL2	3	O	Output Flags
V_{DDINT}	2	I	Internal V_{DD} (1.8 V) Power (LQFP)
V_{DDEXT}	4	I	External V_{DD} (1.8 V, 2.5 V, or 3.3 V) Power (LQFP)
GND	10	I	Ground (LQFP)

Table 9. Common-Mode Pins (Continued)

Pin Name	No. of Pins	I/O	Function
V_{DDINT}	4	I	Internal V_{DD} (1.8 V) Power (BGA)
V_{DDEXT}	7	I	External V_{DD} (1.8 V, 2.5 V, or 3.3 V) Power (BGA)
GND	20	I	Ground (BGA)
EZ-Port	9	I/O	For Emulation Use

[1] Interrupt/Flag pins retain both functions concurrently. If IMASK is set to enable the corresponding interrupts, the DSP will vector to the appropriate interrupt vector address when the pin is asserted, either by external devices or set as a programmable flag.
[2] SPORT configuration determined by the DSP System Control Register. Software configurable.

MEMORY INTERFACE PINS

ADSP-218xN series members can be used in one of two modes: Full Memory Mode, which allows BDMA operation with full external overlay memory and I/O capability, or Host Mode, which allows IDMA operation with limited external addressing capabilities.

The operating mode is determined by the state of the Mode C pin during $\overline{\text{RESET}}$ and cannot be changed while the processor is running. Table 10 and Table 11 list the active signals at specific pins of the DSP during either of the two operating modes (Full Memory or Host). A signal in one table shares a pin with a signal from the other table, with the active signal determined by the mode that is set. For the shared pins and their alternate signals (e.g., A4/IAD3), refer to the package pinouts in Table 27 on Page 41 and Table 28 on Page 43.

Table 10. Full Memory Mode Pins (Mode C = 0)

Pin Name	No. of Pins	I/O	Function
A13–0	14	O	Address Output Pins for Program, Data, Byte, and I/O Spaces
D23–0	24	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces (8 MSBs are also used as Byte Memory Addresses.)

Table 11. Host Mode Pins (Mode C = 1)

Pin Name	No. of Pins	I/O	Function
IAD15–0	16	I/O	IDMA Port Address/Data Bus
A0	1	O	Address Pin for External I/O, Program, Data, or Byte Access[1]
D23–8	16	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces
$\overline{\text{IWR}}$	1	I	IDMA Write Enable
$\overline{\text{IRD}}$	1	I	IDMA Read Enable
IAL	1	I	IDMA Address Latch Pin
$\overline{\text{IS}}$	1	I	IDMA Select
$\overline{\text{IACK}}$	1	O	IDMA Port Acknowledge Configurable in Mode D; Open Drain

[1] In Host Mode, external peripheral addresses can be decoded using the A0, $\overline{\text{CMS}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, and $\overline{\text{IOMS}}$ signals.

TERMINATING UNUSED PINS

Table 12 shows the recommendations for terminating unused pins.

Table 12. Unused Pin Terminations

Pin Name[1]	I/O 3-State (Z)[2]	Reset State	Hi-Z[3] Caused By	Unused Configuration
XTAL	O	O		Float
CLKOUT	O	O		Float[4]
A13–1 or	O (Z)	Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
IAD12–0	I/O (Z)	Hi-Z	$\overline{\text{IS}}$	Float
A0	O (Z)	Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float

Table 12. Unused Pin Terminations (Continued)

Pin Name[1]	I/O 3-State (Z)[2]	Reset State	Hi-Z[3] Caused By	Unused Configuration
D23–8	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
D7 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IWR}$	I	I		High (Inactive)
D6 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IRD}$	I	I	$\overline{BR}$, $\overline{EBR}$	High (Inactive)
D5 or	I/O (Z)	Hi-Z		Float
IAL	I	I		Low (Inactive)
D4 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IS}$	I	I		High (Inactive)
D3 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IACK}$				Float
D2–0 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
IAD15–13	I/O (Z)	Hi-Z	$\overline{IS}$	Float
$\overline{PMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{DMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IOMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{CMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{RD}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{WR}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BR}$	I	I		High (Inactive)
$\overline{BG}$	O (Z)	O	EE	Float
$\overline{BGH}$	O	O		Float
$\overline{IRQ2}$/*PF7*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float[5]
$\overline{IRQL1}$/*PF6*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float[5]
$\overline{IRQL0}$/*PF5*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float[5]
$\overline{IRQE}$/*PF4*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float[5]
$\overline{PWD}$	I	I		High
SCLK0	I/O	I		Input = High or Low, Output = Float
RFS0	I/O	I		High or Low
DR0	I	I		High or Low
TFS0	I/O	I		High or Low
DT0	O	O		Float
SCLK1	I/O	I		Input = High or Low, Output = Float
RFS1/$\overline{IRQ0}$	I/O	I		High or Low
DR1/FI	I	I		High or Low
TFS1/$\overline{IRQ1}$	I/O	I		High or Low
DT1/FO	O	O		Float
EE	I	I		Float
$\overline{EBR}$	I	I		Float
$\overline{EBG}$	O	O		Float

TIMING SPECIFICATIONS

This section contains timing information for the DSP's external signals.

General Notes

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, parameters cannot be added up meaningfully to derive longer times.

Timing Notes

Switching characteristics specify how the processor changes its signals. Designers have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell what the processor will do in a given circumstance. Switching characteristics can also be used to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Frequency Dependency For Timing Specifications

t_{CK} is defined as 0.5 t_{CKI}. The ADSP-218xN uses an input clock with a frequency equal to half the instruction rate. For example, a 40 MHz input clock (which is equivalent to 25 ns) yields a 12.5 ns processor cycle (equivalent to 80 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain the specification value.

Example: t_{CKH} = 0.5 t_{CK} – 2 ns = 0.5 (12.5 ns) – 2 ns = 4.25 ns

Output Drive Currents

Figure 21 shows typical I-V characteristics for the output drivers on the ADSP-218xN series.The curves represent the current drive capability of the output drivers as a function of output voltage.

Figure 23 shows the typical power-down supply current.

Capacitive Loading

Figure 24 and Figure 25 show the capacitive loading characteristics of the ADSP-218xN.

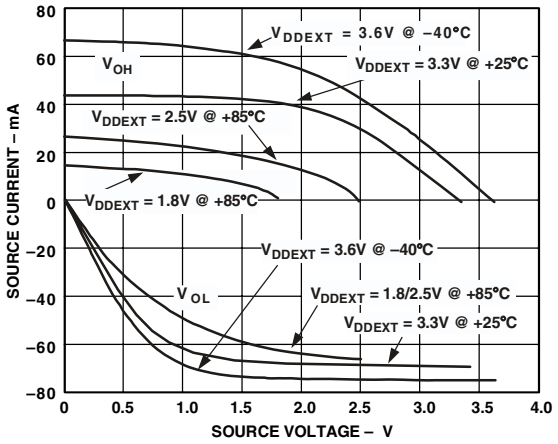

Figure 21. Typical Output Driver Characteristics for V_{DDEXT} at 3.6 V, 3.3 V, 2.5 V, and 1.8 V

Clock Signals and Reset

Table 15. Clock Signals and Reset

Parameter		Min	Max	Unit
Timing Requirements:				
t_{CKI}	CLKIN Period	25	40	ns
t_{CKIL}	CLKIN Width Low	8		ns
t_{CKIH}	CLKIN Width High	8		ns
Switching Characteristics:				
t_{CKL}	CLKOUT Width Low	$0.5t_{CK} - 3$		ns
t_{CKH}	CLKOUT Width High	$0.5t_{CK} - 3$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	8	ns
Control Signals Timing Requirements:				
t_{RSP}	$\overline{\text{RESET}}$ Width Low	$5t_{CK}$[1]		ns
t_{MS}	Mode Setup before $\overline{\text{RESET}}$ High	7		ns
t_{MH}	Mode Hold after $\overline{\text{RESET}}$ High	5		ns

[1] Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles, assuming stable CLKIN (not including crystal oscillator start-up time).

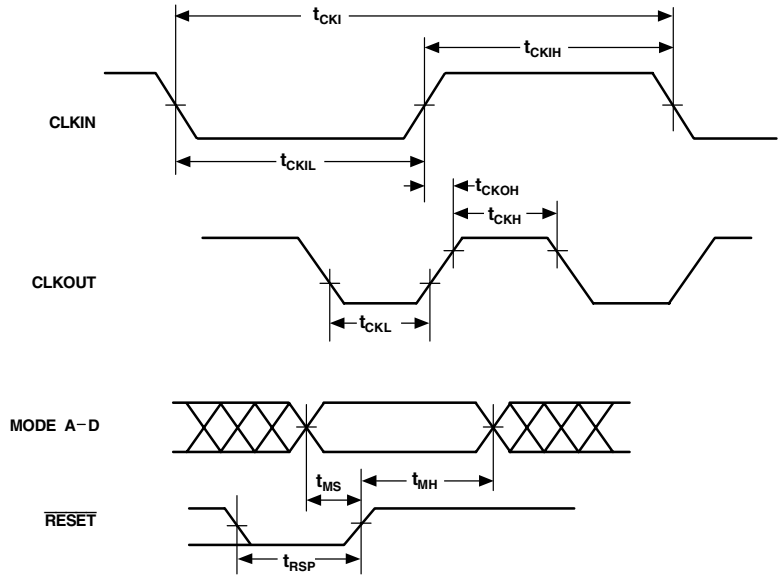

Figure 26. Clock Signals and Reset

Bus Request–Bus Grant

Table 17. Bus Request–Bus Grant

Parameter		Min	Max	Unit
Timing Requirements:				
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	$0.25t_{CK} + 2$		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	$0.25t_{CK} + 8$		ns
Switching Characteristics:				
t_{SD}	CLKOUT High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable[2]		$0.25t_{CK} + 8$	ns
t_{SDB}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE}	$\overline{BG}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	$0.25t_{CK} - 3$		ns
t_{SDBH}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BGH}$ Low[3]	0		ns
t_{SEH}	$\overline{BGH}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable[3]	0		ns

[1] $\overline{BR}$ is an asynchronous signal. If $\overline{BR}$ meets the setup/hold requirements, it will be recognized during the current clock cycle; otherwise the signal will be recognized on the following cycle. Refer to the *ADSP-2100 Family User's Manual* for $\overline{BR}$/BG cycle relationships.

[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

[3] $\overline{BGH}$ is asserted when the bus is granted and the processor or BDMA requires control of the bus to continue.

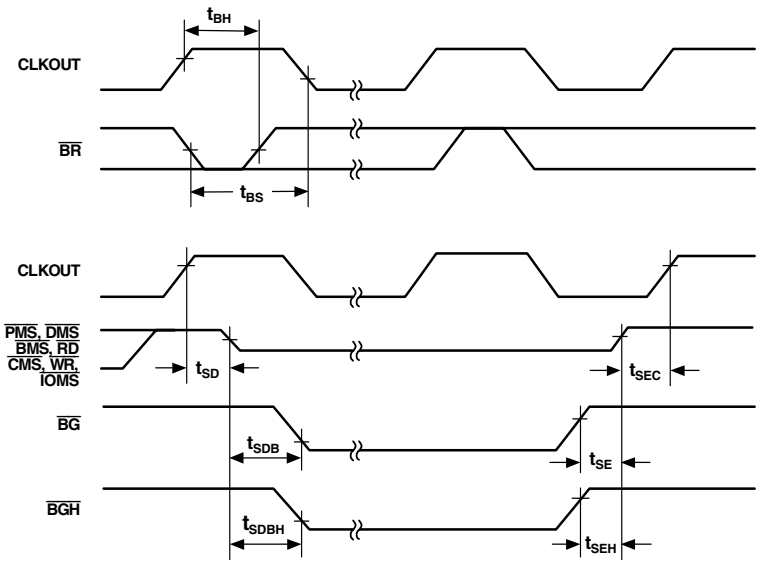

Figure 28. Bus Request–Bus Grant

Memory Read

Table 18. Memory Read

Parameter		Min	Max	Unit
Timing Requirements:				
t_{RDD}	$\overline{RD}$ Low to Data Valid[1]		$0.5t_{CK} - 5 + w$	ns
t_{AA}	A13–0, $\overline{xMS}$ to Data Valid[2]		$0.75t_{CK} - 6 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristics:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 3 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 2$	$0.25t_{CK} + 4$	ns
t_{ASR}	A13–0, $\overline{xMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 3$		ns
t_{RDA}	A13–0, $\overline{xMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 3$		ns

[1] w = wait states 3 t_{CK}.
[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

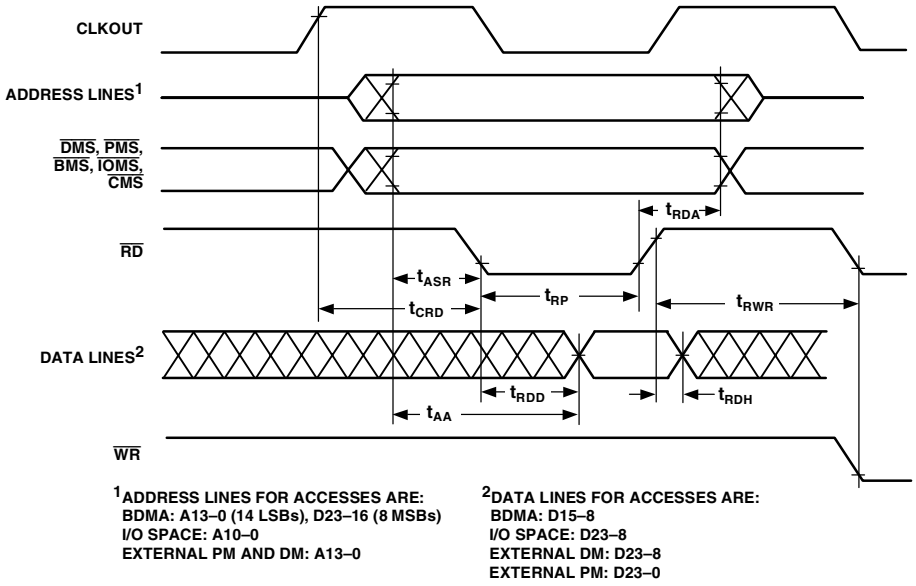

Figure 29. Memory Read

Memory Write

Table 19. Memory Write

Parameter		Min	Max	Unit
Switching Characteristics:				
t_{DW}	Data Setup before $\overline{WR}$ High[1]	$0.5t_{CK}$– 4 + w		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK}$ – 1		ns
t_{WP}	$\overline{WR}$ Pulse Width	$0.5t_{CK}$ – 3 + w		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A13–0, $\overline{xMS}$ Setup before $\overline{WR}$ Low[2]	$0.25t_{CK}$ – 3		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK}$ – 3		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK}$ – 2	$0.25t_{CK}$ + 4	ns
t_{AW}	A13–0, $\overline{xMS}$ Setup before $\overline{WR}$ Deasserted	$0.75t_{CK}$ – 5 + w		ns
t_{WRA}	A13–0, $\overline{xMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK}$ – 1		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK}$ – 3		ns

[1] w = wait states 3 t_{CK}.
[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

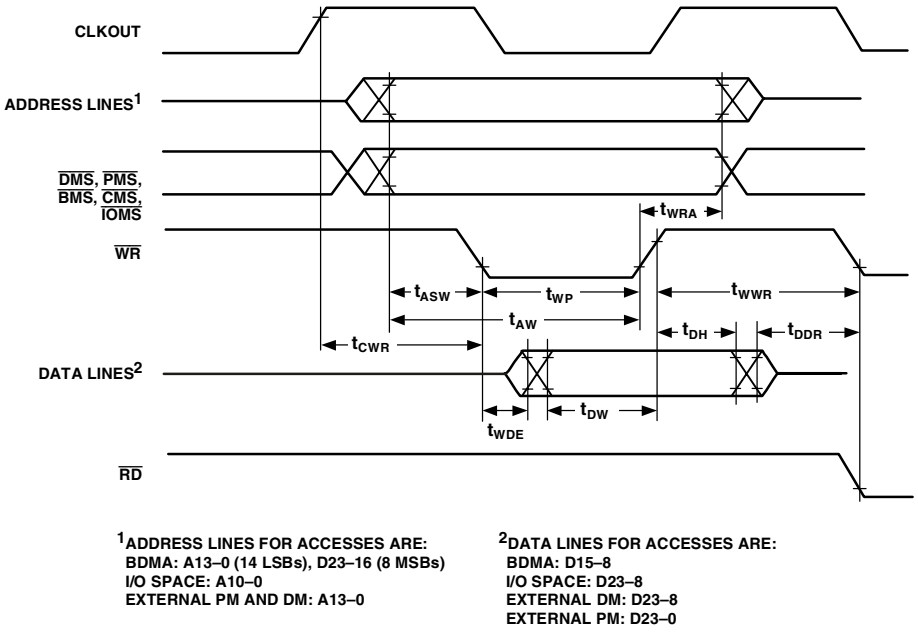

Figure 30. Memory Write

IDMA Read, Long Read Cycle

Table 24. IDMA Read, Long Read Cycle

Parameter		Min	Max	Unit
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low Before Start of Read[1]	0		ns
t_{IRK}	End of read After $\overline{IACK}$ Low[2]	2		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High After Start of Read[1]		10	ns
t_{IKDS}	IAD15–0 Data Setup Before $\overline{IACK}$ Low	$0.5t_{CK} - 3$		ns
t_{IKDH}	IAD15–0 Data Hold After End of Read[2]	0		ns
t_{IKDD}	IAD15–0 Data Disabled After End of Read[2]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled After Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid After Start of Read		11	ns
t_{IRDH1}	IAD15–0 Previous Data Hold After Start of Read (DM/PM1)[3]	$2t_{CK} - 5$		ns
t_{IRDH2}	IAD15–0 Previous Data Hold After Start of Read (PM2)[4]	$t_{CK} - 5$		ns

[1] Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[2] End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.
[3] DM read or first half of PM read.
[4] Second half of PM read.

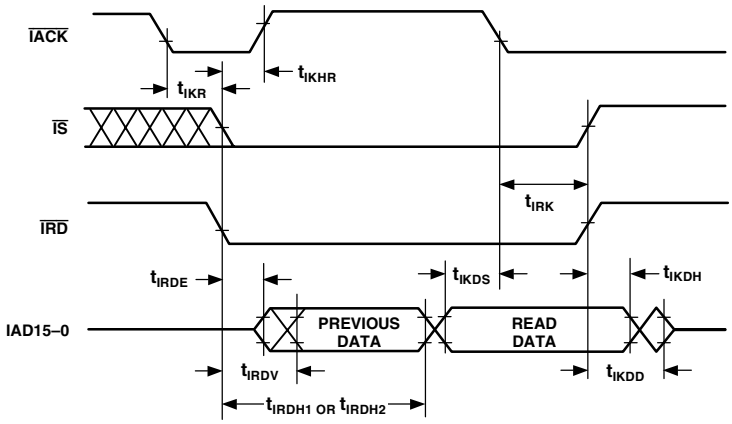

Figure 35. IDMA Read, Long Read Cycle

IDMA Read, Short Read Cycle in Short Read Only Mode

Table 26. IDMA Read, Short Read Cycle in Short Read Only Mode

Parameter[1]		Min	Max	Unit
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low Before Start of Read[2]	0		ns
t_{IRP}	Duration of Read[3]	10		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High After Start of Read[2]		10	ns
t_{IKDH}	IAD15–0 Previous Data Hold After End of Read[3]	0		ns
t_{IKDD}	IAD15–0 Previous Data Disabled After End of Read[3]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled After Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid After Start of Read		10	ns

[1] Short Read Only is enabled by setting Bit 14 of the IDMA overlay Register to 1 (0x3FE7). Short Read Only can be enabled by the processor core writing to the register or by an external host writing to the register. Disabled by default.
[2] Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low. Previous data remains until end of read.
[3] End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

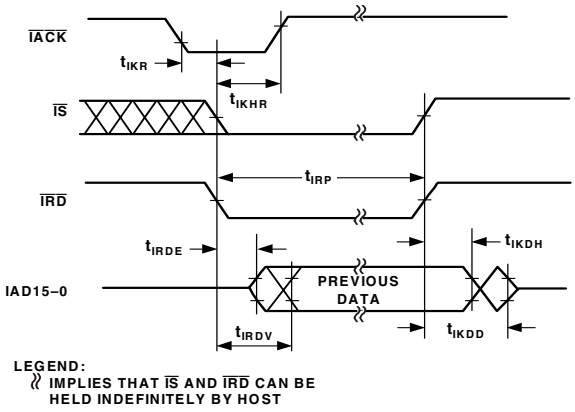

Figure 37. IDMA Read, Short Read Cycle in Short Read Only Mode

LQFP PACKAGE PINOUT

The LQFP package pinout is shown Figure 38 and in Table 27. Pin names in bold text in the table replace the plain-text-named functions when Mode C = 1. A + sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$. The multiplexed pins DT1/FO, TFS1/$\overline{\text{IRQ1}}$, RFS1/$\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default, upon reset.

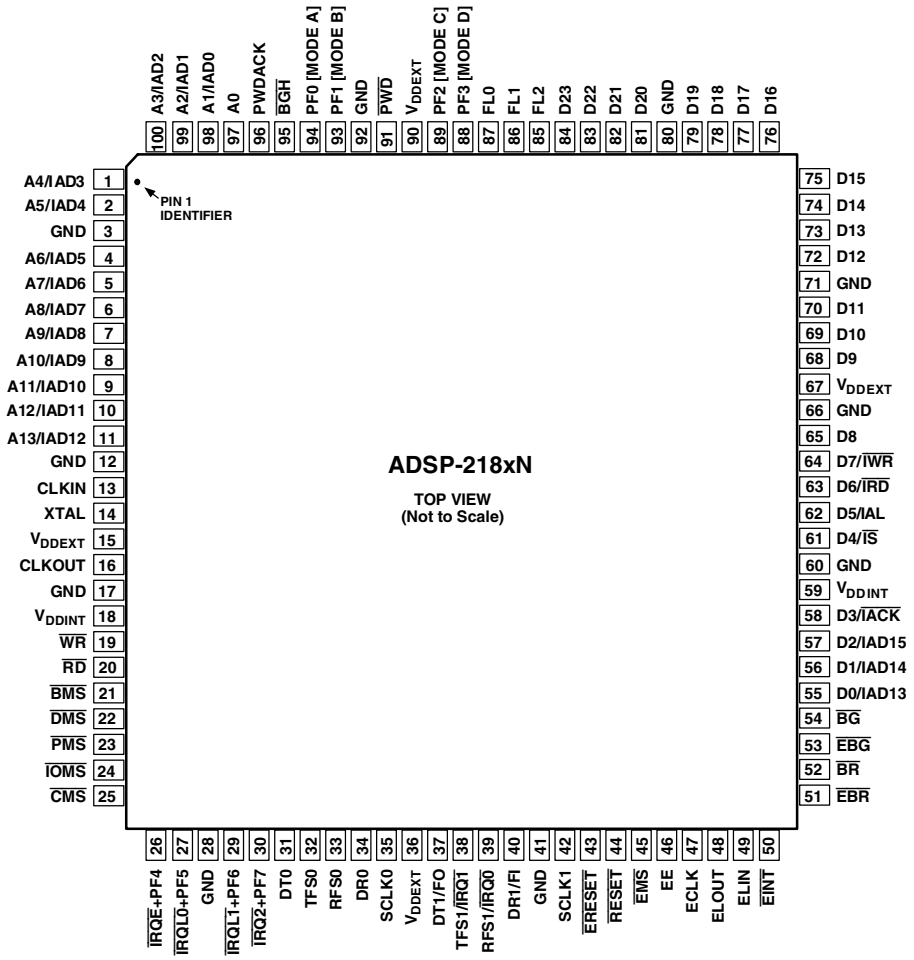

Figure 38. 100-Lead LQFP Pin Configuration

Table 27. LQFP Package Pinout

Pin No.	Pin Name
1	A4/**IAD3**
2	A5/**IAD4**
3	GND
4	A6/**IAD5**
5	A7/**IAD6**
6	A8/**IAD7**
7	A9/**IAD8**
8	A10/**IAD9**
9	A11/**IAD10**
10	A12/**IAD11**
11	A13/**IAD12**
12	GND
13	CLKIN
14	XTAL
15	V_{DDEXT}
16	CLKOUT
17	GND
18	V_{DDINT}
19	$\overline{WR}$
20	$\overline{RD}$
21	$\overline{BMS}$
22	$\overline{DMS}$
23	$\overline{PMS}$
24	$\overline{IOMS}$
25	$\overline{CMS}$
26	$\overline{IRQE}$ + PF4
27	$\overline{IRQL0}$ + PF5
28	GND
29	$\overline{IRQL1}$ + PF6
30	$\overline{IRQ2}$ + PF7
31	DT0
32	TFS0
33	RFS0
34	DR0
35	SCLK0
36	V_{DDEXT}
37	DT1/FO
38	TFS1/$\overline{IRQ1}$
39	RFS1/$\overline{IRQ0}$
40	DR1/FI
41	GND
42	SCLK1
43	$\overline{ERESET}$
44	$\overline{RESET}$
45	$\overline{EMS}$
46	EE
47	ECLK
48	ELOUT
49	ELIN
50	$\overline{EINT}$

Table 27. LQFP Package Pinout (Continued)

Pin No.	Pin Name
51	$\overline{EBR}$
52	$\overline{BR}$
53	$\overline{EBG}$
54	$\overline{BG}$
55	D0/**IAD13**
56	D1/**IAD14**
57	D2/**IAD15**
58	D3/$\overline{\textbf{IACK}}$
59	V_{DDINT}
60	GND
61	D4/$\overline{\textbf{IS}}$
62	D5/**IAL**
63	D6/$\overline{\textbf{IRD}}$
64	D7/$\overline{\textbf{IWR}}$
65	D8
66	GND
67	V_{DDEXT}
68	D9
69	D10
70	D11
71	GND
72	D12
73	D13
74	D14
75	D15
76	D16
77	D17
78	D18
79	D19
80	GND
81	D20
82	D21
83	D22
84	D23
85	FL2
86	FL1
87	FL0
88	PF3 [Mode D]
89	PF2 [Mode C]
90	V_{DDEXT}
91	$\overline{PWD}$
92	GND
93	PF1 [Mode B]
94	PF0 [Mode A]
95	$\overline{BGH}$
96	PWDACK
97	A0
98	A1/**IAD0**
99	A2/**IAD1**
100	A3/**IAD2**

BGA PACKAGE PINOUT

The BGA package pinout is shown in Figure 39 and in Table 28. Pin names in bold text in the table replace the plain text named functions when Mode C = 1. A + sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$. The multiplexed pins DT1/FO, TFS1/$\overline{\text{IRQ1}}$, RFS1/$\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default upon reset.

12	11	10	9	8	7	6	5	4	3	2	1	
GND	GND	D22	NC	NC	NC	GND	NC	A0	GND	A1/IAD0	A2/IAD1	A
D16	D17	D18	D20	D23	V_{DDEXT}	GND	NC	NC	GND	A3/IAD2	A4/IAD3	B
D14	NC	D15	D19	D21	V_{DDEXT}	$\overline{\text{PWD}}$	A7/IAD6	A5/IAD4	$\overline{\text{RD}}$	A6/IAD5	PWDACK	C
GND	NC	D12	D13	NC	PF2 [MODE C]	PF1 [MODE B]	A9/IAD8	$\overline{\text{BGH}}$	NC	$\overline{\text{WR}}$	NC	D
D10	GND	V_{DDEXT}	GND	GND	PF3 [MODE D]	FL2	PF0 [MODE A]	FL0	A8/IAD7	V_{DDEXT}	V_{DDEXT}	E
D9	NC	D8	D11	D7/$\overline{\text{IWR}}$	NC	NC	FL1	A11/IAD10	A12/IAD11	NC	A13/IAD12	F
D4/$\overline{\text{IS}}$	NC	NC	D5/IAL	D6/$\overline{\text{IRD}}$	NC	NC	NC	A10/IAD9	GND	NC	XTAL	G
GND	NC	GND	D3/$\overline{\text{IACK}}$	D2/IAD15	TFS0	DT0	V_{DDINT}	GND	GND	GND	CLKIN	H
V_{DDINT}	V_{DDINT}	D1/IAD14	$\overline{\text{BG}}$	RFS1/$\overline{\text{IRQ0}}$	D0/IAD13	SCLK0	V_{DDEXT}	V_{DDEXT}	NC	V_{DDINT}	CLKOUT	J
$\overline{\text{EBG}}$	$\overline{\text{BR}}$	$\overline{\text{EBR}}$	$\overline{\text{ERESET}}$	SCLK1	TFS1/$\overline{\text{IRQ1}}$	RFS0	$\overline{\text{DMS}}$	$\overline{\text{BMS}}$	NC	NC	NC	K
$\overline{\text{EINT}}$	ELOUT	ELIN	$\overline{\text{RESET}}$	GND	DR0	$\overline{\text{PMS}}$	GND	$\overline{\text{IOMS}}$	$\overline{\text{IRQL1}}$ + PF6	NC	$\overline{\text{IRQE}}$ + PF4	L
ECLK	EE	$\overline{\text{EMS}}$	NC	GND	DR1/FI	DT1/FO	GND	$\overline{\text{CMS}}$	NC	$\overline{\text{IRQ2}}$ + PF7	$\overline{\text{IRQL0}}$ + PF5	M

Figure 39. 144-Ball BGA Package Pinout (Bottom View)

OUTLINE DIMENSIONS

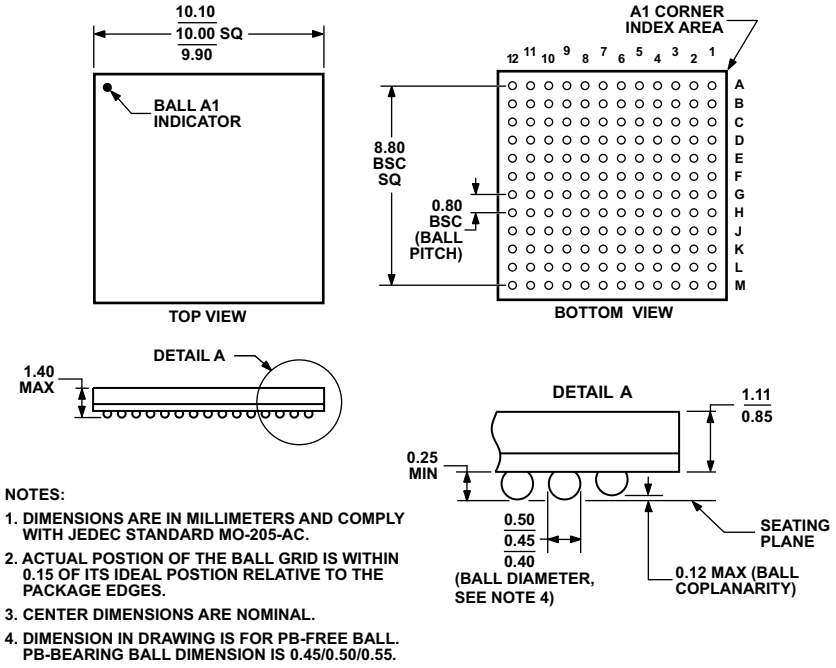

Figure 40. 144-Ball BGA [CSP_BGA] (BC-144-6)

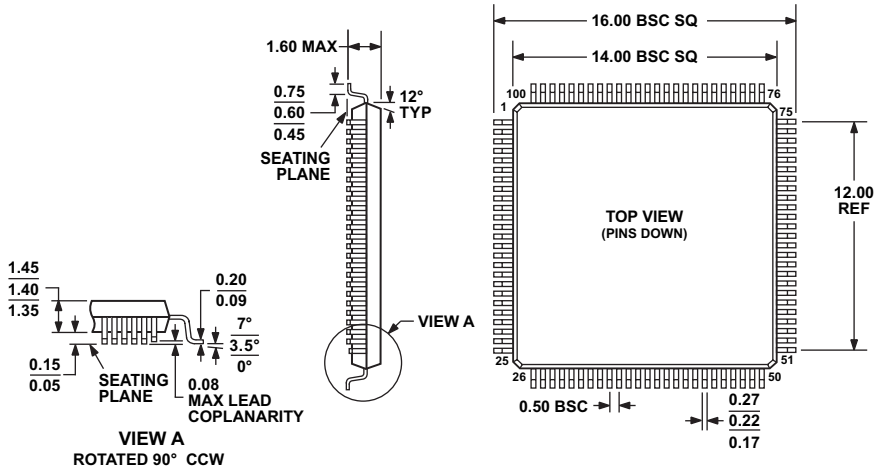

Figure 41. 100-Lead Low Profile Quad Flat Package [LQFP] (ST-100-1)

SURFACE MOUNT DESIGN

Table 29 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard*.

Table 29. BGA Data for Use with Surface Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
144-Ball BGA (BC-144-6)	Solder Mask Defined	0.40 mm diameter	0.50 mm diameter