Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, Serial Port
Clock Rate	80MHz
Non-Volatile Memory	External
On-Chip RAM	40kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.90V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2186nbstz-320

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting ADSP-218xN series members to fetch two operands in a single cycle, one from program memory and one from data memory. ADSP-218xN series members can fetch an operand from program memory and the next instruction in the same cycle.

In lieu of the address and data bus for external memory connection, ADSP-218xN series members may be configured for 16-bit Internal DMA port (IDMA port) connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSP's on-chip program and data RAM.

An interface to low-cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals ($\overline{BR}$, $\overline{BGH}$, and $\overline{BG}$). One execution mode (Go Mode) allows the ADSP-218xN to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

ADSP-218xN series members can respond to eleven interrupts. There can be up to six external interrupts (one edge-sensitive, two level-sensitive, and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORT), the BDMA port, and the power-down circuitry. There is also a master $\overline{RESET}$ signal. The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation.

Each port can generate an internal programmable serial clock or accept an external serial clock.

ADSP-218xN series members provide up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, eight flags are programmable as inputs or outputs, and three flags are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) decrements every n processor cycle, where n is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

ADSP-218xN series members incorporate two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Following is a brief list of the capabilities of the ADSP-218xN SPORTs. For additional information on Serial Ports, refer to the *ADSP-218x DSP Hardware Reference*.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulsewidths and timings.
- SPORTs support serial data word lengths from 3 bits to 16 bits and provide optional A-law and μ-law companding, according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24 word or 32-word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts ($\overline{IRQ0}$ and $\overline{IRQ1}$) and the FI and FO signals. The internally generated serial clock may still be used in this configuration.

Table 3. Interrupt Priority and Interrupt Vector Addresses

Source Of Interrupt	Interrupt Vector Address (Hex)
Reset (or Power-Up with PUCR = 1)	0x0000 (Highest Priority)
Power-Down (Nonmaskable)	0x002C
$\overline{\text{IRQ2}}$	0x0004
$\overline{\text{IRQL1}}$	0x0008
$\overline{\text{IRQL0}}$	0x000C
SPORT0 Transmit	0x0010
SPORT0 Receive	0x0014
$\overline{\text{IRQE}}$	0x0018
BDMA Interrupt	0x001C
SPORT1 Transmit or $\overline{\text{IRQ1}}$	0x0020
SPORT1 Receive or $\overline{\text{IRQ0}}$	0x0024
Timer	0x0028 (Lowest Priority)

Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially. Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The power-down interrupt is nonmaskable.

ADSP-218xN series members mask all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect serial port autobuffering or DMA transfers.

The interrupt control register, ICNTL, controls interrupt nesting and defines the $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ external interrupts to be either edge- or level-sensitive. The $\overline{\text{IRQE}}$ pin is an external edge-sensitive interrupt and can be forced and cleared. The $\overline{\text{IRQL0}}$ and $\overline{\text{IRQL1}}$ pins are external level sensitive interrupts.

The IFC register is a write-only register used to force and clear interrupts. On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are 12 levels deep to allow interrupt, loop, and subroutine nesting. The following instructions allow global enable or disable servicing of the interrupts (including power-down), regardless of the state of IMASK:

```
ENA INTS;
DIS INTS;
```

Disabling the interrupts does not affect serial port autobuffering or DMA. When the processor is reset, interrupt servicing is enabled.

LOW-POWER OPERATION

ADSP-218xN series members have three low-power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

Power-Down

ADSP-218xN series members have a low-power feature that lets the processor enter a very low-power dormant state through hardware or software control. Following is a brief list of power-down features. Refer to the *ADSP-218x DSP Hardware Reference*, "System Interface" chapter, for detailed information about the power-down feature.

- Quick recovery from power-down. The processor begins executing instructions in as few as 200 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the lowest power rating and 200 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits approximately 4096 CLKIN cycles for the crystal oscillator to start or stabilize), and letting the oscillator run to allow 200 CLKIN cycle start-up.
- Power-down is initiated by either the power-down pin ($\overline{\text{PWD}}$) or the software power-down force bit. Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt also can be used as a nonmaskable, edge-sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{\text{RESET}}$ pin also can be used to terminate power-down.
- Power-down acknowledge pin (PWDACK) indicates when the processor has entered power-down.

Idle

When the ADSP-218xN is in the Idle Mode, the processor waits indefinitely in a low-power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. In Idle mode IDMA, BDMA, and autobuffer cycle steals still occur.

Slow Idle

The IDLE instruction is enhanced on ADSP-218xN series members to let the processor's internal clock signal be slowed, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the IDLE instruction.

The format of the instruction is:

```
IDLE (n);
```

where n = 16, 32, 64, or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals,

MEMORY ARCHITECTURE

The ADSP-218xN series provides a variety of memory and peripheral interface options. The key functional groups are Program Memory, Data Memory, Byte Memory, and I/O. Refer to Figure 4 through Figure 9, Table 4 on Page 11, and Table 5 on Page 11 for PM and DM memory allocations in the ADSP-218xN series.

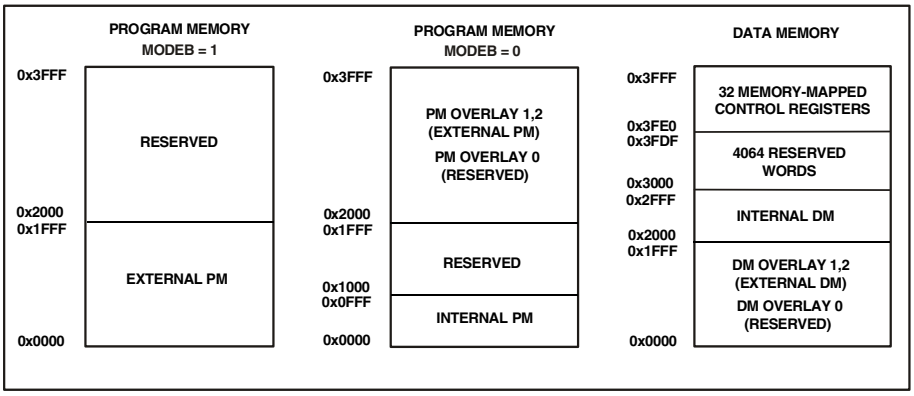

Figure 4. ADSP-2184 Memory Architecture

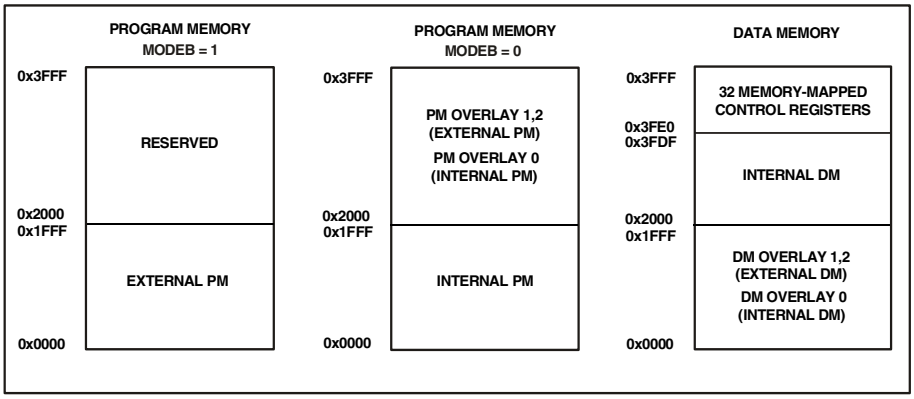

Figure 5. ADSP-2185 Memory Architecture

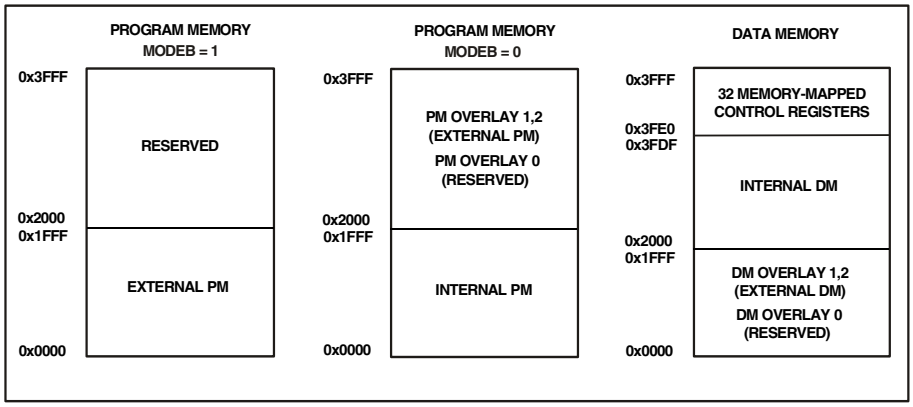

Figure 6. ADSP-2186 Memory Architecture

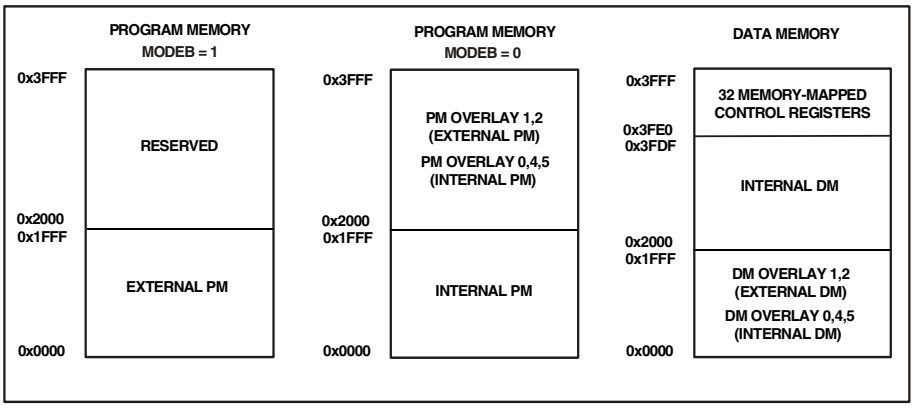

Figure 7. ADSP-2187 Memory Architecture

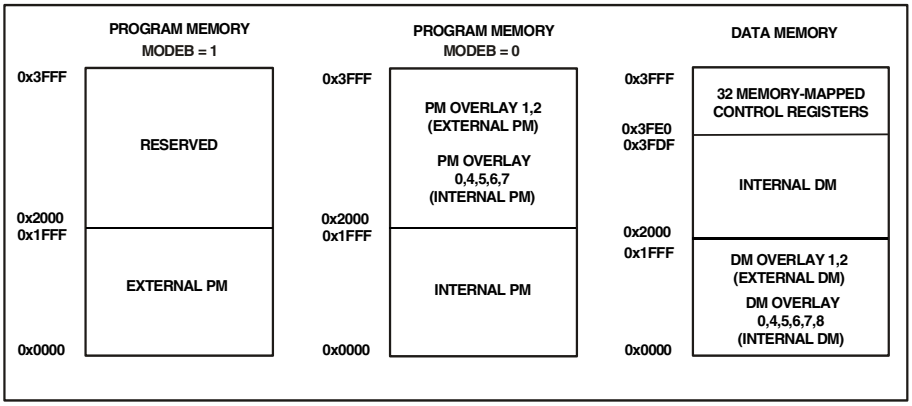

Figure 8. ADSP-2188 Memory Architecture

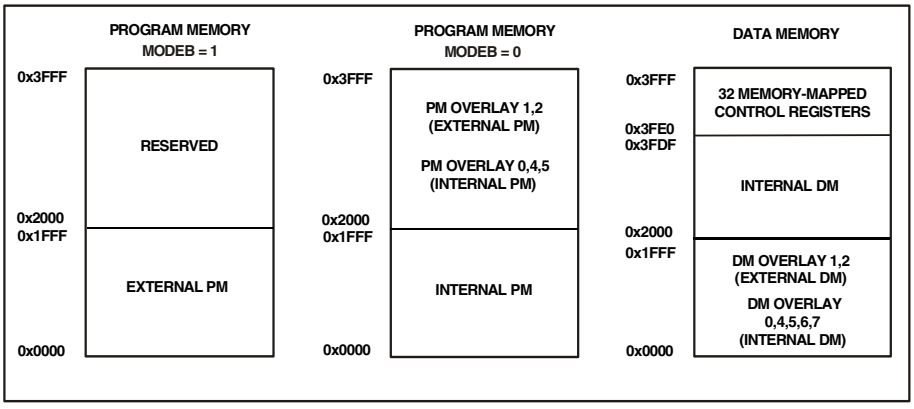

Figure 9. ADSP-2189 Memory Architecture

Program Memory

Program Memory (Full Memory Mode) is a 24-bit-wide space for storing both instruction opcodes and data. The member DSPs of this series have up to 48K words of Program Memory RAM on chip, and the capability of accessing up to two 8K external memory overlay spaces, using the external data bus.

Program Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0). External program execution is not available in host mode due to a restricted data bus that is only 16 bits wide.

Table 4. PMOVLAY Bits

Processor	PMOVLAY	Memory	A13	A12–0
ADSP-2184N	No Internal Overlay Region	Not Applicable	Not Applicable	Not Applicable
ADSP-2185N	0	Internal Overlay	Not Applicable	Not Applicable
ADSP-2186N	No Internal Overlay Region	Not Applicable	Not Applicable	Not Applicable
ADSP-2187N	0, 4, 5	Internal Overlay	Not Applicable	Not Applicable
ADSP-2188N	0, 4, 5, 6, 7	Internal Overlay	Not Applicable	Not Applicable
ADSP-2189N	0, 4, 5	Internal Overlay	Not Applicable	Not Applicable
All Processors	1	External Overlay 1	0	13 LSBs of Address Between 0x2000 and 0x3FFF
All Processors	2	External Overlay 2	1	13 LSBs of Address Between 0x2000 and 0x3FFF

Data Memory

Data Memory (Full Memory Mode) is a 16-bit-wide space used for the storage of data variables and for memory-mapped control registers. The ADSP-218xN series has up to 56K words of Data Memory RAM on-chip. Part of this space is used by 32 memory-mapped registers. Support also exists for up to two 8K external memory overlay spaces through the external data bus.

All internal accesses complete in one cycle. Accesses to external memory are timed using the wait states specified by the DWAIT register and the wait state mode bit.

Data Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0).

Table 5. DMOVLAY Bits

Processor	DMOVLAY	Memory	A13	A12–0
ADSP-2184N	No Internal Overlay Region	Not Applicable	Not Applicable	Not Applicable
ADSP-2185N	0	Internal Overlay	Not Applicable	Not Applicable
ADSP-2186N	No Internal Overlay Region	Not Applicable	Not Applicable	Not Applicable
ADSP-2187N	0, 4, 5	Internal Overlay	Not Applicable	Not Applicable
ADSP-2188N	0, 4, 5, 6, 7, 8	Internal Overlay	Not Applicable	Not Applicable
ADSP-2189N	0, 4, 5, 6, 7	Internal Overlay	Not Applicable	Not Applicable
All Processors	1	External Overlay 1	0	13 LSBs of Address Between 0x0000 and 0x1FFF
All Processors	2	External Overlay 2	1	13 LSBs of Address Between 0x0000 and 0x1FFF

Memory-Mapped Registers (New to the ADSP-218xM and N series)

ADSP-218xN series members have three memory-mapped registers that differ from other ADSP-21xx Family DSPs. The slight modifications to these registers (Wait State Control, Programmable Flag and Composite Select Control, and System Control) provide the ADSP-218xN's wait state and $\overline{\text{BMS}}$ control features. Default bit values at reset are shown; if no value is shown, the bit is undefined at reset. Reserved bits are shown on a grey field. These bits should always be written with zeros.

I/O Space (Full Memory Mode)

ADSP-218xN series members support an additional external memory space called I/O space. This space is designed to support simple connections to peripherals (such as data converters and external registers) or to bus interface ASIC data registers. I/O space supports 2048 locations of 16-bit wide data. The lower eleven bits of the external address bus are used; the upper three bits are undefined.

Two instructions were added to the core ADSP-2100 Family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated three-bit wait state registers,

($\overline{BR}$) signal. If the ADSP-218xN is not performing an external memory access, it responds to the active $\overline{BR}$ input in the following processor cycle by:

- Three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- Asserting the bus grant ($\overline{BG}$) signal, and
- Halting program execution.

If Go Mode is enabled, the ADSP-218xN will not halt program execution until it encounters an instruction that requires an external memory access.

If an ADSP-218xN series member is performing an external memory access when the external device asserts the $\overline{BR}$ signal, it will not three-state the memory interfaces nor assert the $\overline{BG}$ signal until the processor cycle after the access completes. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, re-enables the output drivers, and continues program execution from the point at which it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active.

The $\overline{BGH}$ pin is asserted when an ADSP-218xN series member requires the external bus for a memory or BDMA access, but is stopped. The other device can release the bus by deasserting bus request. Once the bus is released, the ADSP-218xN deasserts $\overline{BG}$ and $\overline{BGH}$ and executes the external memory access.

FLAG I/O PINS

ADSP-218xN series members have eight general-purpose programmable input/output flag pins. They are controlled by two memory-mapped registers. The PFTYPE register determines the direction, 1 = output and 0 = input. The PFDATA register is used to read and write the values on the pins. Data being read from a pin configured as an input is synchronized to the ADSP-218xN's clock. Bits that are programmed as outputs will read the value being output. The PF pins default to input during reset.

In addition to the programmable flags, ADSP-218xN series members have five fixed-mode flags, FI, FO, FL0, FL1, and FL2. FL0 to FL2 are dedicated output flags. FI and FO are available as an alternate configuration of SPORT1.

Note: Pins PF0, PF1, PF2, and PF3 are also used for device configuration during reset.

INSTRUCTION SET DESCRIPTION

The ADSP-218xN series assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 Family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to utilize on-chip memory and conform to the ADSP-218xN's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return, or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction, with up to two fetches or one write to processor memory space, during a single instruction cycle.

DEVELOPMENT SYSTEM

Analog Devices' wide range of software and hardware development tools supports the ADSP-218xN series. The DSP tools include an integrated development environment, an evaluation kit, and a serial port emulator.

VisualDSP++®† is an integrated development environment, allowing for fast and easy development, debug, and deployment. The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy-to-use assembler that is based on an algebraic syntax; an archiver (librarian/library builder); a linker; a PROM-splitter utility; a cycle-accurate, instruction-level simulator; a C compiler; and a C run-time library that includes DSP and mathematical functions.

Debugging both C and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C and assembly code (interleaved source and object information)
- Insert break points
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution

† VisualDSP++ is a registered trademark of Analog Devices, Inc.

Table 9. Common-Mode Pins (Continued)

Pin Name	No. of Pins	I/O	Function
V_{DDINT}	4	I	Internal V_{DD} (1.8 V) Power (BGA)
V_{DDEXT}	7	I	External V_{DD} (1.8 V, 2.5 V, or 3.3 V) Power (BGA)
GND	20	I	Ground (BGA)
EZ-Port	9	I/O	For Emulation Use

[1] Interrupt/Flag pins retain both functions concurrently. If IMASK is set to enable the corresponding interrupts, the DSP will vector to the appropriate interrupt vector address when the pin is asserted, either by external devices or set as a programmable flag.
[2] SPORT configuration determined by the DSP System Control Register. Software configurable.

MEMORY INTERFACE PINS

ADSP-218xN series members can be used in one of two modes: Full Memory Mode, which allows BDMA operation with full external overlay memory and I/O capability, or Host Mode, which allows IDMA operation with limited external addressing capabilities.

The operating mode is determined by the state of the Mode C pin during $\overline{\text{RESET}}$ and cannot be changed while the processor is running. Table 10 and Table 11 list the active signals at specific pins of the DSP during either of the two operating modes (Full Memory or Host). A signal in one table shares a pin with a signal from the other table, with the active signal determined by the mode that is set. For the shared pins and their alternate signals (e.g., A4/IAD3), refer to the package pinouts in Table 27 on Page 41 and Table 28 on Page 43.

Table 10. Full Memory Mode Pins (Mode C = 0)

Pin Name	No. of Pins	I/O	Function
A13–0	14	O	Address Output Pins for Program, Data, Byte, and I/O Spaces
D23–0	24	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces (8 MSBs are also used as Byte Memory Addresses.)

Table 11. Host Mode Pins (Mode C = 1)

Pin Name	No. of Pins	I/O	Function
IAD15–0	16	I/O	IDMA Port Address/Data Bus
A0	1	O	Address Pin for External I/O, Program, Data, or Byte Access[1]
D23–8	16	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces
$\overline{\text{IWR}}$	1	I	IDMA Write Enable
$\overline{\text{IRD}}$	1	I	IDMA Read Enable
IAL	1	I	IDMA Address Latch Pin
$\overline{\text{IS}}$	1	I	IDMA Select
$\overline{\text{IACK}}$	1	O	IDMA Port Acknowledge Configurable in Mode D; Open Drain

[1] In Host Mode, external peripheral addresses can be decoded using the A0, $\overline{\text{CMS}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, and $\overline{\text{IOMS}}$ signals.

TERMINATING UNUSED PINS

Table 12 shows the recommendations for terminating unused pins.

Table 12. Unused Pin Terminations

Pin Name[1]	I/O 3-State (Z)[2]	Reset State	Hi-Z[3] Caused By	Unused Configuration
XTAL	O	O		Float
CLKOUT	O	O		Float[4]
A13–1 or	O (Z)	Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
IAD12–0	I/O (Z)	Hi-Z	$\overline{\text{IS}}$	Float
A0	O (Z)	Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float

Table 12. Unused Pin Terminations (Continued)

Pin Name[1]	I/O 3-State (Z)[2]	Reset State	Hi-Z[3] Caused By	Unused Configuration
D23–8	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
D7 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IWR}$	I	I		High (Inactive)
D6 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IRD}$	I	I	$\overline{BR}$, $\overline{EBR}$	High (Inactive)
D5 or	I/O (Z)	Hi-Z		Float
IAL	I	I		Low (Inactive)
D4 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IS}$	I	I		High (Inactive)
D3 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IACK}$				Float
D2–0 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
IAD15–13	I/O (Z)	Hi-Z	$\overline{IS}$	Float
$\overline{PMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{DMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IOMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{CMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{RD}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{WR}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BR}$	I	I		High (Inactive)
$\overline{BG}$	O (Z)	O	EE	Float
$\overline{BGH}$	O	O		Float
$\overline{IRQ2}$/*PF7*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float[5]
$\overline{IRQL1}$/*PF6*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float[5]
$\overline{IRQL0}$/*PF5*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float[5]
$\overline{IRQE}$/*PF4*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float[5]
$\overline{PWD}$	I	I		High
SCLK0	I/O	I		Input = High or Low, Output = Float
RFS0	I/O	I		High or Low
DR0	I	I		High or Low
TFS0	I/O	I		High or Low
DT0	O	O		Float
SCLK1	I/O	I		Input = High or Low, Output = Float
RFS1/$\overline{IRQ0}$	I/O	I		High or Low
DR1/FI	I	I		High or Low
TFS1/$\overline{IRQ1}$	I/O	I		High or Low
DT1/FO	O	O		Float
EE	I	I		Float
$\overline{EBR}$	I	I		Float
$\overline{EBG}$	O	O		Float

ENVIRONMENTAL CONDITIONS

Table 14. Thermal Resistance

Rating Description[1]	Symbol	LQFP (°C/W)	BGA (°C/W)
Thermal Resistance (Case-to-Ambient)	θ_{CA}	48	63.3
Thermal Resistance (Junction-to-Ambient)	θ_{JA}	50	70.7
Thermal Resistance (Junction-to-Case)	θ_{JC}	2	7.4

[1] Where the Ambient Temperature Rating (T_{AMB}) is:
$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W

TEST CONDITIONS

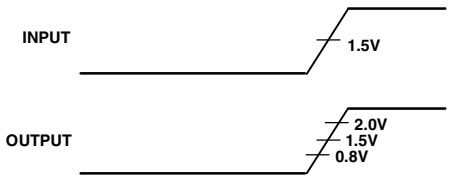

Figure 18. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

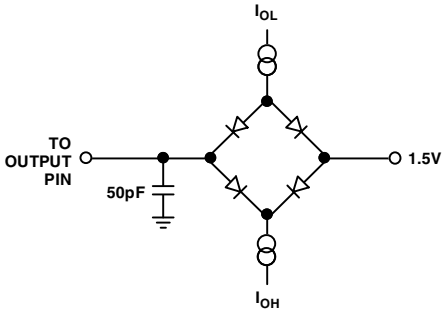

Figure 19. Equivalent Loading for AC Measurements (Including All Fixtures)

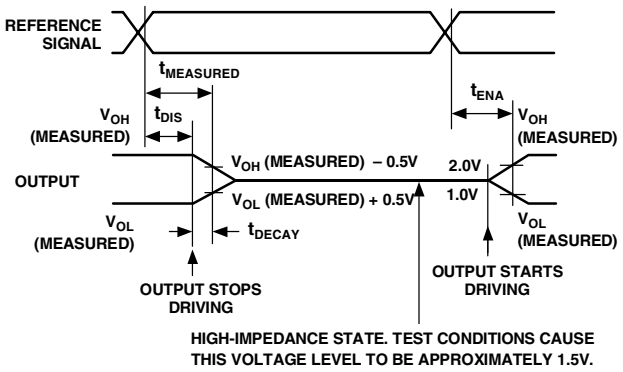

Figure 20. Output Enable/Disable

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 20. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitive load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 20. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

TIMING SPECIFICATIONS

This section contains timing information for the DSP's external signals.

General Notes

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, parameters cannot be added up meaningfully to derive longer times.

Timing Notes

Switching characteristics specify how the processor changes its signals. Designers have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell what the processor will do in a given circumstance. Switching characteristics can also be used to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Frequency Dependency For Timing Specifications

t_{CK} is defined as 0.5 t_{CKI}. The ADSP-218xN uses an input clock with a frequency equal to half the instruction rate. For example, a 40 MHz input clock (which is equivalent to 25 ns) yields a 12.5 ns processor cycle (equivalent to 80 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain the specification value.

Example: t_{CKH} = 0.5 t_{CK} – 2 ns = 0.5 (12.5 ns) – 2 ns = 4.25 ns

Output Drive Currents

Figure 21 shows typical I-V characteristics for the output drivers on the ADSP-218xN series.The curves represent the current drive capability of the output drivers as a function of output voltage.

Figure 23 shows the typical power-down supply current.

Capacitive Loading

Figure 24 and Figure 25 show the capacitive loading characteristics of the ADSP-218xN.

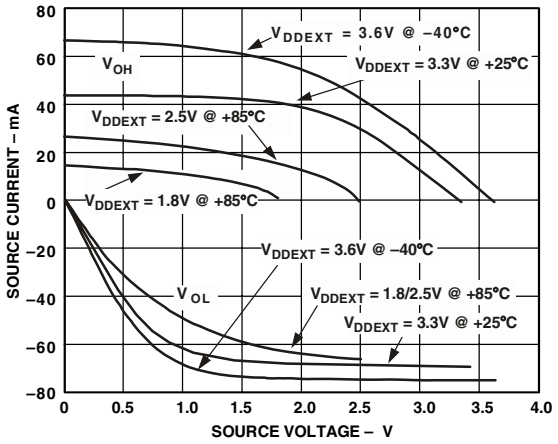

Figure 21. Typical Output Driver Characteristics for V_{DDEXT} at 3.6 V, 3.3 V, 2.5 V, and 1.8 V

Clock Signals and Reset

Table 15. Clock Signals and Reset

Parameter		Min	Max	Unit
Timing Requirements:				
t_{CKI}	CLKIN Period	25	40	ns
t_{CKIL}	CLKIN Width Low	8		ns
t_{CKIH}	CLKIN Width High	8		ns
Switching Characteristics:				
t_{CKL}	CLKOUT Width Low	$0.5t_{CK} - 3$		ns
t_{CKH}	CLKOUT Width High	$0.5t_{CK} - 3$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	8	ns
Control Signals Timing Requirements:				
t_{RSP}	$\overline{\text{RESET}}$ Width Low	$5t_{CK}$[1]		ns
t_{MS}	Mode Setup before $\overline{\text{RESET}}$ High	7		ns
t_{MH}	Mode Hold after $\overline{\text{RESET}}$ High	5		ns

[1] Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles, assuming stable CLKIN (not including crystal oscillator start-up time).

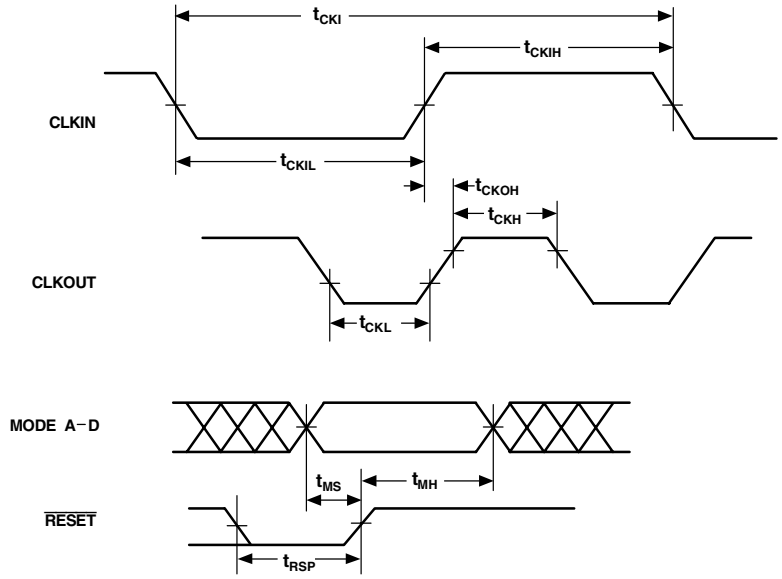

Figure 26. Clock Signals and Reset

Interrupts and Flags

Table 16. Interrupts and Flags

Parameter		Min	Max	Unit
Timing Requirements:				
t_{IFS}	$\overline{IRQx}$, FI, or PFx Setup before CLKOUT Low[1, 2, 3, 4]	$0.25t_{CK} + 10$		ns
t_{IFH}	$\overline{IRQx}$, FI, or PFx Hold after CLKOUT High[1, 2, 3, 4]	$0.25t_{CK}$		ns
Switching Characteristics:				
t_{FOH}	Flag Output Hold after CLKOUT Low[5]	$0.5t_{CK} - 5$		ns
t_{FOD}	Flag Output Delay from CLKOUT Low[5]		$0.5t_{CK} + 4$	ns

[1] If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to "Interrupt Controller Operation" in the *Program Control* chapter of the *ADSP-218x DSP Hardware Reference* for further information on interrupt servicing.)

[2] Edge-sensitive interrupts require pulse widths greater than 10 ns; level-sensitive interrupts must be held low until serviced.

[3] $\overline{IRQx}$ = $\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$, $\overline{IRQLE}$.

[4] PFx = PF0, PF1, PF2, PF3, PF4, PF5, PF6, PF7.

[5] Flag Outputs = PFx, FL0, FL1, FL2, FO.

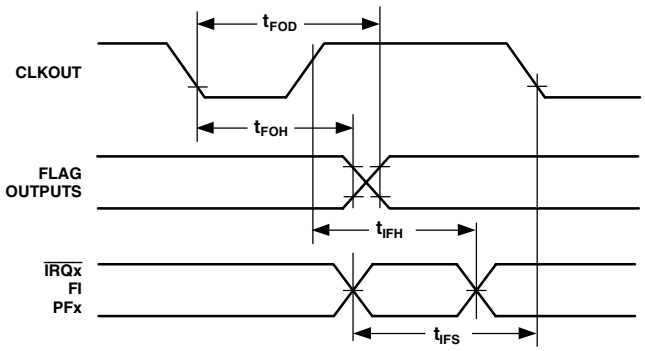

Figure 27. Interrupts and Flags

Memory Read

Table 18. Memory Read

Parameter		Min	Max	Unit
Timing Requirements:				
t_{RDD}	$\overline{RD}$ Low to Data Valid[1]		$0.5t_{CK} - 5 + w$	ns
t_{AA}	A13–0, $\overline{xMS}$ to Data Valid[2]		$0.75t_{CK} - 6 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristics:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 3 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 2$	$0.25t_{CK} + 4$	ns
t_{ASR}	A13–0, $\overline{xMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 3$		ns
t_{RDA}	A13–0, $\overline{xMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 3$		ns

[1] w = wait states 3 t_{CK}.
[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

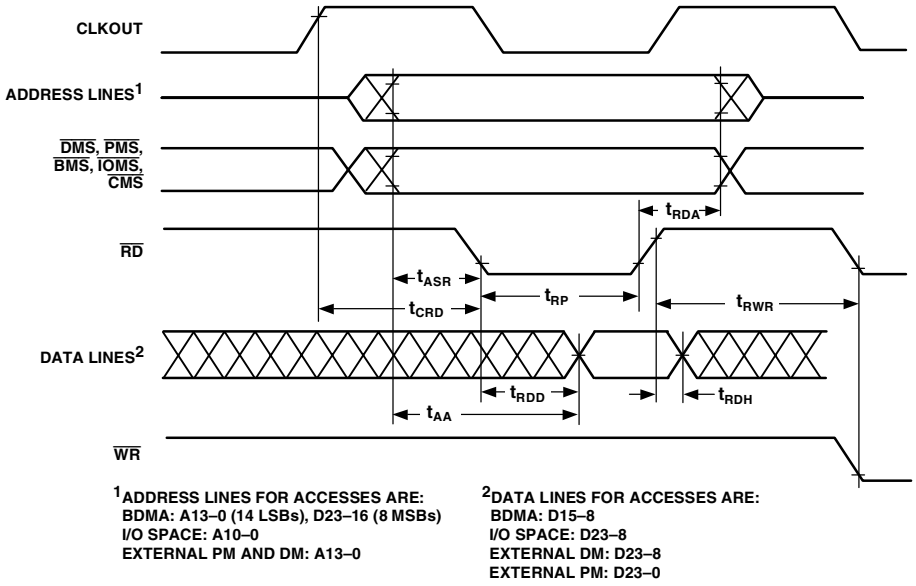

Figure 29. Memory Read

Memory Write

Table 19. Memory Write

Parameter		Min	Max	Unit
Switching Characteristics:				
t_{DW}	Data Setup before $\overline{WR}$ High[1]	$0.5t_{CK}$– 4 + w		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK}$ – 1		ns
t_{WP}	$\overline{WR}$ Pulse Width	$0.5t_{CK}$ – 3 + w		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A13–0, $\overline{xMS}$ Setup before $\overline{WR}$ Low[2]	$0.25t_{CK}$ – 3		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK}$ – 3		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK}$ – 2	$0.25t_{CK}$ + 4	ns
t_{AW}	A13–0, $\overline{xMS}$ Setup before $\overline{WR}$ Deasserted	$0.75t_{CK}$ – 5 + w		ns
t_{WRA}	A13–0, $\overline{xMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK}$ – 1		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK}$ – 3		ns

[1] w = wait states 3 t_{CK}.
[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

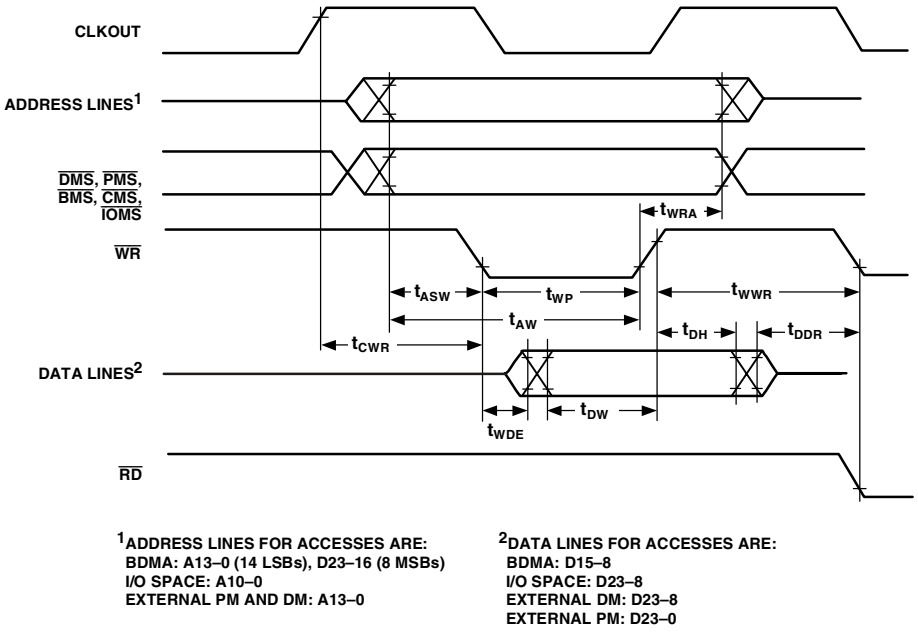

Figure 30. Memory Write

IDMA Read, Short Read Cycle

Table 25. IDMA Read, Short Read Cycle

Parameter[1, 2]		Min	Max	Unit
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low Before Start of Read[3]	0		ns
t_{IRP1}	Duration of Read (DM/PM1)[4]	10	$2t_{CK} - 5$	ns
t_{IRP2}	Duration of Read (PM2)[5]	10	$t_{CK} - 5$	ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High After Start of Read[3]		10	ns
t_{IKDH}	IAD15–0 Data Hold After End of Read[6]	0		ns
t_{IKDD}	IAD15–0 Data Disabled After End of Read[6]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled After Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid After Start of Read		10	ns

[1] Short Read Only must be disabled in the IDMA overlay memory mapped register. This mode is disabled by clearing (=0) Bit 14 of the IDMA overlay register, and is disabled by default upon reset.
[2] Consider using the Short Read Only mode, instead, because Short Read mode is not applicable at high clock frequencies.
[3] Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[4] DM Read or first half of PM Read.
[5] Second half of PM Read.
[6] End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

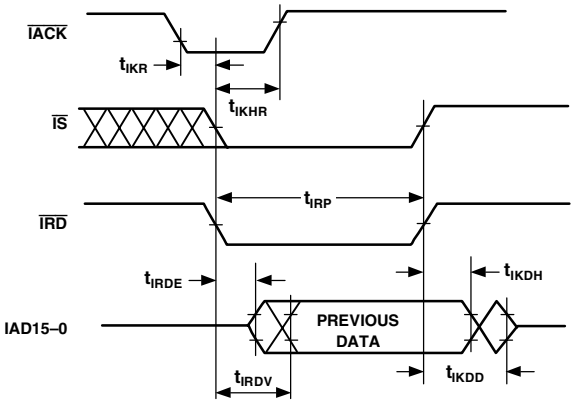

Figure 36. IDMA Read, Short Read Cycle

LQFP PACKAGE PINOUT

The LQFP package pinout is shown Figure 38 and in Table 27. Pin names in bold text in the table replace the plain-text-named functions when Mode C = 1. A + sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$. The multiplexed pins DT1/FO, TFS1/$\overline{\text{IRQ1}}$, RFS1/$\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default, upon reset.

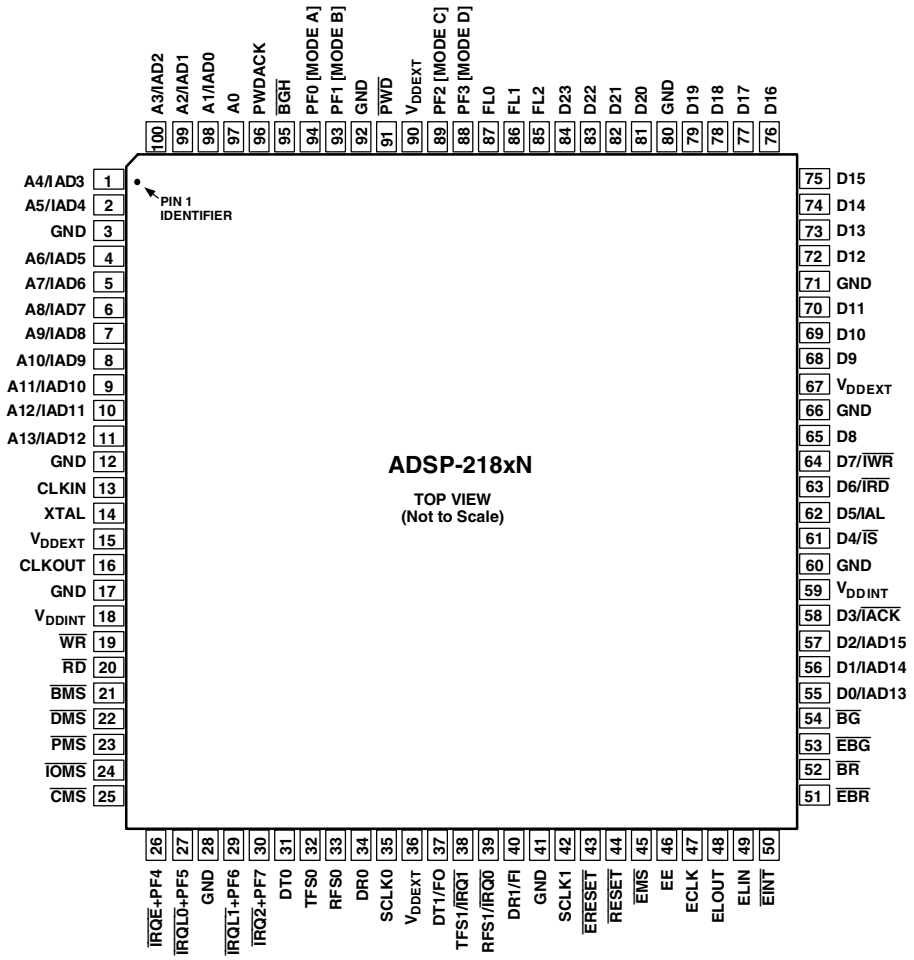

Figure 38. 100-Lead LQFP Pin Configuration

Table 27. LQFP Package Pinout

Pin No.	Pin Name
1	A4/**IAD3**
2	A5/**IAD4**
3	GND
4	A6/**IAD5**
5	A7/**IAD6**
6	A8/**IAD7**
7	A9/**IAD8**
8	A10/**IAD9**
9	A11/**IAD10**
10	A12/**IAD11**
11	A13/**IAD12**
12	GND
13	CLKIN
14	XTAL
15	V_{DDEXT}
16	CLKOUT
17	GND
18	V_{DDINT}
19	$\overline{WR}$
20	$\overline{RD}$
21	$\overline{BMS}$
22	$\overline{DMS}$
23	$\overline{PMS}$
24	$\overline{IOMS}$
25	$\overline{CMS}$
26	$\overline{IRQE}$ + PF4
27	$\overline{IRQL0}$ + PF5
28	GND
29	$\overline{IRQL1}$ + PF6
30	$\overline{IRQ2}$ + PF7
31	DT0
32	TFS0
33	RFS0
34	DR0
35	SCLK0
36	V_{DDEXT}
37	DT1/FO
38	TFS1/$\overline{IRQ1}$
39	RFS1/$\overline{IRQ0}$
40	DR1/FI
41	GND
42	SCLK1
43	$\overline{ERESET}$
44	$\overline{RESET}$
45	$\overline{EMS}$
46	EE
47	ECLK
48	ELOUT
49	ELIN
50	$\overline{EINT}$

Table 27. LQFP Package Pinout (Continued)

Pin No.	Pin Name
51	$\overline{EBR}$
52	$\overline{BR}$
53	$\overline{EBG}$
54	$\overline{BG}$
55	D0/**IAD13**
56	D1/**IAD14**
57	D2/**IAD15**
58	D3/$\overline{\textbf{IACK}}$
59	V_{DDINT}
60	GND
61	D4/$\overline{\textbf{IS}}$
62	D5/**IAL**
63	D6/$\overline{\textbf{IRD}}$
64	D7/$\overline{\textbf{IWR}}$
65	D8
66	GND
67	V_{DDEXT}
68	D9
69	D10
70	D11
71	GND
72	D12
73	D13
74	D14
75	D15
76	D16
77	D17
78	D18
79	D19
80	GND
81	D20
82	D21
83	D22
84	D23
85	FL2
86	FL1
87	FL0
88	PF3 [Mode D]
89	PF2 [Mode C]
90	V_{DDEXT}
91	$\overline{PWD}$
92	GND
93	PF1 [Mode B]
94	PF0 [Mode A]
95	$\overline{BGH}$
96	PWDACK
97	A0
98	A1/**IAD0**
99	A2/**IAD1**
100	A3/**IAD2**

OUTLINE DIMENSIONS

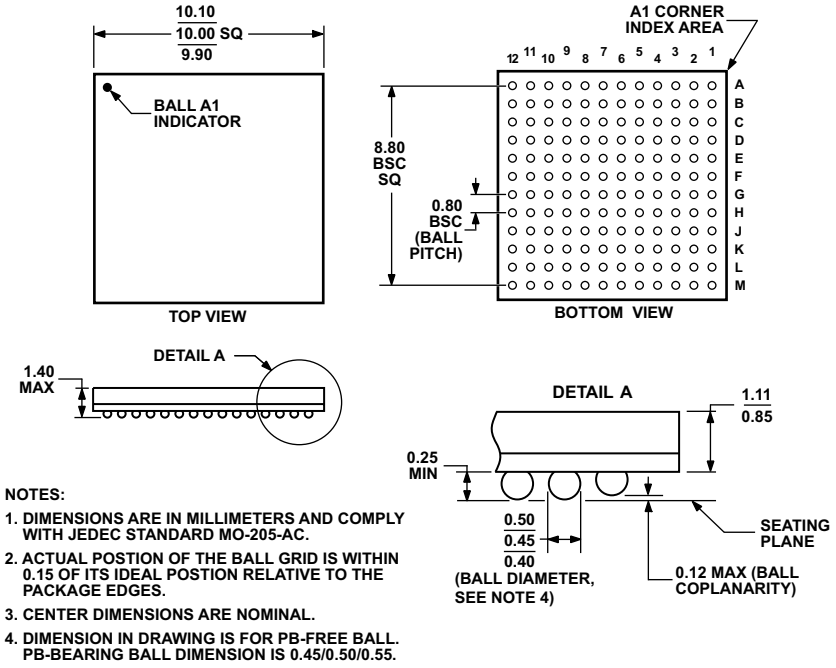

Figure 40. 144-Ball BGA [CSP_BGA] (BC-144-6)

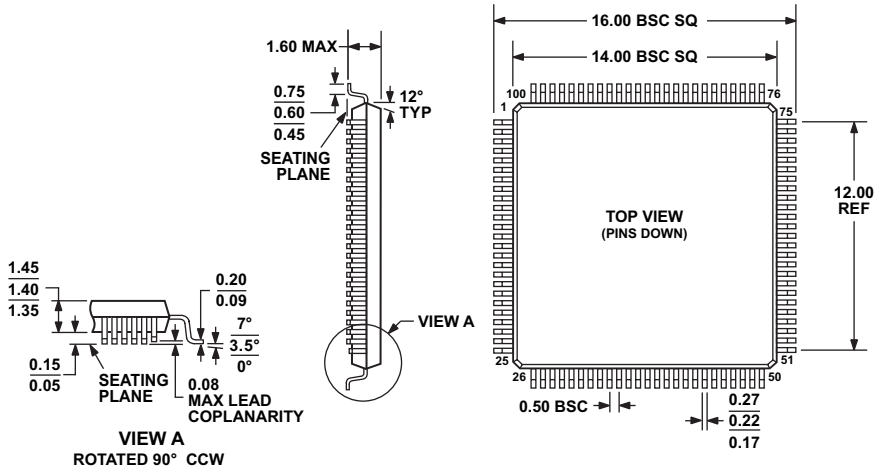

Figure 41. 100-Lead Low Profile Quad Flat Package [LQFP] (ST-100-1)

SURFACE MOUNT DESIGN

Table 29 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard*.

Table 29. BGA Data for Use with Surface Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
144-Ball BGA (BC-144-6)	Solder Mask Defined	0.40 mm diameter	0.50 mm diameter

ORDERING GUIDE

Model	Temperature Range[1]	Instruction Rate (MHz)	Package Description	Package Option
ADSP-2184NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2184NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2184NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2184NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2184NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2185NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2185NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2185NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2185NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2185NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2185NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2186NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2186NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2186NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2186NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2186NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2186NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2187NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2187NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2187NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2187NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2187NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2187NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2188NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2188NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2188NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2188NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2188NKCAZ-320[2]	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2188NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2188NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2189NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2189NBCAZ-320[2]	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2189NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2189NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2189NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2189NKCAZ-320[2]	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2189NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2189NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1

[1] Ranges shown represent ambient temperature.
[2] Z = Pb-free part.