Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, Serial Port
Clock Rate	80MHz
Non-Volatile Memory	External
On-Chip RAM	160kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.90V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA, CSPBGA
Supplier Device Package	144-CSPBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2187nbca-320

TABLE OF CONTENTS

REVISION HISTORY

8/06—Rev. 0 to Rev. A

Miscellaneous Format Updates..... Universal

Applied Corrections or Additional Information to:

GENERAL DESCRIPTION

The ADSP-218xN series consists of six single chip microcomputers optimized for digital signal processing applications. The high-level block diagram for the ADSP-218xN series members appears on the previous page. All series members are pin-compatible and are differentiated solely by the amount of on-chip SRAM. This feature, combined with ADSP-21xx code compatibility, provides a great deal of flexibility in the design decision. Specific family members are shown in Table 1.

Table 1. ADSP-218xN DSP Microcomputer Family

Device	Program Memory (K words)	Data Memory (K words)
ADSP-2184N	4	4
ADSP-2185N	16	16
ADSP-2186N	8	8
ADSP-2187N	32	32
ADSP-2188N	48	56
ADSP-2189N	32	48

ADSP-218xN series members combine the ADSP-2100 family base architecture (three computational units, data address generators, and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, Flag I/O, extensive interrupt capabilities, and on-chip program and data memory.

ADSP-218xN series members integrate up to 256K bytes of on-chip memory configured as up to 48K words (24-bit) of program RAM, and up to 56K words (16-bit) of data RAM. Power-down circuitry is also provided to meet the low power needs of battery-operated portable equipment. The ADSP-218xN is available in a 100-lead LQFP package and 144-ball BGA.

Fabricated in a high-speed, low-power, 0.18 µm CMOS process, ADSP-218xN series members operate with a 12.5 ns instruction cycle time. Every instruction can execute in a single processor cycle.

The ADSP-218xN's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle, ADSP-218xN series members can:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computational operation

This takes place while the processor continues to:

- Receive and transmit data through the two serial ports
- Receive and/or transmit data through the internal DMA port
- Receive and/or transmit data through the byte DMA port
- Decrement timer

ARCHITECTURE OVERVIEW

The ADSP-218xN series instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-218xN assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

The functional block diagram is an overall block diagram of the ADSP-218xN series. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add, and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations.

The shifter can be used to efficiently implement numeric format control, including multiword and block floating-point representations.

The internal result (R) bus connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls, and returns in a single cycle. With internal loop counters and loop stacks, ADSP-218xN series members execute looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Five internal buses provide efficient data transfer:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting ADSP-218xN series members to fetch two operands in a single cycle, one from program memory and one from data memory. ADSP-218xN series members can fetch an operand from program memory and the next instruction in the same cycle.

In lieu of the address and data bus for external memory connection, ADSP-218xN series members may be configured for 16-bit Internal DMA port (IDMA port) connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSP's on-chip program and data RAM.

An interface to low-cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals ($\overline{BR}$, $\overline{BGH}$, and $\overline{BG}$). One execution mode (Go Mode) allows the ADSP-218xN to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

ADSP-218xN series members can respond to eleven interrupts. There can be up to six external interrupts (one edge-sensitive, two level-sensitive, and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORT), the BDMA port, and the power-down circuitry. There is also a master $\overline{RESET}$ signal. The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation.

Each port can generate an internal programmable serial clock or accept an external serial clock.

ADSP-218xN series members provide up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, eight flags are programmable as inputs or outputs, and three flags are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) decrements every n processor cycle, where n is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

ADSP-218xN series members incorporate two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Following is a brief list of the capabilities of the ADSP-218xN SPORTs. For additional information on Serial Ports, refer to the *ADSP-218x DSP Hardware Reference*.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulsewidths and timings.
- SPORTs support serial data word lengths from 3 bits to 16 bits and provide optional A-law and μ-law companding, according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24 word or 32-word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts ($\overline{IRQ0}$ and $\overline{IRQ1}$) and the FI and FO signals. The internally generated serial clock may still be used in this configuration.

Table 3. Interrupt Priority and Interrupt Vector Addresses

Source Of Interrupt	Interrupt Vector Address (Hex)
Reset (or Power-Up with PUCR = 1)	0x0000 (Highest Priority)
Power-Down (Nonmaskable)	0x002C
$\overline{\text{IRQ2}}$	0x0004
$\overline{\text{IRQL1}}$	0x0008
$\overline{\text{IRQL0}}$	0x000C
SPORT0 Transmit	0x0010
SPORT0 Receive	0x0014
$\overline{\text{IRQE}}$	0x0018
BDMA Interrupt	0x001C
SPORT1 Transmit or $\overline{\text{IRQ1}}$	0x0020
SPORT1 Receive or $\overline{\text{IRQ0}}$	0x0024
Timer	0x0028 (Lowest Priority)

Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially. Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The power-down interrupt is nonmaskable.

ADSP-218xN series members mask all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect serial port autobuffering or DMA transfers.

The interrupt control register, ICNTL, controls interrupt nesting and defines the $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ external interrupts to be either edge- or level-sensitive. The $\overline{\text{IRQE}}$ pin is an external edge-sensitive interrupt and can be forced and cleared. The $\overline{\text{IRQL0}}$ and $\overline{\text{IRQL1}}$ pins are external level sensitive interrupts.

The IFC register is a write-only register used to force and clear interrupts. On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are 12 levels deep to allow interrupt, loop, and subroutine nesting. The following instructions allow global enable or disable servicing of the interrupts (including power-down), regardless of the state of IMASK:

```
ENA INTS;
DIS INTS;
```

Disabling the interrupts does not affect serial port autobuffering or DMA. When the processor is reset, interrupt servicing is enabled.

LOW-POWER OPERATION

ADSP-218xN series members have three low-power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

Power-Down

ADSP-218xN series members have a low-power feature that lets the processor enter a very low-power dormant state through hardware or software control. Following is a brief list of power-down features. Refer to the *ADSP-218x DSP Hardware Reference*, "System Interface" chapter, for detailed information about the power-down feature.

- Quick recovery from power-down. The processor begins executing instructions in as few as 200 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the lowest power rating and 200 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits approximately 4096 CLKIN cycles for the crystal oscillator to start or stabilize), and letting the oscillator run to allow 200 CLKIN cycle start-up.
- Power-down is initiated by either the power-down pin ($\overline{\text{PWD}}$) or the software power-down force bit. Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt also can be used as a nonmaskable, edge-sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{\text{RESET}}$ pin also can be used to terminate power-down.
- Power-down acknowledge pin (PWDACK) indicates when the processor has entered power-down.

Idle

When the ADSP-218xN is in the Idle Mode, the processor waits indefinitely in a low-power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. In Idle mode IDMA, BDMA, and autobuffer cycle steals still occur.

Slow Idle

The IDLE instruction is enhanced on ADSP-218xN series members to let the processor's internal clock signal be slowed, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the IDLE instruction.

The format of the instruction is:

```
IDLE (n);
```

where n = 16, 32, 64, or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals,

MEMORY ARCHITECTURE

The ADSP-218xN series provides a variety of memory and peripheral interface options. The key functional groups are Program Memory, Data Memory, Byte Memory, and I/O. Refer to Figure 4 through Figure 9, Table 4 on Page 11, and Table 5 on Page 11 for PM and DM memory allocations in the ADSP-218xN series.

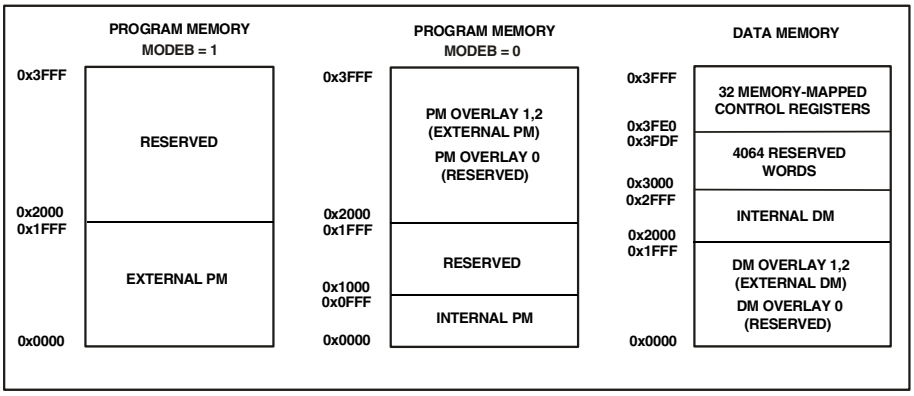

Figure 4. ADSP-2184 Memory Architecture

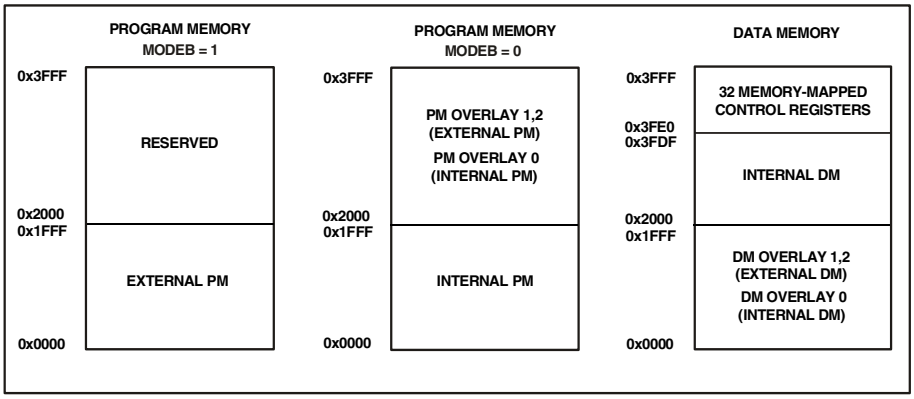

Figure 5. ADSP-2185 Memory Architecture

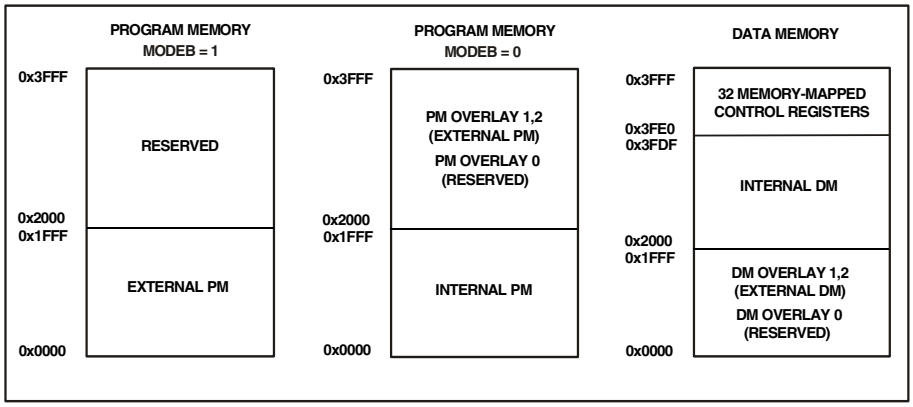

Figure 6. ADSP-2186 Memory Architecture

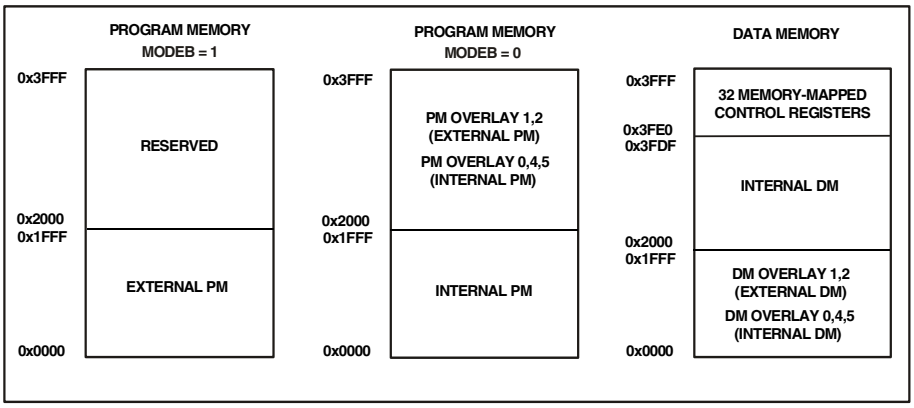

Figure 7. ADSP-2187 Memory Architecture

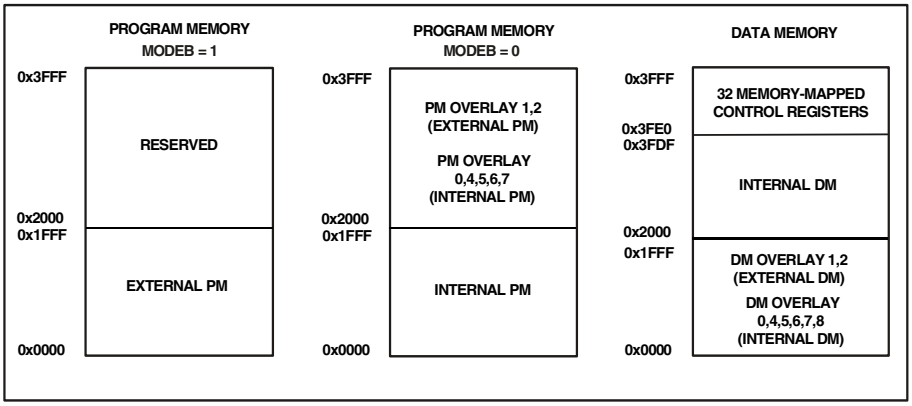

Figure 8. ADSP-2188 Memory Architecture

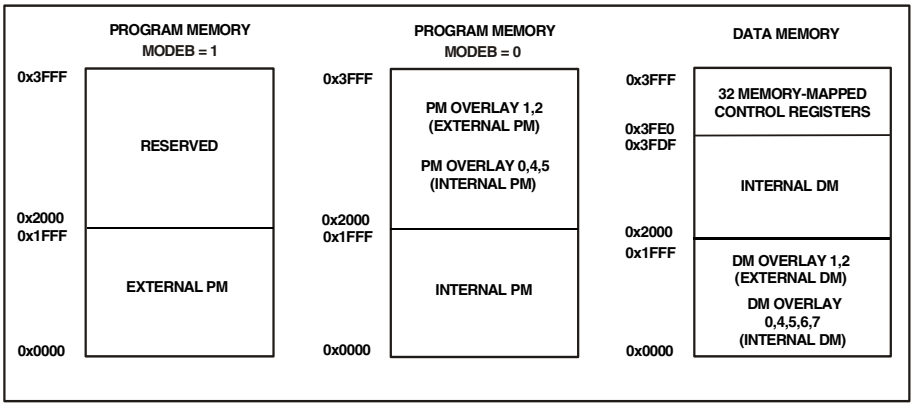

Figure 9. ADSP-2189 Memory Architecture

Program Memory

Program Memory (Full Memory Mode) is a 24-bit-wide space for storing both instruction opcodes and data. The member DSPs of this series have up to 48K words of Program Memory RAM on chip, and the capability of accessing up to two 8K external memory overlay spaces, using the external data bus.

Program Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0). External program execution is not available in host mode due to a restricted data bus that is only 16 bits wide.

Table 4. PMOVLAY Bits

Processor	PMOVLAY	Memory	A13	A12–0
ADSP-2184N	No Internal Overlay Region	Not Applicable	Not Applicable	Not Applicable
ADSP-2185N	0	Internal Overlay	Not Applicable	Not Applicable
ADSP-2186N	No Internal Overlay Region	Not Applicable	Not Applicable	Not Applicable
ADSP-2187N	0, 4, 5	Internal Overlay	Not Applicable	Not Applicable
ADSP-2188N	0, 4, 5, 6, 7	Internal Overlay	Not Applicable	Not Applicable
ADSP-2189N	0, 4, 5	Internal Overlay	Not Applicable	Not Applicable
All Processors	1	External Overlay 1	0	13 LSBs of Address Between 0x2000 and 0x3FFF
All Processors	2	External Overlay 2	1	13 LSBs of Address Between 0x2000 and 0x3FFF

Data Memory

Data Memory (Full Memory Mode) is a 16-bit-wide space used for the storage of data variables and for memory-mapped control registers. The ADSP-218xN series has up to 56K words of Data Memory RAM on-chip. Part of this space is used by 32 memory-mapped registers. Support also exists for up to two 8K external memory overlay spaces through the external data bus.

All internal accesses complete in one cycle. Accesses to external memory are timed using the wait states specified by the DWAIT register and the wait state mode bit.

Data Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0).

Table 5. DMOVLAY Bits

Processor	DMOVLAY	Memory	A13	A12–0
ADSP-2184N	No Internal Overlay Region	Not Applicable	Not Applicable	Not Applicable
ADSP-2185N	0	Internal Overlay	Not Applicable	Not Applicable
ADSP-2186N	No Internal Overlay Region	Not Applicable	Not Applicable	Not Applicable
ADSP-2187N	0, 4, 5	Internal Overlay	Not Applicable	Not Applicable
ADSP-2188N	0, 4, 5, 6, 7, 8	Internal Overlay	Not Applicable	Not Applicable
ADSP-2189N	0, 4, 5, 6, 7	Internal Overlay	Not Applicable	Not Applicable
All Processors	1	External Overlay 1	0	13 LSBs of Address Between 0x0000 and 0x1FFF
All Processors	2	External Overlay 2	1	13 LSBs of Address Between 0x0000 and 0x1FFF

Memory-Mapped Registers (New to the ADSP-218xM and N series)

ADSP-218xN series members have three memory-mapped registers that differ from other ADSP-21xx Family DSPs. The slight modifications to these registers (Wait State Control, Programmable Flag and Composite Select Control, and System Control) provide the ADSP-218xN's wait state and $\overline{\text{BMS}}$ control features. Default bit values at reset are shown; if no value is shown, the bit is undefined at reset. Reserved bits are shown on a grey field. These bits should always be written with zeros.

I/O Space (Full Memory Mode)

ADSP-218xN series members support an additional external memory space called I/O space. This space is designed to support simple connections to peripherals (such as data converters and external registers) or to bus interface ASIC data registers. I/O space supports 2048 locations of 16-bit wide data. The lower eleven bits of the external address bus are used; the upper three bits are undefined.

Two instructions were added to the core ADSP-2100 Family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated three-bit wait state registers,

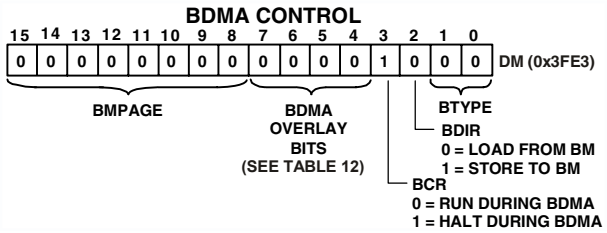

Figure 13. BDMA Control Register

The BDMA circuit supports four different data formats that are selected by the BTYPE register field. The appropriate number of 8-bit accesses are done from the byte memory space to build the word size selected. Table 7 shows the data formats supported by the BDMA circuit.

Table 7. Data Formats

BTYPE	Internal Memory Space	Word Size	Alignment
00	Program Memory	24	Full Word
01	Data Memory	16	Full Word
10	Data Memory	8	MSBs
11	Data Memory	8	LSBs

Unused bits in the 8-bit data memory formats are filled with 0s. The BIAD register field is used to specify the starting address for the on-chip memory involved with the transfer. The 14-bit BEAD register specifies the starting address for the external byte memory space. The 8-bit BMPAGE register specifies the starting page for the external byte memory space. The BDIR register field selects the direction of the transfer. Finally, the 14-bit BWCOUNT register specifies the number of DSP words to transfer and initiates the BDMA circuit transfers.

BDMA accesses can cross page boundaries during sequential addressing. A BDMA interrupt is generated on the completion of the number of transfers specified by the BWCOUNT register.

The BWCOUNT register is updated after each transfer so it can be used to check the status of the transfers. When it reaches zero, the transfers have finished and a BDMA interrupt is generated. The BMPAGE and BEAD registers must not be accessed by the DSP during BDMA operations.

The source or destination of a BDMA transfer will always be on-chip program or data memory.

When the BWCOUNT register is written with a nonzero value the BDMA circuit starts executing byte memory accesses with wait states set by BMWAIT. These accesses continue until the count reaches zero. When enough accesses have occurred to create a destination word, it is transferred to or from on-chip memory. The transfer takes one DSP cycle. DSP accesses to external memory have priority over BDMA byte memory accesses.

The BDMA Context Reset bit (BCR) controls whether the processor is held off while the BDMA accesses are occurring. Setting the BCR bit to 0 allows the processor to continue operations. Setting the BCR bit to 1 causes the processor to stop execution while the BDMA accesses are occurring, to clear the context of the processor, and start execution at address 0 when the BDMA accesses have completed.

The BDMA overlay bits specify the OVLAY memory blocks to be accessed for internal memory. Set these bits as indicated in Figure 13.

Note: BDMA cannot access external overlay memory regions 1 and 2.

The BMWAIT field, which has four bits on ADSP-218xN series members, allows selection up to 15 wait states for BDMA transfers.

Internal Memory DMA Port (IDMA Port; Host Memory Mode)

The IDMA Port provides an efficient means of communication between a host system and ADSP-218xN series members. The port is used to access the on-chip program memory and data memory of the DSP with only one DSP cycle per word overhead. The IDMA port cannot, however, be used to write to the DSP's memory-mapped control registers. A typical IDMA transfer process is shown as follows:

1. Host starts IDMA transfer.
2. Host checks $\overline{\text{IACK}}$ control line to see if the DSP is busy.
3. Host uses $\overline{\text{IS}}$ and IAL control lines to latch either the DMA starting address (IDMAA) or the PM/DM OVLAY selection into the DSP's IDMA control registers. If Bit 15 = 1, the values of Bits 7–0 represent the IDMA overlay; Bits 14–8 must be set to 0. If Bit 15 = 0, the value of Bits 13–0 represent the starting address of internal memory to be accessed and Bit 14 reflects PM or DM for access. Set IDDMOVLAY and IDPMOVLAY bits in the IDMA overlay register as indicted in Table 8.
4. Host uses $\overline{\text{IS}}$ and $\overline{\text{IRD}}$ (or $\overline{\text{IWR}}$) to read (or write) DSP internal memory (PM or DM).
5. Host checks $\overline{\text{IACK}}$ line to see if the DSP has completed the previous IDMA operation.
6. Host ends IDMA transfer.

Table 8. IDMA/BDMA Overlay Bits

Processor	IDMA/BDMA PMOVLAY	IDMA/BDMA DMOVLAY
ADSP-2184N	0	0
ADSP-2185N	0	0
ADSP-2186N	0	0
ADSP-2187N	0, 4, 5	0, 4, 5
ADSP-2188N	0, 4, 5, 6, 7	0, 4, 5, 6, 7, 8
ADSP-2189N	0, 4, 5	0, 4, 5, 6, 7

The IDMA port has a 16-bit multiplexed address and data bus and supports 24-bit program memory. The IDMA port is completely asynchronous and can be written while the ADSP-218xN is operating at full speed.

The DSP memory address is latched and then automatically incremented after each IDMA transaction. An external device can therefore access a block of sequentially addressed memory by specifying only the starting address of the block. This increases throughput as the address does not have to be sent for each memory access.

IDMA port access occurs in two phases. The first is the IDMA Address Latch cycle. When the acknowledge is asserted, a 14-bit address and 1-bit destination type can be driven onto the bus by an external device. The address specifies an on-chip memory location, the destination type specifies whether it is a DM or PM access. The falling edge of the IDMA address latch signal (IAL) or the missing edge of the IDMA select signal ($\overline{IS}$) latches this value into the IDMAA register.

Once the address is stored, data can be read from, or written to, the ADSP-218xN's on-chip memory. Asserting the select line ($\overline{IS}$) and the appropriate read or write line ($\overline{IRD}$ and $\overline{IWR}$ respectively) signals the ADSP-218xN that a particular transaction is required. In either case, there is a one-processor-cycle delay for synchronization. The memory access consumes one additional processor cycle.

Once an access has occurred, the latched address is automatically incremented, and another access can occur.

Through the IDMAA register, the DSP can also specify the starting address and data format for DMA operation. Asserting the IDMA port select ($\overline{IS}$) and address latch enable (IAL) directs the ADSP-218xN to write the address onto the IAD14–0 bus into the IDMA Control Register (Figure 14). If Bit 15 is set to 0, IDMA latches the address. If Bit 15 is set to 1, IDMA latches into the OVLAY register. This register, also shown in Figure 14, is memory-mapped at address DM (0x3FE0). Note that the latched address (IDMAA) cannot be read back by the host.

When Bit 14 in 0x3FE7 is set to zero, short reads use the timing shown in Figure 36 on Page 38. When Bit 14 in 0x3FE7 is set to 1, timing in Figure 37 on Page 39 applies for short reads in short read only mode. Set IDDMOVLAY and IDPMOVLAY bits in the IDMA overlay register as indicated in Table 8. Refer to the *ADSP-218x DSP Hardware Reference* for additional details.

Note: In full memory mode all locations of 4M-byte memory space are directly addressable. In host memory mode, only address pin A0 is available, requiring additional external logic to provide address information for the byte.

Bootstrap Loading (Booting)

ADSP-218xN series members have two mechanisms to allow automatic loading of the internal program memory after reset. The method for booting is controlled by the Mode A, B, and C configuration bits.

When the mode pins specify BDMA booting, the ADSP-218xN initiates a BDMA boot sequence when reset is released.

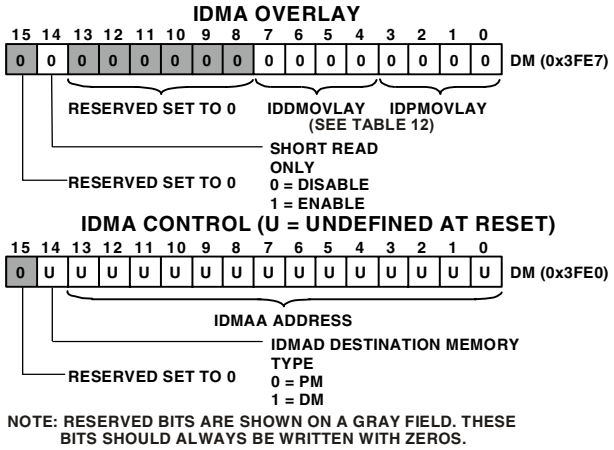

Figure 14. IDMA OVLAY/Control Registers

The BDMA interface is set up during reset to the following defaults when BDMA booting is specified: the BDIR, BMPAGE, BIAD, and BEAD registers are set to 0, the BTYPE register is set to 0 to specify program memory 24-bit words, and the BWCOUNT register is set to 32. This causes 32 words of on-chip program memory to be loaded from byte memory. These 32 words are used to set up the BDMA to load in the remaining program code. The BCR bit is also set to 1, which causes program execution to be held off until all 32 words are loaded into on-chip program memory. Execution then begins at address 0.

The ADSP-2100 Family development software (Revision 5.02 and later) fully supports the BDMA booting feature and can generate byte memory space-compatible boot code.

The IDLE instruction can also be used to allow the processor to hold off execution while booting continues through the BDMA interface. For BDMA accesses while in Host Mode, the addresses to boot memory must be constructed externally to the ADSP-218xN. The only memory address bit provided by the processor is A0.

IDMA Port Booting

ADSP-218xN series members can also boot programs through its internal DMA port. If Mode C = 1, Mode B = 0, and Mode A = 1, the ADSP-218xN boots from the IDMA port. IDMA feature can load as much on-chip memory as desired. Program execution is held off until the host writes to on-chip program memory location 0.

BUS REQUEST AND BUS GRANT

ADSP-218xN series members can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the Bus Request

($\overline{BR}$) signal. If the ADSP-218xN is not performing an external memory access, it responds to the active $\overline{BR}$ input in the following processor cycle by:

- Three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- Asserting the bus grant ($\overline{BG}$) signal, and
- Halting program execution.

If Go Mode is enabled, the ADSP-218xN will not halt program execution until it encounters an instruction that requires an external memory access.

If an ADSP-218xN series member is performing an external memory access when the external device asserts the $\overline{BR}$ signal, it will not three-state the memory interfaces nor assert the $\overline{BG}$ signal until the processor cycle after the access completes. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, re-enables the output drivers, and continues program execution from the point at which it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active.

The $\overline{BGH}$ pin is asserted when an ADSP-218xN series member requires the external bus for a memory or BDMA access, but is stopped. The other device can release the bus by deasserting bus request. Once the bus is released, the ADSP-218xN deasserts $\overline{BG}$ and $\overline{BGH}$ and executes the external memory access.

FLAG I/O PINS

ADSP-218xN series members have eight general-purpose programmable input/output flag pins. They are controlled by two memory-mapped registers. The PFTYPE register determines the direction, 1 = output and 0 = input. The PFDATA register is used to read and write the values on the pins. Data being read from a pin configured as an input is synchronized to the ADSP-218xN's clock. Bits that are programmed as outputs will read the value being output. The PF pins default to input during reset.

In addition to the programmable flags, ADSP-218xN series members have five fixed-mode flags, FI, FO, FL0, FL1, and FL2. FL0 to FL2 are dedicated output flags. FI and FO are available as an alternate configuration of SPORT1.

Note: Pins PF0, PF1, PF2, and PF3 are also used for device configuration during reset.

INSTRUCTION SET DESCRIPTION

The ADSP-218xN series assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 Family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to utilize on-chip memory and conform to the ADSP-218xN's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return, or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction, with up to two fetches or one write to processor memory space, during a single instruction cycle.

DEVELOPMENT SYSTEM

Analog Devices' wide range of software and hardware development tools supports the ADSP-218xN series. The DSP tools include an integrated development environment, an evaluation kit, and a serial port emulator.

VisualDSP++®† is an integrated development environment, allowing for fast and easy development, debug, and deployment. The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy-to-use assembler that is based on an algebraic syntax; an archiver (librarian/library builder); a linker; a PROM-splitter utility; a cycle-accurate, instruction-level simulator; a C compiler; and a C run-time library that includes DSP and mathematical functions.

Debugging both C and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C and assembly code (interleaved source and object information)
- Insert break points
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution

† VisualDSP++ is a registered trademark of Analog Devices, Inc.

Table 12. Unused Pin Terminations (Continued)

Pin Name[1]	I/O 3-State (Z)[2]	Reset State	Hi-Z[3] Caused By	Unused Configuration
$\overline{\text{ERESET}}$	I	I		Float
$\overline{\text{EMS}}$	O	O		Float
$\overline{\text{EINT}}$	I	I		Float
ECLK	I	I		Float
ELIN	I	I		Float
ELOUT	O	O		Float

[1] CLKIN, $\overline{\text{RESET}}$, and PF3 – 0/Mode D – A are not included in this table because these pins must be used.
[2] All bidirectional pins have three-stated outputs. When the pin is configured as an output, the output is Hi-Z (high impedance) when inactive.
[3] Hi-Z = High Impedance.
[4] If the CLKOUT pin is not used, turn it OFF, using CLKODIS in SPORT0 autobuffer control register.
[5] If the Interrupt/Programmable Flag pins are not used, there are two options: Option 1: When these pins are configured as INPUTS at reset and function as interrupts and input flag pins, pull the pins High (inactive). Option 2: Program the unused pins as OUTPUTS, set them to 1 prior to enabling interrupts, and let pins float.

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter[1]	K Grade (Commercial)		B Grade (Industrial)		Unit
	Min	Max	Min	Max	
V_{DDINT}	1.71	1.89	1.8	2.0	V
V_{DDEXT}	1.71	3.6	1.8	3.6	V
V_{INPUT}[2]	V_{IL} = – 0.3	V_{IH} = + 3.6	V_{IL} = – 0.3	V_{IH} = + 3.6	V
T_{AMB}	0	70	–40	+85	°C

[1] Specifications subject to change without notice.

[2] The ADSP-218xN is 3.3 V tolerant (always accepts up to 3.6 V max V_{IH}), but voltage compliance (on outputs, V_{OH}) depends on the input V_{DDEXT}, because V_{OH} (max) approximately equals V_{DDEXT} (max). This 3.3 V tolerance applies to bidirectional pins (D23–D0, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A13–A1, PF7–PF0) and input-only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$).

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Hi-Level Input Voltage[2, 3]	@ V_{DDEXT} = 1.71 V to 2.0 V, V_{DDINT} = max	1.25			V
		@ V_{DDEXT} = 2.1 V to 3.6 V, V_{DDINT} = max	1.7			V
V_{IL}	Lo-Level Input Voltage[2, 3]	@ $V_{DDEXT} \leq$ 2.0 V, V_{DDINT} = min			0.6	V
		@ $V_{DDEXT} \geq$ 2.0 V, V_{DDINT} = min			0.7	V
V_{OH}	Hi-Level Output Voltage[2, 4, 5]	@ V_{DDEXT} = 1.71 V to 2.0 V, I_{OH} = – 0.5 mA	1.35			V
		@ V_{DDEXT} = 2.1 V to 2.9 V, I_{OH} = – 0.5 mA	2.0			V
		@ V_{DDEXT} = 3.0 V to 3.6 V, I_{OH} = – 0.5 mA	2.4			V
		@ V_{DDEXT} = 1.71 V to 3.6 V, I_{OH} = – 100 µA[6]	V_{DDEXT} – 0.3			V
V_{OL}	Lo-Level Output Voltage[2, 4, 5]	@ V_{DDEXT} = 1.71 V to 3.6 V, I_{OL} = 2.0 mA			0.4	V
I_{IH}	Hi-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 3.6 V			10	µA
I_{IL}	Lo-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 0 V			10	µA
I_{OZH}	Three-State Leakage Current[7]	@ V_{DDEXT} = max, V_{IN} = 3.6 V[8]			10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DDEXT} = max, V_{IN} = 0 V[8]			10	µA
I_{DD}	Supply Current (Idle)[9]	@ V_{DDINT} = 1.8 V, t_{CK} = 12.5 ns, T_{AMB} = 25°C		6		mA
I_{DD}	Supply Current (Dynamic)[10]	@ V_{DDINT} = 1.8 V, t_{CK} = 12.5 ns[11], T_{AMB} = 25°C		25		mA

ENVIRONMENTAL CONDITIONS

Table 14. Thermal Resistance

Rating Description[1]	Symbol	LQFP (°C/W)	BGA (°C/W)
Thermal Resistance (Case-to-Ambient)	θ_{CA}	48	63.3
Thermal Resistance (Junction-to-Ambient)	θ_{JA}	50	70.7
Thermal Resistance (Junction-to-Case)	θ_{JC}	2	7.4

[1] Where the Ambient Temperature Rating (T_{AMB}) is:
$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W

TEST CONDITIONS

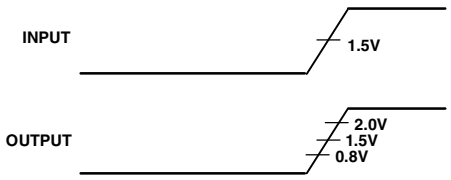

Figure 18. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

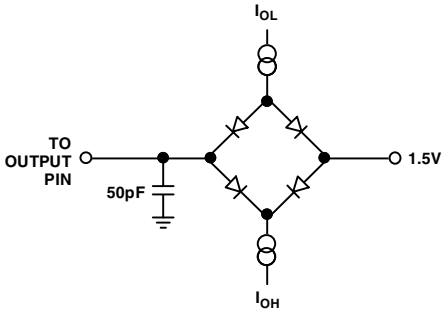

Figure 19. Equivalent Loading for AC Measurements (Including All Fixtures)

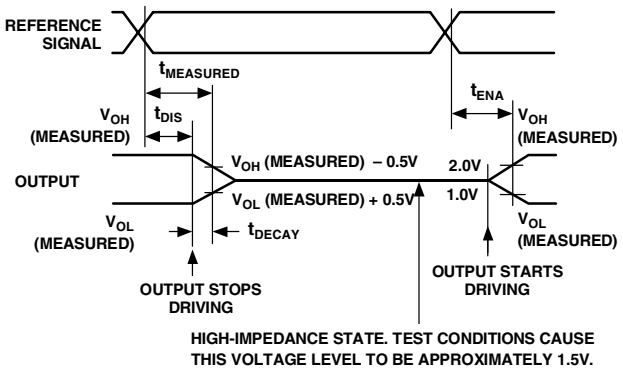

Figure 20. Output Enable/Disable

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 20. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitive load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 20. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Memory Read

Table 18. Memory Read

Parameter		Min	Max	Unit
Timing Requirements:				
t_{RDD}	$\overline{RD}$ Low to Data Valid[1]		$0.5t_{CK} - 5 + w$	ns
t_{AA}	A13–0, $\overline{xMS}$ to Data Valid[2]		$0.75t_{CK} - 6 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristics:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 3 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 2$	$0.25t_{CK} + 4$	ns
t_{ASR}	A13–0, $\overline{xMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 3$		ns
t_{RDA}	A13–0, $\overline{xMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 3$		ns

[1] w = wait states 3 t_{CK}.
[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

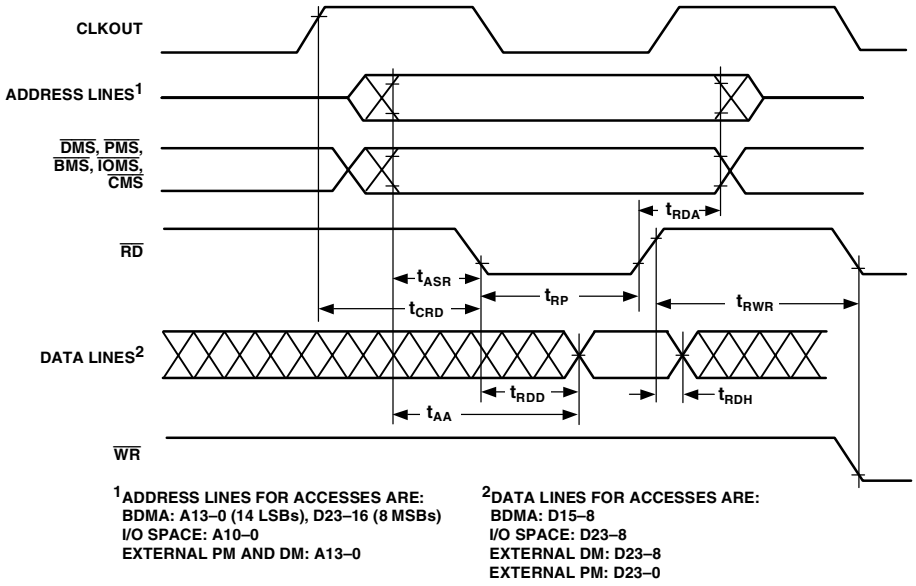

Figure 29. Memory Read

IDMA Address Latch

Table 21. IDMA Address Latch

Parameter		Min	Max	Unit
Timing Requirements:				
t_{IALP}	Duration of Address Latch[1, 2]	10		ns
t_{IASU}	IAD15–0 Address Setup Before Address Latch End[2]	5		ns
t_{IAH}	IAD15–0 Address Hold After Address Latch End[2]	3		ns
t_{IKA}	$\overline{IACK}$ Low before Start of Address Latch[2, 3]	0		ns
t_{IALS}	Start of Write or Read After Address Latch End[2, 3]	3		ns
t_{IALD}	Address Latch Start After Address Latch End[1, 2]	2		ns

[1] Start of Address Latch = $\overline{IS}$ Low and IAL High.
[2] End of Address Latch = $\overline{IS}$ High or IAL Low.
[3] Start of Write or Read = $\overline{IS}$ Low and $\overline{IWR}$ Low or $\overline{IRD}$ Low.

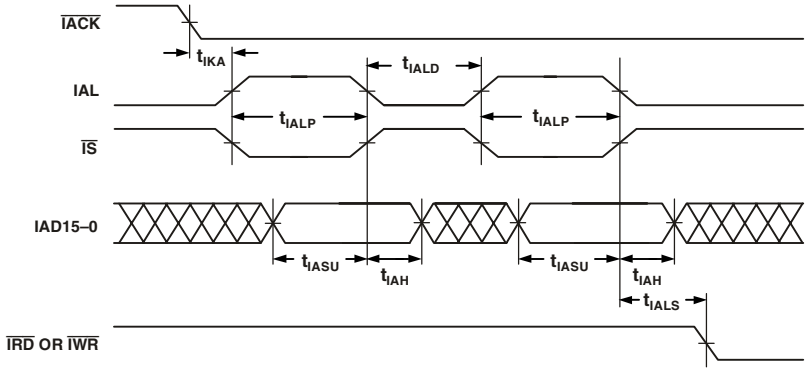

Figure 32. IDMA Address Latch

IDMA Write, Short Write Cycle

Table 22. IDMA Write, Short Write Cycle

Parameter		Min	Max	Unit
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low Before Start of Write[1]	0		ns
t_{IWP}	Duration of Write[1, 2]	10		ns
t_{IDSU}	IAD15–0 Data Setup Before End of Write[2, 3, 4]	3		ns
t_{IDH}	IAD15–0 Data Hold After End of Write[2, 3, 4]	2		ns
Switching Characteristic:				
t_{IKHW}	Start of Write to $\overline{IACK}$ High		10	ns

[1] Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2] End of Write = $\overline{IS}$ High or $\overline{IWR}$ High.
[3] If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[4] If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.

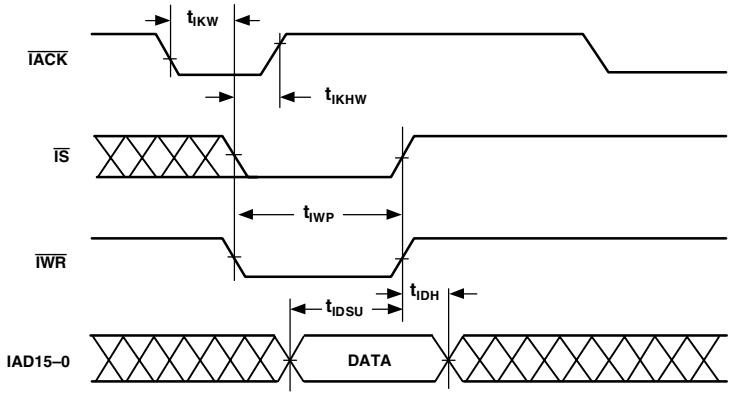

Figure 33. IDMA Write, Short Write Cycle

LQFP PACKAGE PINOUT

The LQFP package pinout is shown Figure 38 and in Table 27. Pin names in bold text in the table replace the plain-text-named functions when Mode C = 1. A + sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$. The multiplexed pins DT1/FO, TFS1/$\overline{\text{IRQ1}}$, RFS1/$\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default, upon reset.

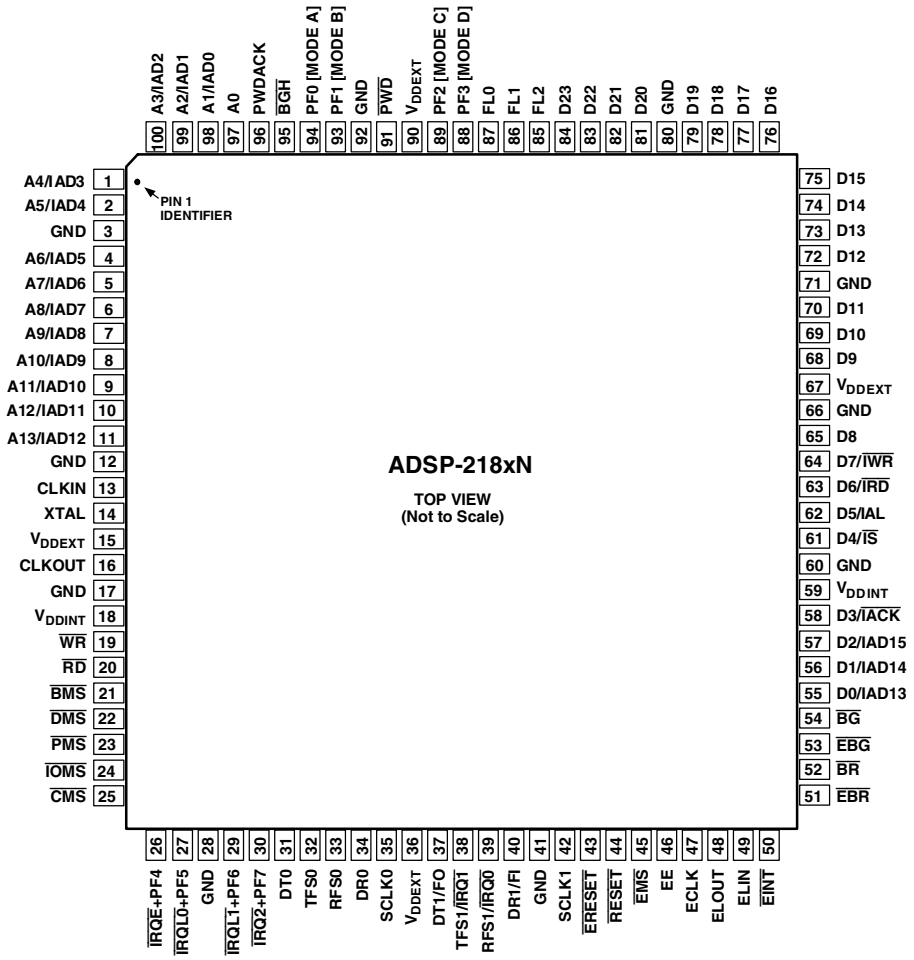

Figure 38. 100-Lead LQFP Pin Configuration

BGA PACKAGE PINOUT

The BGA package pinout is shown in Figure 39 and in Table 28. Pin names in bold text in the table replace the plain text named functions when Mode C = 1. A + sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$. The multiplexed pins DT1/FO, TFS1/$\overline{\text{IRQ1}}$, RFS1/$\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default upon reset.

12	11	10	9	8	7	6	5	4	3	2	1	
GND	GND	D22	NC	NC	NC	GND	NC	A0	GND	A1/IAD0	A2/IAD1	A
D16	D17	D18	D20	D23	V_{DDEXT}	GND	NC	NC	GND	A3/IAD2	A4/IAD3	B
D14	NC	D15	D19	D21	V_{DDEXT}	$\overline{\text{PWD}}$	A7/IAD6	A5/IAD4	$\overline{\text{RD}}$	A6/IAD5	PWDACK	C
GND	NC	D12	D13	NC	PF2 [MODE C]	PF1 [MODE B]	A9/IAD8	$\overline{\text{BGH}}$	NC	$\overline{\text{WR}}$	NC	D
D10	GND	V_{DDEXT}	GND	GND	PF3 [MODE D]	FL2	PF0 [MODE A]	FL0	A8/IAD7	V_{DDEXT}	V_{DDEXT}	E
D9	NC	D8	D11	D7/$\overline{\text{IWR}}$	NC	NC	FL1	A11/IAD10	A12/IAD11	NC	A13/IAD12	F
D4/$\overline{\text{IS}}$	NC	NC	D5/IAL	D6/$\overline{\text{IRD}}$	NC	NC	NC	A10/IAD9	GND	NC	XTAL	G
GND	NC	GND	D3/$\overline{\text{IACK}}$	D2/IAD15	TFS0	DT0	V_{DDINT}	GND	GND	GND	CLKIN	H
V_{DDINT}	V_{DDINT}	D1/IAD14	$\overline{\text{BG}}$	RFS1/$\overline{\text{IRQ0}}$	D0/IAD13	SCLK0	V_{DDEXT}	V_{DDEXT}	NC	V_{DDINT}	CLKOUT	J
$\overline{\text{EBG}}$	$\overline{\text{BR}}$	$\overline{\text{EBR}}$	$\overline{\text{ERESET}}$	SCLK1	TFS1/$\overline{\text{IRQ1}}$	RFS0	$\overline{\text{DMS}}$	$\overline{\text{BMS}}$	NC	NC	NC	K
$\overline{\text{EINT}}$	ELOUT	ELIN	$\overline{\text{RESET}}$	GND	DR0	$\overline{\text{PMS}}$	GND	$\overline{\text{IOMS}}$	$\overline{\text{IRQL1}}$ + PF6	NC	$\overline{\text{IRQE}}$ + PF4	L
ECLK	EE	$\overline{\text{EMS}}$	NC	GND	DR1/FI	DT1/FO	GND	$\overline{\text{CMS}}$	NC	$\overline{\text{IRQ2}}$ + PF7	$\overline{\text{IRQL0}}$ + PF5	M

Figure 39. 144-Ball BGA Package Pinout (Bottom View)

Table 28. BGA Package Pinout

Ball No.	Pin Name
A01	A2/**IAD1**
A02	A1/**IAD0**
A03	GND
A04	A0
A05	NC
A06	GND
A07	NC
A08	NC
A09	NC
A10	D22
A11	GND
A12	GND
B01	A4/**IAD3**
B02	A3/**IAD2**
B03	GND
B04	NC
B05	NC
B06	GND
B07	V_{DDEXT}
B08	D23
B09	D20
B10	D18
B11	D17
B12	D16
C01	PWDACK
C02	A6/**IAD5**
C03	$\overline{RD}$
C04	A5/**IAD4**
C05	A7/**IAD6**
C06	$\overline{PWD}$
C07	V_{DDEXT}
C08	D21
C09	D19
C10	D15
C11	NC
C12	D14
D01	NC
D02	$\overline{WR}$
D03	NC
D04	$\overline{BGH}$
D05	A9/**IAD8**
D06	PF1 [MODE B]
D07	PF2 [MODE C]
D08	NC
D09	D13
D10	D12
D11	NC
D12	GND
E01	V_{DDEXT}

Table 28. BGA Package Pinout (Continued)

Ball No.	Pin Name
E02	V_{DDEXT}
E03	A8/**IAD7**
E04	FL0
E05	PF0 [MODE A]
E06	FL2
E07	PF3 [MODE D]
E08	GND
E09	GND
E10	V_{DDEXT}
E11	GND
E12	D10
F01	A13/**IAD12**
F02	NC
F03	A12/**IAD11**
F04	A11/**IAD10**
F05	FL1
F06	NC
F07	NC
F08	D7/$\overline{\textbf{IWR}}$
F09	D11
F10	D8
F11	NC
F12	D9
G01	XTAL
G02	NC
G03	GND
G04	A10/**IAD9**
G05	NC
G06	NC
G07	NC
G08	D6/$\overline{\textbf{IRD}}$
G09	D5/**IAL**
G10	NC
G11	NC
G12	D4/$\overline{\textbf{IS}}$
H01	CLKIN
H02	GND
H03	GND
H04	GND
H05	V_{DDINT}
H06	DT0
H07	TFS0
H08	D2/**IAD15**
H09	D3/$\overline{\textbf{IACK}}$
H10	GND
H11	NC
H12	GND
J01	CLKOUT
J02	V_{DDINT}

Table 28. BGA Package Pinout (Continued)

Ball No.	Pin Name
J03	NC
J04	V_{DDEXT}
J05	V_{DDEXT}
J06	SCLK0
J07	D0/**IAD13**
J08	RFS1/$\overline{IRQ0}$
J09	$\overline{BG}$
J10	D1/**IAD14**
J11	V_{DDINT}
J12	V_{DDINT}
K01	NC
K02	NC
K03	NC
K04	$\overline{BMS}$
K05	$\overline{DMS}$
K06	RFS0
K07	TFS1/$\overline{IRQ1}$
K08	SCLK1
K09	$\overline{ERESET}$
K10	$\overline{EBR}$
K11	$\overline{BR}$
K12	$\overline{EBG}$
L01	$\overline{IRQE}$ + PF4
L02	NC
L03	$\overline{IRQL1}$ + PF6
L04	$\overline{IOMS}$
L05	GND
L06	$\overline{PMS}$
L07	DR0
L08	GND
L09	$\overline{RESET}$
L10	ELIN
L11	ELOUT
L12	$\overline{EINT}$
M01	$\overline{IRQL0}$ + PF5
M02	$\overline{IRQL2}$ + PF7
M03	NC
M04	$\overline{CMS}$
M05	GND
M06	DT1/FO
M07	DR1/FI
M08	GND
M09	NC
M10	$\overline{EMS}$
M11	EE
M12	ECLK