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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, Serial Port
Clock Rate	80MHz
Non-Volatile Memory	External
On-Chip RAM	192kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.90V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA, CSPBGA
Supplier Device Package	144-CSPBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2189nbca-320

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REVISION HISTORY

8/06—Rev. 0 to Rev. A

Miscellaneous Format Updates..... Universal

Applied Corrections or Additional Information to:

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting ADSP-218xN series members to fetch two operands in a single cycle, one from program memory and one from data memory. ADSP-218xN series members can fetch an operand from program memory and the next instruction in the same cycle.

In lieu of the address and data bus for external memory connection, ADSP-218xN series members may be configured for 16-bit Internal DMA port (IDMA port) connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSP's on-chip program and data RAM.

An interface to low-cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals ($\overline{BR}$, $\overline{BGH}$, and $\overline{BG}$). One execution mode (Go Mode) allows the ADSP-218xN to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

ADSP-218xN series members can respond to eleven interrupts. There can be up to six external interrupts (one edge-sensitive, two level-sensitive, and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORT), the BDMA port, and the power-down circuitry. There is also a master $\overline{RESET}$ signal. The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation.

Each port can generate an internal programmable serial clock or accept an external serial clock.

ADSP-218xN series members provide up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, eight flags are programmable as inputs or outputs, and three flags are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) decrements every n processor cycle, where n is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

ADSP-218xN series members incorporate two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Following is a brief list of the capabilities of the ADSP-218xN SPORTs. For additional information on Serial Ports, refer to the *ADSP-218x DSP Hardware Reference*.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulsewidths and timings.
- SPORTs support serial data word lengths from 3 bits to 16 bits and provide optional A-law and μ-law companding, according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24 word or 32-word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts ($\overline{IRQ0}$ and $\overline{IRQ1}$) and the FI and FO signals. The internally generated serial clock may still be used in this configuration.

Table 3. Interrupt Priority and Interrupt Vector Addresses

Source Of Interrupt	Interrupt Vector Address (Hex)
Reset (or Power-Up with PUCR = 1)	0x0000 (Highest Priority)
Power-Down (Nonmaskable)	0x002C
$\overline{\text{IRQ2}}$	0x0004
$\overline{\text{IRQL1}}$	0x0008
$\overline{\text{IRQL0}}$	0x000C
SPORT0 Transmit	0x0010
SPORT0 Receive	0x0014
$\overline{\text{IRQE}}$	0x0018
BDMA Interrupt	0x001C
SPORT1 Transmit or $\overline{\text{IRQ1}}$	0x0020
SPORT1 Receive or $\overline{\text{IRQ0}}$	0x0024
Timer	0x0028 (Lowest Priority)

Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially. Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The power-down interrupt is nonmaskable.

ADSP-218xN series members mask all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect serial port autobuffering or DMA transfers.

The interrupt control register, ICNTL, controls interrupt nesting and defines the $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ external interrupts to be either edge- or level-sensitive. The $\overline{\text{IRQE}}$ pin is an external edge-sensitive interrupt and can be forced and cleared. The $\overline{\text{IRQL0}}$ and $\overline{\text{IRQL1}}$ pins are external level sensitive interrupts.

The IFC register is a write-only register used to force and clear interrupts. On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are 12 levels deep to allow interrupt, loop, and subroutine nesting. The following instructions allow global enable or disable servicing of the interrupts (including power-down), regardless of the state of IMASK:

```
ENA INTS;
DIS INTS;
```

Disabling the interrupts does not affect serial port autobuffering or DMA. When the processor is reset, interrupt servicing is enabled.

LOW-POWER OPERATION

ADSP-218xN series members have three low-power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

Power-Down

ADSP-218xN series members have a low-power feature that lets the processor enter a very low-power dormant state through hardware or software control. Following is a brief list of power-down features. Refer to the *ADSP-218x DSP Hardware Reference*, "System Interface" chapter, for detailed information about the power-down feature.

- Quick recovery from power-down. The processor begins executing instructions in as few as 200 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the lowest power rating and 200 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits approximately 4096 CLKIN cycles for the crystal oscillator to start or stabilize), and letting the oscillator run to allow 200 CLKIN cycle start-up.
- Power-down is initiated by either the power-down pin ($\overline{\text{PWD}}$) or the software power-down force bit. Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt also can be used as a nonmaskable, edge-sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{\text{RESET}}$ pin also can be used to terminate power-down.
- Power-down acknowledge pin (PWDACK) indicates when the processor has entered power-down.

Idle

When the ADSP-218xN is in the Idle Mode, the processor waits indefinitely in a low-power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. In Idle mode IDMA, BDMA, and autobuffer cycle steals still occur.

Slow Idle

The IDLE instruction is enhanced on ADSP-218xN series members to let the processor's internal clock signal be slowed, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the IDLE instruction.

The format of the instruction is:

```
IDLE (n);
```

where n = 16, 32, 64, or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals,

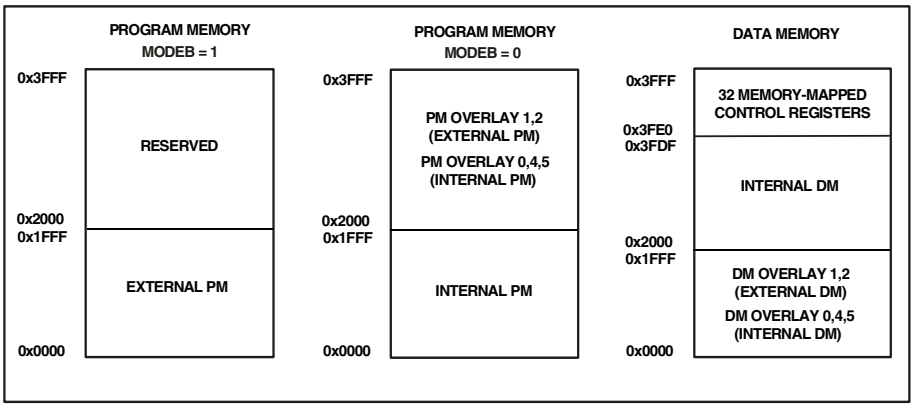


Figure 7. ADSP-2187 Memory Architecture

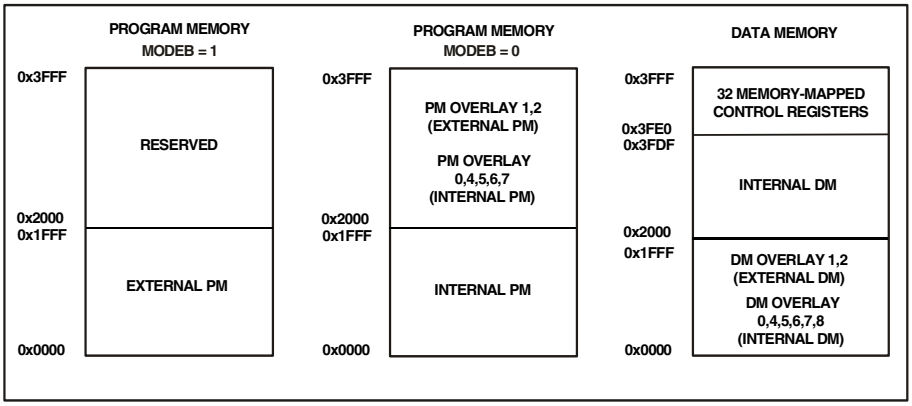


Figure 8. ADSP-2188 Memory Architecture

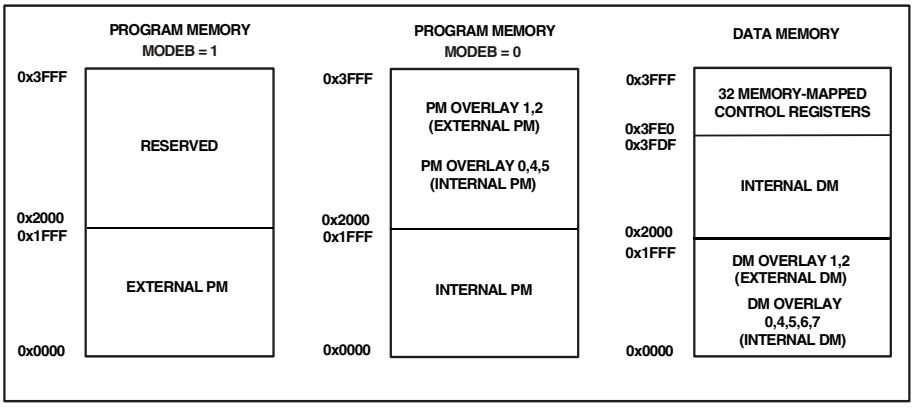


Figure 9. ADSP-2189 Memory Architecture

Program Memory

Program Memory (Full Memory Mode) is a 24-bit-wide space for storing both instruction opcodes and data. The member DSPs of this series have up to 48K words of Program Memory RAM on chip, and the capability of accessing up to two 8K external memory overlay spaces, using the external data bus.

IOWAIT0–3 as shown in Figure 10, which in combination with the wait state mode bit, specify up to 15 wait states to be automatically generated for each of four regions. The wait states act on address ranges, as shown in Table 6.

Note: In Full Memory Mode, all 2048 locations of I/O space are directly addressable. In Host Memory Mode, only address pin A0 is available; therefore, additional logic is required externally to achieve complete addressability of the 2048 I/O space locations.

Table 6. Wait States

Address Range	Wait State Register
0x000–0x1FF	IOWAIT0 and Wait State Mode Select Bit
0x200–0x3FF	IOWAIT1 and Wait State Mode Select Bit
0x400–0x5FF	IOWAIT2 and Wait State Mode Select Bit
0x600–0x7FF	IOWAIT3 and Wait State Mode Select Bit

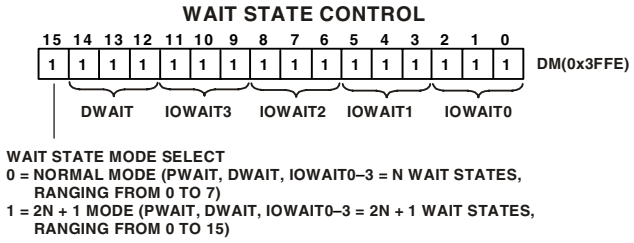


Figure 10. Wait State Control Register

Composite Memory Select

ADSP-218xN series members have a programmable memory select signal that is useful for generating memory select signals for memories mapped to more than one space. The $\overline{\text{CMS}}$ signal is generated to have the same timing as each of the individual memory select signals ($\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$) but can combine their functionality. Each bit in the CMSSEL register, when set, causes the $\overline{\text{CMS}}$ signal to be asserted when the selected memory select is asserted. For example, to use a 32K word memory to act as both program and data memory, set the $\overline{\text{PMS}}$ and $\overline{\text{DMS}}$ bits in the CMSSEL register and use the $\overline{\text{CMS}}$ pin to drive the chip select of the memory, and use either $\overline{\text{DMS}}$ or $\overline{\text{PMS}}$ as the additional address bit.

The $\overline{\text{CMS}}$ pin functions like the other memory select signals with the same timing and bus request logic. A 1 in the enable bit causes the assertion of the $\overline{\text{CMS}}$ signal at the same time as the selected memory select signal. All enable bits default to 1 at reset, except the $\overline{\text{BMS}}$ bit.

See Figure 11 and Figure 12 for illustration of the programmable flag and composite control register and the system control register.

Byte Memory Select

The ADSP-218xN's $\overline{\text{BMS}}$ disable feature combined with the $\overline{\text{CMS}}$ pin allows use of multiple memories in the byte memory space. For example, an EPROM could be attached to the $\overline{\text{BMS}}$

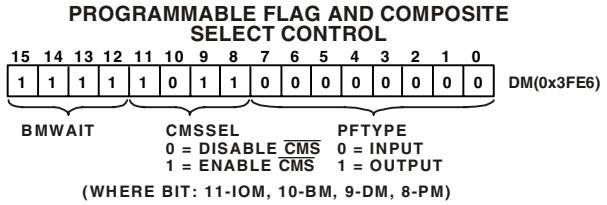


Figure 11. Programmable Flag and Composite Control Register

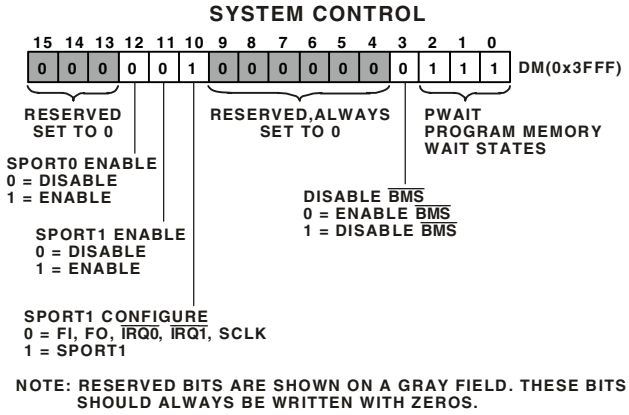


Figure 12. System Control Register

select, and a flash memory could be connected to $\overline{\text{CMS}}$. Because at reset $\overline{\text{BMS}}$ is enabled, the EPROM would be used for booting. After booting, software could disable $\overline{\text{BMS}}$ and set the $\overline{\text{CMS}}$ signal to respond to $\overline{\text{BMS}}$, enabling the flash memory.

Byte Memory

The byte memory space is a bidirectional, 8-bit-wide, external memory space used to store programs and data. Byte memory is accessed using the BDMA feature. The byte memory space consists of 256 pages, each of which is 16K × 8 bits.

The byte memory space on the ADSP-218xN series supports read and write operations as well as four different data formats. The byte memory uses data bits 15–8 for data. The byte memory uses data bits 23–16 and address bits 13–0 to create a 22-bit address. This allows up to a 4 megabit × 8 (32 megabit) ROM or RAM to be used without glue logic. All byte memory accesses are timed by the BMWAIT register and the wait state mode bit.

Byte Memory DMA (BDMA, Full Memory Mode)

The byte memory DMA controller (Figure 13) allows loading and storing of program instructions and data using the byte memory space. The BDMA circuit is able to access the byte memory space while the processor is operating normally and steals only one DSP cycle per 8-, 16-, or 24-bit word transferred.

($\overline{BR}$) signal. If the ADSP-218xN is not performing an external memory access, it responds to the active $\overline{BR}$ input in the following processor cycle by:

- Three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- Asserting the bus grant ($\overline{BG}$) signal, and
- Halting program execution.

If Go Mode is enabled, the ADSP-218xN will not halt program execution until it encounters an instruction that requires an external memory access.

If an ADSP-218xN series member is performing an external memory access when the external device asserts the $\overline{BR}$ signal, it will not three-state the memory interfaces nor assert the $\overline{BG}$ signal until the processor cycle after the access completes. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, re-enables the output drivers, and continues program execution from the point at which it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active.

The $\overline{BGH}$ pin is asserted when an ADSP-218xN series member requires the external bus for a memory or BDMA access, but is stopped. The other device can release the bus by deasserting bus request. Once the bus is released, the ADSP-218xN deasserts $\overline{BG}$ and $\overline{BGH}$ and executes the external memory access.

FLAG I/O PINS

ADSP-218xN series members have eight general-purpose programmable input/output flag pins. They are controlled by two memory-mapped registers. The PFTYPE register determines the direction, 1 = output and 0 = input. The PFDATA register is used to read and write the values on the pins. Data being read from a pin configured as an input is synchronized to the ADSP-218xN's clock. Bits that are programmed as outputs will read the value being output. The PF pins default to input during reset.

In addition to the programmable flags, ADSP-218xN series members have five fixed-mode flags, FI, FO, FL0, FL1, and FL2. FL0 to FL2 are dedicated output flags. FI and FO are available as an alternate configuration of SPORT1.

Note: Pins PF0, PF1, PF2, and PF3 are also used for device configuration during reset.

INSTRUCTION SET DESCRIPTION

The ADSP-218xN series assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 Family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to utilize on-chip memory and conform to the ADSP-218xN's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return, or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction, with up to two fetches or one write to processor memory space, during a single instruction cycle.

DEVELOPMENT SYSTEM

Analog Devices' wide range of software and hardware development tools supports the ADSP-218xN series. The DSP tools include an integrated development environment, an evaluation kit, and a serial port emulator.

VisualDSP++®† is an integrated development environment, allowing for fast and easy development, debug, and deployment. The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy-to-use assembler that is based on an algebraic syntax; an archiver (librarian/library builder); a linker; a PROM-splitter utility; a cycle-accurate, instruction-level simulator; a C compiler; and a C run-time library that includes DSP and mathematical functions.

Debugging both C and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C and assembly code (interleaved source and object information)
- Insert break points
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution

† VisualDSP++ is a registered trademark of Analog Devices, Inc.

- Fill and dump memory
- Source level debugging

The VisualDSP++ IDE lets programmers define and manage DSP software development. The dialog boxes and property pages let programmers configure and manage all of the ADSP-218xN development tools, including the syntax highlighting in the VisualDSP++ editor. This capability controls how the development tools process inputs and generate outputs.

The ADSP-2189M EZ-KIT Lite®† provides developers with a cost-effective method for initial evaluation of the powerful ADSP-218xN DSP family architecture. The ADSP-2189M EZ-KIT Lite includes a stand-alone ADSP-2189M DSP board supported by an evaluation suite of VisualDSP++. With this EZ-KIT Lite, users can learn about DSP hardware and software development and evaluate potential applications of the ADSP-218xN series. The ADSP-2189M EZ-KIT Lite provides an evaluation suite of the VisualDSP++ development environment with the C compiler, assembler, and linker. The size of the DSP executable that can be built using the EZ-KIT Lite tools is limited to 8K words.

The EZ-KIT Lite includes the following features:

- 75 MHz ADSP-2189M
- Full 16-Bit Stereo Audio I/O with AD73322 Codec
- RS-232 Interface
- EZ-ICE Connector for Emulator Control
- DSP Demonstration Programs
- Evaluation Suite of VisualDSP++

The ADSP-218x EZ-ICE®‡ Emulator provides an easier and more cost-effective method for engineers to develop and optimize DSP systems, shortening product development cycles for faster time-to-market. ADSP-218xN series members integrate on-chip emulation support with a 14-pin ICE-Port interface. This interface provides a simpler target board connection that requires fewer mechanical clearance considerations than other ADSP-2100 Family EZ-ICEs. ADSP-218xN series members need not be removed from the target system when using the EZ-ICE, nor are any adapters needed. Due to the small footprint of the EZ-ICE connector, emulation can be supported in final board designs.The EZ-ICE performs a full range of functions, including:

- In-target operation
- Up to 20 breakpoints
- Single-step or full-speed operation
- Registers and memory values can be examined and altered
- PC upload and download functions
- Instruction-level emulation of program booting and execution
- Complete assembly and disassembly of instructions
- C source-level debugging

Designing an EZ-ICE-Compatible System

ADSP-218xN series members have on-chip emulation support and an ICE-Port, a special set of pins that interface to the EZ-ICE. These features allow in-circuit emulation without replacing the target system processor by using only a 14-pin connection from the target system to the EZ-ICE. Target systems must have a 14-pin connector to accept the EZ-ICE's in-circuit probe, a 14-pin plug.

Note: The EZ-ICE uses the same V_{DD} voltage as the V_{DD} voltage used for V_{DDEXT}. Because the input pins of the ADSP-218xN series members are tolerant to input voltages up to 3.6 V, regardless of the value of V_{DDEXT}, the voltage setting for the EZ-ICE must not exceed 3.3 V.

Issuing the chip reset command during emulation causes the DSP to perform a full chip reset, including a reset of its memory mode. Therefore, it is vital that the mode pins are set correctly PRIOR to issuing a chip reset command from the emulator user interface. If a passive method of maintaining mode information is being used (as discussed in Setting Memory Mode on Page 5), it does not matter that the mode information is latched by an emulator reset. However, if the $\overline{\text{RESET}}$ pin is being used as a method of setting the value of the mode pins, the effects of an emulator reset must be taken into consideration.

One method of ensuring that the values located on the mode pins are those desired is to construct a circuit like the one shown in Figure 15. This circuit forces the value located on the Mode A pin to logic high, regardless of whether it is latched via the $\overline{\text{RESET}}$ or $\overline{\text{ERESET}}$ pin.

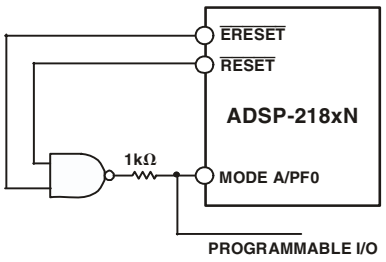


Figure 15. Mode A Pin/EZ-ICE Circuit

The ICE-Port interface consists of the following ADSP-218xN pins: $\overline{\text{EBR}}$, $\overline{\text{EINT}}$, EE, $\overline{\text{EBG}}$, ECLK, $\overline{\text{ERESET}}$, ELIN, $\overline{\text{EMS}}$, and ELOUT.

These ADSP-218xN pins must be connected only to the EZ-ICE connector in the target system. These pins have no function except during emulation, and do not require pull-up or pull-down resistors. The traces for these signals between the ADSP-218xN and the connector must be kept as short as possible, no longer than 3 inches.

The following pins are also used by the EZ-ICE: $\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{RESET}}$, and GND.

† EZ-KIT Lite is a registered trademark of Analog Devices, Inc.
‡ EZ-ICE is a registered trademark of Analog Devices, Inc.

Table 9. Common-Mode Pins (Continued)

Pin Name	No. of Pins	I/O	Function
V_{DDINT}	4	I	Internal V_{DD} (1.8 V) Power (BGA)
V_{DDEXT}	7	I	External V_{DD} (1.8 V, 2.5 V, or 3.3 V) Power (BGA)
GND	20	I	Ground (BGA)
EZ-Port	9	I/O	For Emulation Use

[1] Interrupt/Flag pins retain both functions concurrently. If IMASK is set to enable the corresponding interrupts, the DSP will vector to the appropriate interrupt vector address when the pin is asserted, either by external devices or set as a programmable flag.
[2] SPORT configuration determined by the DSP System Control Register. Software configurable.

MEMORY INTERFACE PINS

ADSP-218xN series members can be used in one of two modes: Full Memory Mode, which allows BDMA operation with full external overlay memory and I/O capability, or Host Mode, which allows IDMA operation with limited external addressing capabilities.

The operating mode is determined by the state of the Mode C pin during $\overline{\text{RESET}}$ and cannot be changed while the processor is running. Table 10 and Table 11 list the active signals at specific pins of the DSP during either of the two operating modes (Full Memory or Host). A signal in one table shares a pin with a signal from the other table, with the active signal determined by the mode that is set. For the shared pins and their alternate signals (e.g., A4/IAD3), refer to the package pinouts in Table 27 on Page 41 and Table 28 on Page 43.

Table 10. Full Memory Mode Pins (Mode C = 0)

Pin Name	No. of Pins	I/O	Function
A13–0	14	O	Address Output Pins for Program, Data, Byte, and I/O Spaces
D23–0	24	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces (8 MSBs are also used as Byte Memory Addresses.)

Table 11. Host Mode Pins (Mode C = 1)

Pin Name	No. of Pins	I/O	Function
IAD15–0	16	I/O	IDMA Port Address/Data Bus
A0	1	O	Address Pin for External I/O, Program, Data, or Byte Access[1]
D23–8	16	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces
$\overline{\text{IWR}}$	1	I	IDMA Write Enable
$\overline{\text{IRD}}$	1	I	IDMA Read Enable
IAL	1	I	IDMA Address Latch Pin
$\overline{\text{IS}}$	1	I	IDMA Select
$\overline{\text{IACK}}$	1	O	IDMA Port Acknowledge Configurable in Mode D; Open Drain

[1] In Host Mode, external peripheral addresses can be decoded using the A0, $\overline{\text{CMS}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, and $\overline{\text{IOMS}}$ signals.

TERMINATING UNUSED PINS

Table 12 shows the recommendations for terminating unused pins.

Table 12. Unused Pin Terminations

Pin Name[1]	I/O 3-State (Z)[2]	Reset State	Hi-Z[3] Caused By	Unused Configuration
XTAL	O	O		Float
CLKOUT	O	O		Float[4]
A13–1 or	O (Z)	Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
IAD12–0	I/O (Z)	Hi-Z	$\overline{\text{IS}}$	Float
A0	O (Z)	Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float

Table 12. Unused Pin Terminations (Continued)

Pin Name[1]	I/O 3-State (Z)[2]	Reset State	Hi-Z[3] Caused By	Unused Configuration
$\overline{\text{ERESET}}$	I	I		Float
$\overline{\text{EMS}}$	O	O		Float
$\overline{\text{EINT}}$	I	I		Float
ECLK	I	I		Float
ELIN	I	I		Float
ELOUT	O	O		Float

[1] CLKIN, $\overline{\text{RESET}}$, and PF3 – 0/Mode D – A are not included in this table because these pins must be used.
[2] All bidirectional pins have three-stated outputs. When the pin is configured as an output, the output is Hi-Z (high impedance) when inactive.
[3] Hi-Z = High Impedance.
[4] If the CLKOUT pin is not used, turn it OFF, using CLKODIS in SPORT0 autobuffer control register.
[5] If the Interrupt/Programmable Flag pins are not used, there are two options: Option 1: When these pins are configured as INPUTS at reset and function as interrupts and input flag pins, pull the pins High (inactive). Option 2: Program the unused pins as OUTPUTS, set them to 1 prior to enabling interrupts, and let pins float.

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

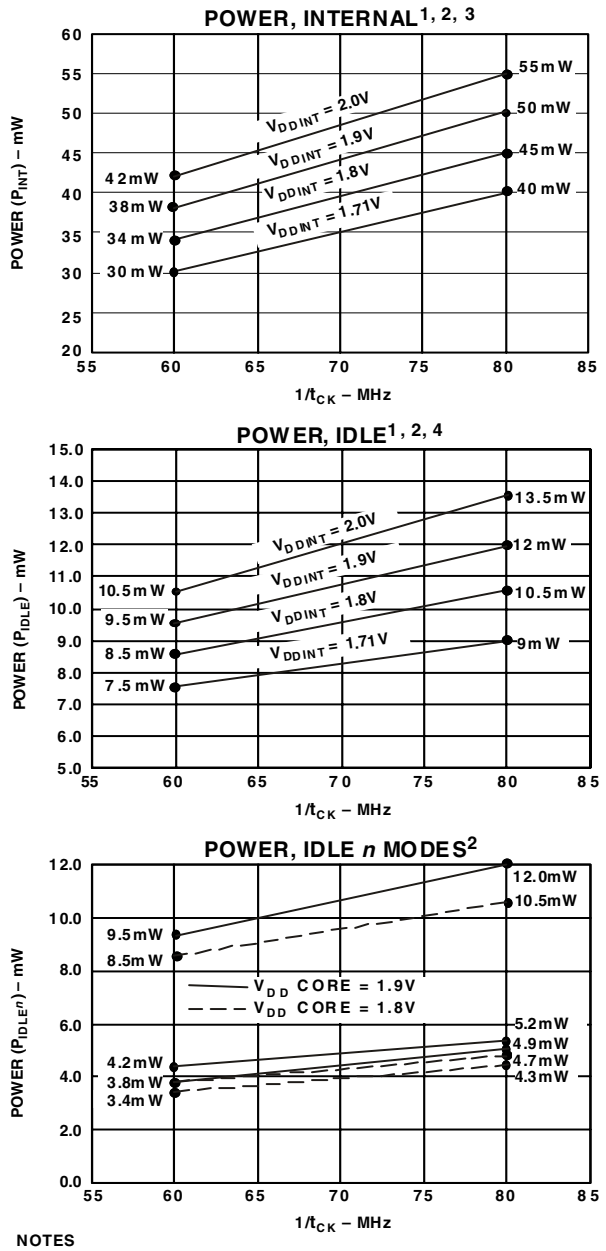
Parameter[1]	K Grade (Commercial)		B Grade (Industrial)		Unit
	Min	Max	Min	Max	
V_{DDINT}	1.71	1.89	1.8	2.0	V
V_{DDEXT}	1.71	3.6	1.8	3.6	V
V_{INPUT}[2]	V_{IL} = – 0.3	V_{IH} = + 3.6	V_{IL} = – 0.3	V_{IH} = + 3.6	V
T_{AMB}	0	70	–40	+85	°C

[1] Specifications subject to change without notice.

[2] The ADSP-218xN is 3.3 V tolerant (always accepts up to 3.6 V max V_{IH}), but voltage compliance (on outputs, V_{OH}) depends on the input V_{DDEXT}, because V_{OH} (max) approximately equals V_{DDEXT} (max). This 3.3 V tolerance applies to bidirectional pins (D23–D0, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A13–A1, PF7–PF0) and input-only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$).

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Hi-Level Input Voltage[2, 3]	@ V_{DDEXT} = 1.71 V to 2.0 V, V_{DDINT} = max	1.25			V
		@ V_{DDEXT} = 2.1 V to 3.6 V, V_{DDINT} = max	1.7			V
V_{IL}	Lo-Level Input Voltage[2, 3]	@ $V_{DDEXT} \leq$ 2.0 V, V_{DDINT} = min			0.6	V
		@ $V_{DDEXT} \geq$ 2.0 V, V_{DDINT} = min			0.7	V
V_{OH}	Hi-Level Output Voltage[2, 4, 5]	@ V_{DDEXT} = 1.71 V to 2.0 V, I_{OH} = – 0.5 mA	1.35			V
		@ V_{DDEXT} = 2.1 V to 2.9 V, I_{OH} = – 0.5 mA	2.0			V
		@ V_{DDEXT} = 3.0 V to 3.6 V, I_{OH} = – 0.5 mA	2.4			V
		@ V_{DDEXT} = 1.71 V to 3.6 V, I_{OH} = – 100 µA[6]	V_{DDEXT} – 0.3			V
V_{OL}	Lo-Level Output Voltage[2, 4, 5]	@ V_{DDEXT} = 1.71 V to 3.6 V, I_{OL} = 2.0 mA			0.4	V
I_{IH}	Hi-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 3.6 V			10	µA
I_{IL}	Lo-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 0 V			10	µA
I_{OZH}	Three-State Leakage Current[7]	@ V_{DDEXT} = max, V_{IN} = 3.6 V[8]			10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DDEXT} = max, V_{IN} = 0 V[8]			10	µA
I_{DD}	Supply Current (Idle)[9]	@ V_{DDINT} = 1.8 V, t_{CK} = 12.5 ns, T_{AMB} = 25°C		6		mA
I_{DD}	Supply Current (Dynamic)[10]	@ V_{DDINT} = 1.8 V, t_{CK} = 12.5 ns[11], T_{AMB} = 25°C		25		mA



NOTES

VALID FOR ALL TEMPERATURE GRADES.

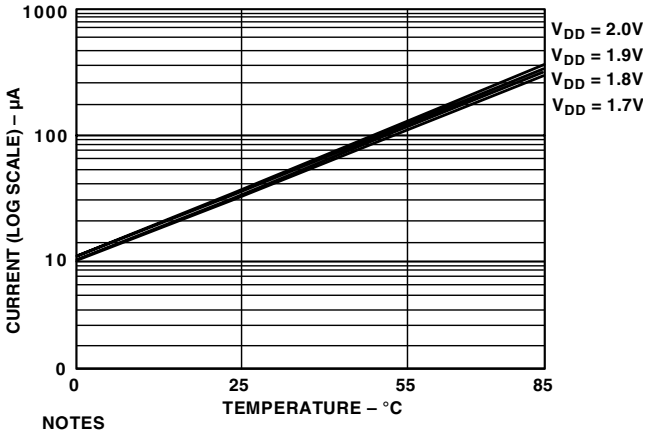
1 POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.

2 TYPICAL POWER DISSIPATION AT 1.8V OR 1.9V V_{DDINT} AND 25°C, EXCEPT WHERE SPECIFIED.

3 I_{DD} MEASUREMENT TAKEN WITH ALL INSTRUCTIONS EXECUTING FROM INTERNAL MEMORY. 50% OF THE INSTRUCTIONS ARE MULTIFUNCTION (TYPES 1, 4, 5, 12, 13, 14), 30% ARE TYPE 2 AND TYPE 6, AND 20% ARE IDLE INSTRUCTIONS.

4 IDLE REFERS TO STATE OF OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.

Figure 22. Power vs. Frequency



NOTES

1. REFLECTS ADSP-218xN OPERATION IN LOWEST POWER MODE. (SEE THE "SYSTEM INTERFACE" CHAPTER OF THE *ADSP-218x DSP HARDWARE REFERENCE* FOR DETAILS.)
2. CURRENT REFLECTS DEVICE OPERATING WITH NO INPUT LOADS.

Figure 23. Typical Power-Down Current

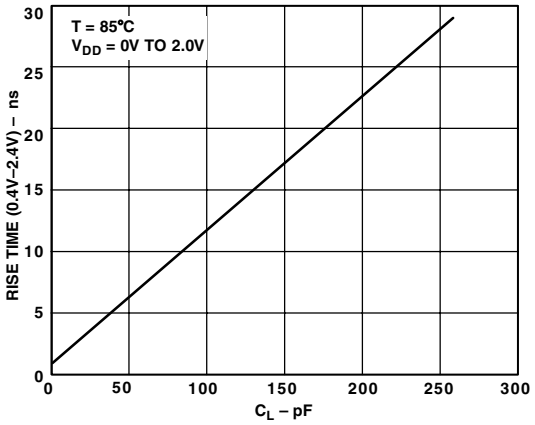


Figure 24. Typical Output Rise Time vs. Load Capacitance (at Maximum Ambient Operating Temperature)

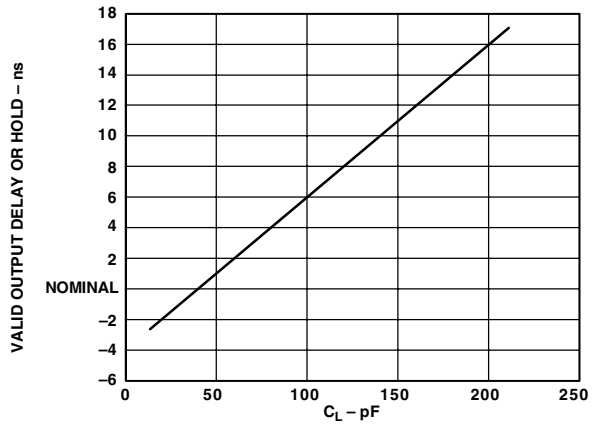


Figure 25. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

Clock Signals and Reset

Table 15. Clock Signals and Reset

Parameter		Min	Max	Unit
Timing Requirements:				
t_{CKI}	CLKIN Period	25	40	ns
t_{CKIL}	CLKIN Width Low	8		ns
t_{CKIH}	CLKIN Width High	8		ns
Switching Characteristics:				
t_{CKL}	CLKOUT Width Low	$0.5t_{CK} - 3$		ns
t_{CKH}	CLKOUT Width High	$0.5t_{CK} - 3$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	8	ns
Control Signals Timing Requirements:				
t_{RSP}	$\overline{\text{RESET}}$ Width Low	$5t_{CK}$[1]		ns
t_{MS}	Mode Setup before $\overline{\text{RESET}}$ High	7		ns
t_{MH}	Mode Hold after $\overline{\text{RESET}}$ High	5		ns

[1] Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles, assuming stable CLKIN (not including crystal oscillator start-up time).

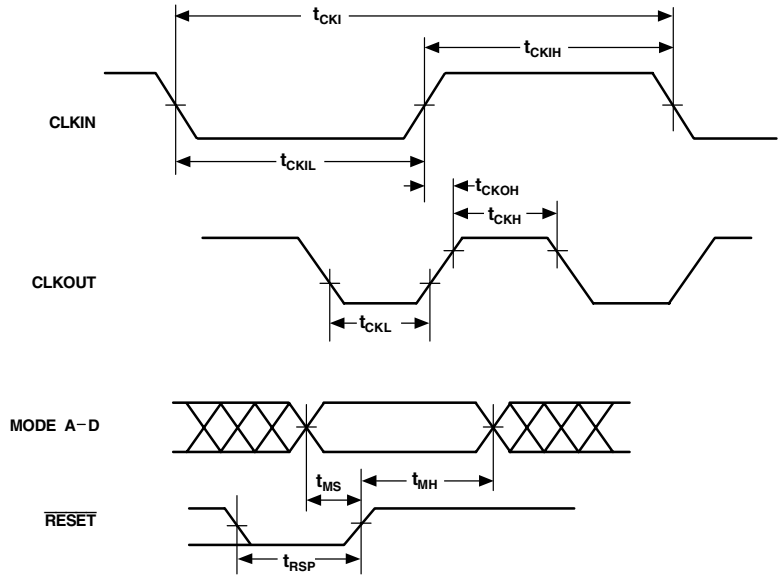


Figure 26. Clock Signals and Reset

Memory Read

Table 18. Memory Read

Parameter		Min	Max	Unit
Timing Requirements:				
t_{RDD}	$\overline{RD}$ Low to Data Valid[1]		$0.5t_{CK} - 5 + w$	ns
t_{AA}	A13–0, $\overline{xMS}$ to Data Valid[2]		$0.75t_{CK} - 6 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristics:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 3 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 2$	$0.25t_{CK} + 4$	ns
t_{ASR}	A13–0, $\overline{xMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 3$		ns
t_{RDA}	A13–0, $\overline{xMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 3$		ns

[1] w = wait states 3 t_{CK}.
[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

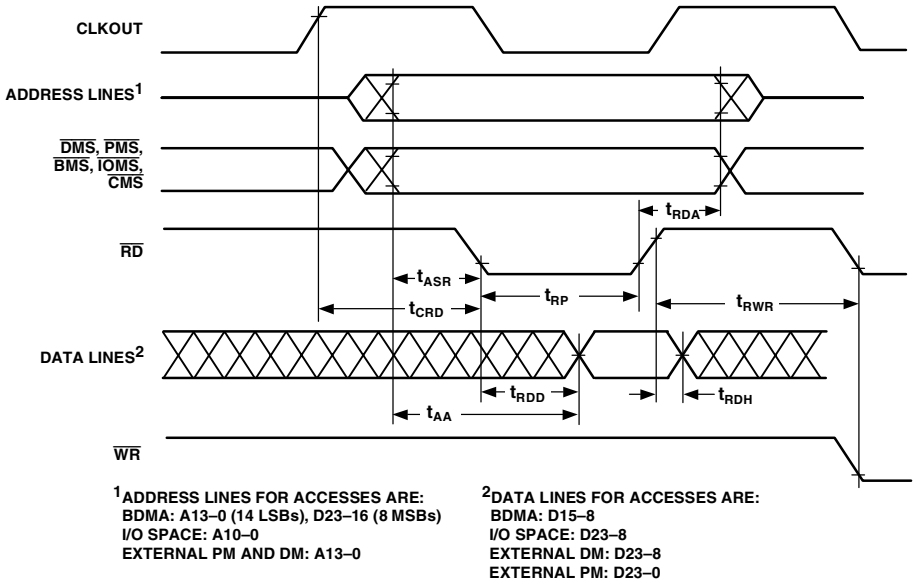


Figure 29. Memory Read

Memory Write

Table 19. Memory Write

Parameter		Min	Max	Unit
Switching Characteristics:				
t_{DW}	Data Setup before $\overline{WR}$ High[1]	$0.5t_{CK}$– 4 + w		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK}$ – 1		ns
t_{WP}	$\overline{WR}$ Pulse Width	$0.5t_{CK}$ – 3 + w		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A13–0, $\overline{xMS}$ Setup before $\overline{WR}$ Low[2]	$0.25t_{CK}$ – 3		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK}$ – 3		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK}$ – 2	$0.25t_{CK}$ + 4	ns
t_{AW}	A13–0, $\overline{xMS}$ Setup before $\overline{WR}$ Deasserted	$0.75t_{CK}$ – 5 + w		ns
t_{WRA}	A13–0, $\overline{xMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK}$ – 1		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK}$ – 3		ns

[1] w = wait states 3 t_{CK}.
[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

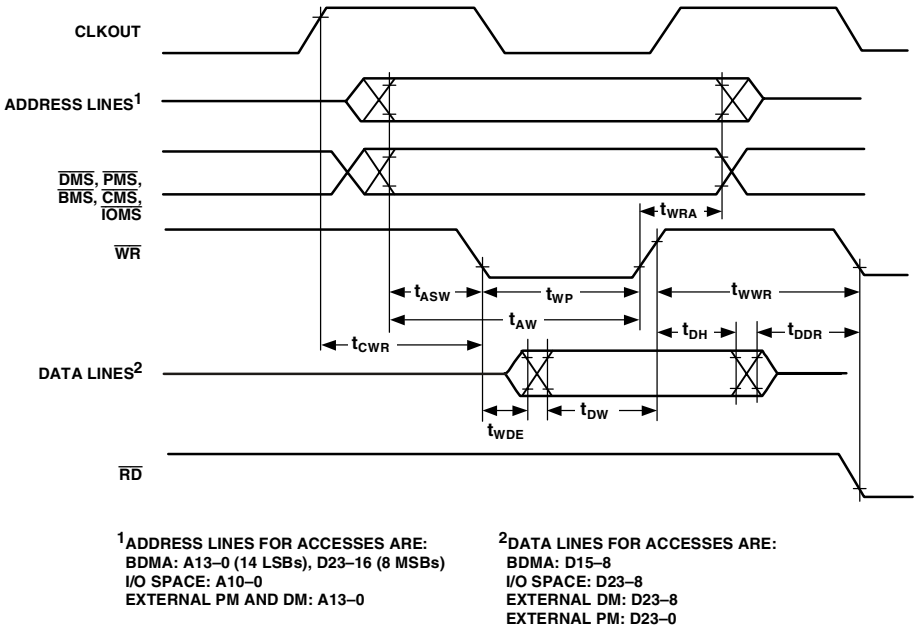


Figure 30. Memory Write

Serial Ports

Table 20. Serial Ports

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SCK}	SCLK Period	30		ns
t_{SCS}	DR/TFS/RFS Setup Before SCLK Low	4		ns
t_{SCH}	DR/TFS/RFS Hold After SCLK Low	7		ns
t_{SCP}	SCLKIN Width	12		ns
Switching Characteristics:				
t_{CC}	CLKOUT High to SCLKOUT	$0.25t_{CK}$	$0.25t_{CK} + 6$	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		7	ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		7	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS (Alt) to DT Enable	0		ns
t_{TDV}	TFS (Alt) to DT Valid		7	ns
t_{SCDD}	SCLK High to DT Disable		7	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		7	ns

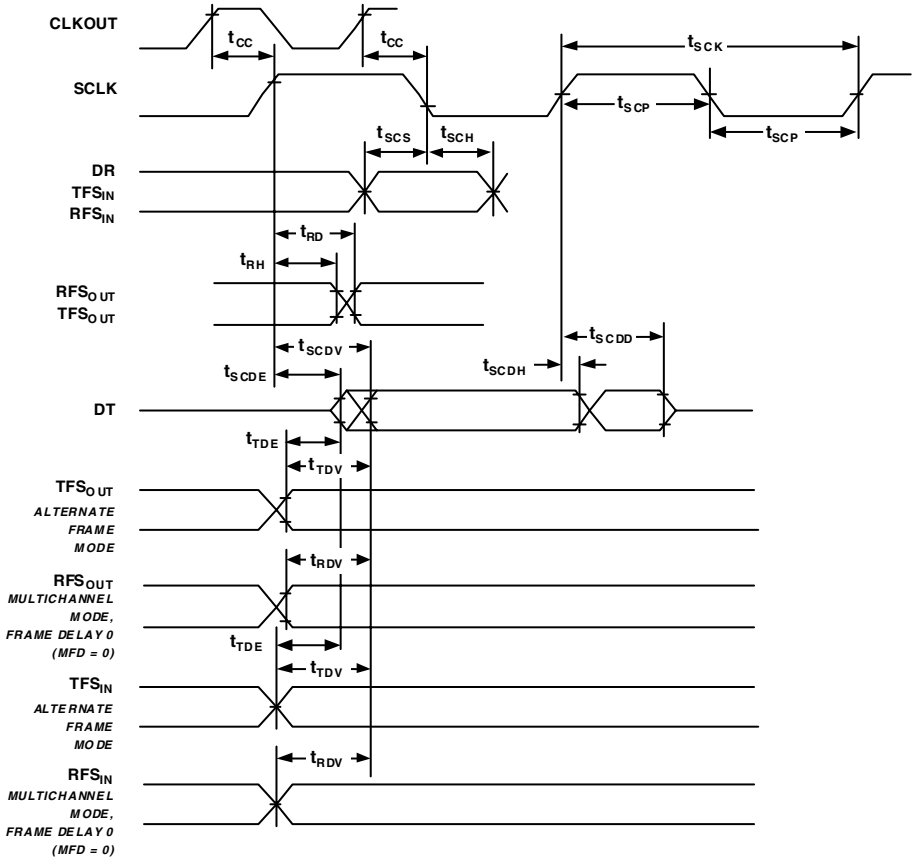


Figure 31. Serial Ports

IDMA Write, Short Write Cycle

Table 22. IDMA Write, Short Write Cycle

Parameter		Min	Max	Unit
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low Before Start of Write[1]	0		ns
t_{IWP}	Duration of Write[1, 2]	10		ns
t_{IDSU}	IAD15–0 Data Setup Before End of Write[2, 3, 4]	3		ns
t_{IDH}	IAD15–0 Data Hold After End of Write[2, 3, 4]	2		ns
Switching Characteristic:				
t_{IKHW}	Start of Write to $\overline{IACK}$ High		10	ns

[1] Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2] End of Write = $\overline{IS}$ High or $\overline{IWR}$ High.
[3] If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[4] If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.

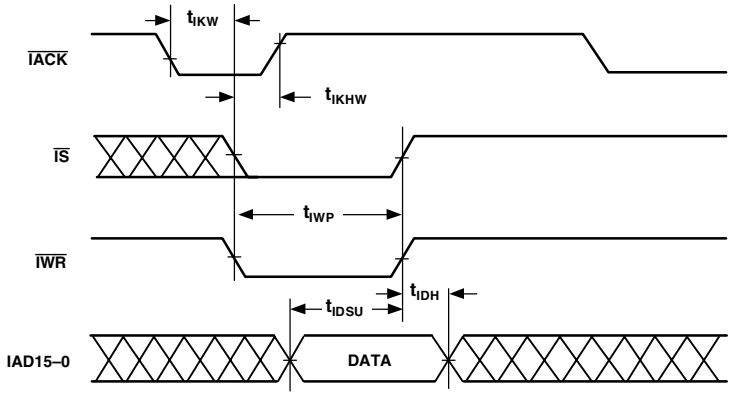


Figure 33. IDMA Write, Short Write Cycle

IDMA Read, Short Read Cycle

Table 25. IDMA Read, Short Read Cycle

Parameter[1, 2]		Min	Max	Unit
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low Before Start of Read[3]	0		ns
t_{IRP1}	Duration of Read (DM/PM1)[4]	10	$2t_{CK} - 5$	ns
t_{IRP2}	Duration of Read (PM2)[5]	10	$t_{CK} - 5$	ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High After Start of Read[3]		10	ns
t_{IKDH}	IAD15–0 Data Hold After End of Read[6]	0		ns
t_{IKDD}	IAD15–0 Data Disabled After End of Read[6]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled After Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid After Start of Read		10	ns

[1] Short Read Only must be disabled in the IDMA overlay memory mapped register. This mode is disabled by clearing (=0) Bit 14 of the IDMA overlay register, and is disabled by default upon reset.
[2] Consider using the Short Read Only mode, instead, because Short Read mode is not applicable at high clock frequencies.
[3] Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[4] DM Read or first half of PM Read.
[5] Second half of PM Read.
[6] End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

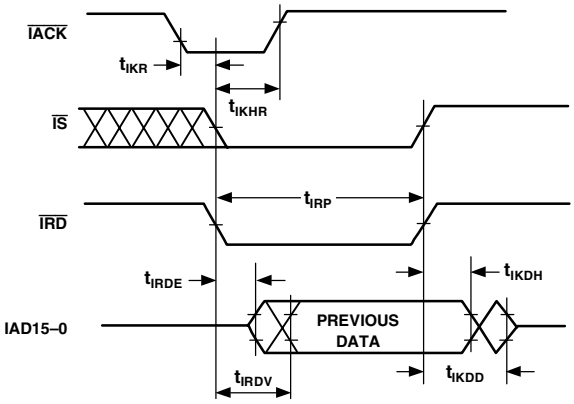


Figure 36. IDMA Read, Short Read Cycle

Table 27. LQFP Package Pinout

Pin No.	Pin Name
1	A4/**IAD3**
2	A5/**IAD4**
3	GND
4	A6/**IAD5**
5	A7/**IAD6**
6	A8/**IAD7**
7	A9/**IAD8**
8	A10/**IAD9**
9	A11/**IAD10**
10	A12/**IAD11**
11	A13/**IAD12**
12	GND
13	CLKIN
14	XTAL
15	V_{DDEXT}
16	CLKOUT
17	GND
18	V_{DDINT}
19	$\overline{WR}$
20	$\overline{RD}$
21	$\overline{BMS}$
22	$\overline{DMS}$
23	$\overline{PMS}$
24	$\overline{IOMS}$
25	$\overline{CMS}$
26	$\overline{IRQE}$ + PF4
27	$\overline{IRQL0}$ + PF5
28	GND
29	$\overline{IRQL1}$ + PF6
30	$\overline{IRQ2}$ + PF7
31	DT0
32	TFS0
33	RFS0
34	DR0
35	SCLK0
36	V_{DDEXT}
37	DT1/FO
38	TFS1/$\overline{IRQ1}$
39	RFS1/$\overline{IRQ0}$
40	DR1/FI
41	GND
42	SCLK1
43	$\overline{ERESET}$
44	$\overline{RESET}$
45	$\overline{EMS}$
46	EE
47	ECLK
48	ELOUT
49	ELIN
50	$\overline{EINT}$

Table 27. LQFP Package Pinout (Continued)

Pin No.	Pin Name
51	$\overline{EBR}$
52	$\overline{BR}$
53	$\overline{EBG}$
54	$\overline{BG}$
55	D0/**IAD13**
56	D1/**IAD14**
57	D2/**IAD15**
58	D3/$\overline{\textbf{IACK}}$
59	V_{DDINT}
60	GND
61	D4/$\overline{\textbf{IS}}$
62	D5/**IAL**
63	D6/$\overline{\textbf{IRD}}$
64	D7/$\overline{\textbf{IWR}}$
65	D8
66	GND
67	V_{DDEXT}
68	D9
69	D10
70	D11
71	GND
72	D12
73	D13
74	D14
75	D15
76	D16
77	D17
78	D18
79	D19
80	GND
81	D20
82	D21
83	D22
84	D23
85	FL2
86	FL1
87	FL0
88	PF3 [Mode D]
89	PF2 [Mode C]
90	V_{DDEXT}
91	$\overline{PWD}$
92	GND
93	PF1 [Mode B]
94	PF0 [Mode A]
95	$\overline{BGH}$
96	PWDACK
97	A0
98	A1/**IAD0**
99	A2/**IAD1**
100	A3/**IAD2**

ORDERING GUIDE

Model	Temperature Range[1]	Instruction Rate (MHz)	Package Description	Package Option
ADSP-2184NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2184NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2184NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2184NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2184NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2185NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2185NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2185NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2185NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2185NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2185NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2186NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2186NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2186NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2186NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2186NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2186NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2187NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2187NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2187NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2187NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2187NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2187NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2188NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2188NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2188NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2188NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2188NKCAZ-320[2]	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2188NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2188NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2189NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2189NBCAZ-320[2]	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2189NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2189NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2189NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2189NKCAZ-320[2]	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2189NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2189NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1

[1] Ranges shown represent ambient temperature.
[2] Z = Pb-free part.

C02666-0-8/06(A)