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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, Serial Port
Clock Rate	80MHz
Non-Volatile Memory	External
On-Chip RAM	192kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.90V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA, CSPBGA
Supplier Device Package	144-CSPBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2189nbcaz-320

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting ADSP-218xN series members to fetch two operands in a single cycle, one from program memory and one from data memory. ADSP-218xN series members can fetch an operand from program memory and the next instruction in the same cycle.

In lieu of the address and data bus for external memory connection, ADSP-218xN series members may be configured for 16-bit Internal DMA port (IDMA port) connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSP's on-chip program and data RAM.

An interface to low-cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals ($\overline{BR}$, $\overline{BGH}$, and $\overline{BG}$). One execution mode (Go Mode) allows the ADSP-218xN to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

ADSP-218xN series members can respond to eleven interrupts. There can be up to six external interrupts (one edge-sensitive, two level-sensitive, and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORT), the BDMA port, and the power-down circuitry. There is also a master $\overline{RESET}$ signal. The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation.

Each port can generate an internal programmable serial clock or accept an external serial clock.

ADSP-218xN series members provide up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, eight flags are programmable as inputs or outputs, and three flags are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) decrements every n processor cycle, where n is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

ADSP-218xN series members incorporate two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Following is a brief list of the capabilities of the ADSP-218xN SPORTs. For additional information on Serial Ports, refer to the *ADSP-218x DSP Hardware Reference*.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulsewidths and timings.
- SPORTs support serial data word lengths from 3 bits to 16 bits and provide optional A-law and μ-law companding, according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24 word or 32-word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts ($\overline{IRQ0}$ and $\overline{IRQ1}$) and the FI and FO signals. The internally generated serial clock may still be used in this configuration.

MODES OF OPERATION

The ADSP-218xN series modes of operation appear in Table 2.

Table 2. Modes of Operation

Mode D	Mode C	Mode B	Mode A	Booting Method
X	0	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Full Memory Mode.[1]
X	0	1	0	No automatic boot operations occur. Program execution starts at external memory location 0. Chip is configured in Full Memory Mode. BDMA can still be used, but the processor does not automatically use or wait for these operations.
0	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode. $\overline{\text{IACK}}$ has active pull-down. (Requires additonal hardware.)
0	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until the host writes to internal program memory location 0. Chip is configured in Host Mode. $\overline{\text{IACK}}$ has active pull-down.[1]
1	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode; $\overline{\text{IACK}}$ requires external pull-down. (Requires additonal hardware.)
1	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until the host writes to internal program memory location 0. Chip is configured in Host Mode. $\overline{\text{IACK}}$ requires external pull-down.[1]

[1] Considered as standard operating settings. Using these configurations allows for easier design and better memory management.

Setting Memory Mode

Memory Mode selection for the ADSP-218xN series is made during chip reset through the use of the Mode C pin. This pin is multiplexed with the DSP's PF2 pin, so care must be taken in how the mode selection is made. The two methods for selecting the value of Mode C are active and passive.

Passive Configuration

Passive Configuration involves the use of a pull-up or pull-down resistor connected to the Mode C pin. To minimize power consumption, or if the PF2 pin is to be used as an output in the DSP application, a weak pull-up or pull-down resistance, on the order of 10 kΩ, can be used. This value should be sufficient to pull the pin to the desired level and still allow the pin to operate as a programmable flag output without undue strain on the processor's output driver. For minimum power consumption during power-down, reconfigure PF2 to be an input, as the pull-up or pull-down resistance will hold the pin in a known state, and will not switch.

Active Configuration

Active Configuration involves the use of a three-statable external driver connected to the Mode C pin. A driver's output enable should be connected to the DSP's $\overline{\text{RESET}}$ signal such that it only drives the PF2 pin when $\overline{\text{RESET}}$ is active (low). When $\overline{\text{RESET}}$ is deasserted, the driver should be three-state, thus allowing full use of the PF2 pin as either an input or output. To minimize power consumption during power-down, configure the programmable flag as an output when connected to a three-stated buffer. This ensures that the pin will be held at a constant level, and will not oscillate should the three-state driver's level hover around the logic switching point.

IDMA ACK Configuration

Mode D = 0 and in host mode: $\overline{\text{IACK}}$ is an active, driven signal and cannot be "wire-OR'ed." Mode D = 1 and in host mode: $\overline{\text{IACK}}$ is an open drain and requires an external pull-down, but multiple $\overline{\text{IACK}}$ pins can be "wire-OR'ed" together.

INTERRUPTS

The interrupt controller allows the processor to respond to the eleven possible interrupts and reset with minimum overhead. ADSP-218xN series members provide four dedicated external interrupt input pins: $\overline{\text{IRQ2}}$, $\overline{\text{IRQL0}}$, $\overline{\text{IRQL1}}$, and $\overline{\text{IRQE}}$ (shared with the PF7–4 pins). In addition, SPORT1 may be reconfigured for $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, FI, and FO, for a total of six external interrupts. The ADSP-218xN also supports internal interrupts from the timer, the byte DMA port, the two serial ports, software, and the power-down control circuit. The interrupt levels are internally prioritized and individually maskable (except power-down and reset). The $\overline{\text{IRQ2}}$, $\overline{\text{IRQ0}}$, and $\overline{\text{IRQ1}}$ input pins can be programmed to be either level- or edge-sensitive. $\overline{\text{IRQL0}}$ and $\overline{\text{IRQL1}}$ are level-sensitive and $\overline{\text{IRQE}}$ is edge-sensitive. The priorities and vector addresses of all interrupts are shown in Table 3.

Table 3. Interrupt Priority and Interrupt Vector Addresses

Source Of Interrupt	Interrupt Vector Address (Hex)
Reset (or Power-Up with PUCR = 1)	0x0000 (Highest Priority)
Power-Down (Nonmaskable)	0x002C
$\overline{\text{IRQ2}}$	0x0004
$\overline{\text{IRQL1}}$	0x0008
$\overline{\text{IRQL0}}$	0x000C
SPORT0 Transmit	0x0010
SPORT0 Receive	0x0014
$\overline{\text{IRQE}}$	0x0018
BDMA Interrupt	0x001C
SPORT1 Transmit or $\overline{\text{IRQ1}}$	0x0020
SPORT1 Receive or $\overline{\text{IRQ0}}$	0x0024
Timer	0x0028 (Lowest Priority)

Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially. Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The power-down interrupt is nonmaskable.

ADSP-218xN series members mask all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect serial port autobuffering or DMA transfers.

The interrupt control register, ICNTL, controls interrupt nesting and defines the $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ external interrupts to be either edge- or level-sensitive. The $\overline{\text{IRQE}}$ pin is an external edge-sensitive interrupt and can be forced and cleared. The $\overline{\text{IRQL0}}$ and $\overline{\text{IRQL1}}$ pins are external level sensitive interrupts.

The IFC register is a write-only register used to force and clear interrupts. On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are 12 levels deep to allow interrupt, loop, and subroutine nesting. The following instructions allow global enable or disable servicing of the interrupts (including power-down), regardless of the state of IMASK:

```
ENA INTS;
DIS INTS;
```

Disabling the interrupts does not affect serial port autobuffering or DMA. When the processor is reset, interrupt servicing is enabled.

LOW-POWER OPERATION

ADSP-218xN series members have three low-power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

Power-Down

ADSP-218xN series members have a low-power feature that lets the processor enter a very low-power dormant state through hardware or software control. Following is a brief list of power-down features. Refer to the *ADSP-218x DSP Hardware Reference*, "System Interface" chapter, for detailed information about the power-down feature.

- Quick recovery from power-down. The processor begins executing instructions in as few as 200 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the lowest power rating and 200 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits approximately 4096 CLKIN cycles for the crystal oscillator to start or stabilize), and letting the oscillator run to allow 200 CLKIN cycle start-up.
- Power-down is initiated by either the power-down pin ($\overline{\text{PWD}}$) or the software power-down force bit. Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt also can be used as a nonmaskable, edge-sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{\text{RESET}}$ pin also can be used to terminate power-down.
- Power-down acknowledge pin (PWDACK) indicates when the processor has entered power-down.

Idle

When the ADSP-218xN is in the Idle Mode, the processor waits indefinitely in a low-power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. In Idle mode IDMA, BDMA, and autobuffer cycle steals still occur.

Slow Idle

The IDLE instruction is enhanced on ADSP-218xN series members to let the processor's internal clock signal be slowed, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the IDLE instruction.

The format of the instruction is:

```
IDLE (n);
```

where n = 16, 32, 64, or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals,

such as SCLK, CLKOUT, and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard IDLE instruction.

When the IDLE (n) instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts. The one-cycle response time of the standard idle state is increased by n, the clock divisor. When an enabled interrupt is received, ADSP-218xN series members remain in the idle state for up to a maximum of n processor cycles (n = 16, 32, 64, or 128) before resuming normal operation.

When the IDLE (n) instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of n processor cycles).

SYSTEM INTERFACE

Figure 2 shows typical basic system configurations with the ADSP-218xN series, two serial devices, a byte-wide EPROM, and optional external program and data overlay memories (mode-selectable). Programmable wait state generation allows the processor to connect easily to slow peripheral devices. ADSP-218xN series members also provide four external interrupts and two serial ports or six external interrupts and one serial port. Host Memory Mode allows access to the full external data bus, but limits addressing to a single address bit (A0). Through the use of external hardware, additional system peripherals can be added in this mode to generate and latch address signals.

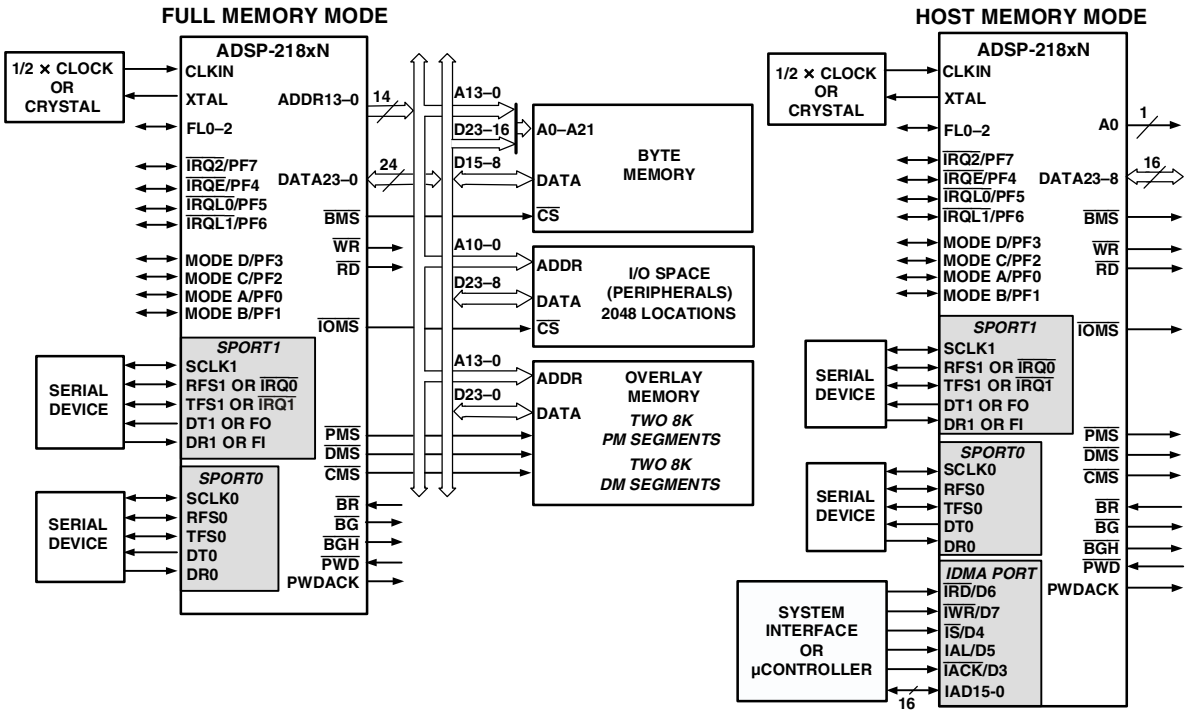

Figure 2. Basic System Interface

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter[1]	K Grade (Commercial)		B Grade (Industrial)		Unit
	Min	Max	Min	Max	
V_{DDINT}	1.71	1.89	1.8	2.0	V
V_{DDEXT}	1.71	3.6	1.8	3.6	V
V_{INPUT}[2]	V_{IL} = – 0.3	V_{IH} = + 3.6	V_{IL} = – 0.3	V_{IH} = + 3.6	V
T_{AMB}	0	70	–40	+85	°C

[1] Specifications subject to change without notice.

[2] The ADSP-218xN is 3.3 V tolerant (always accepts up to 3.6 V max V_{IH}), but voltage compliance (on outputs, V_{OH}) depends on the input V_{DDEXT}, because V_{OH} (max) approximately equals V_{DDEXT} (max). This 3.3 V tolerance applies to bidirectional pins (D23–D0, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A13–A1, PF7–PF0) and input-only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$).

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Hi-Level Input Voltage[2, 3]	@ V_{DDEXT} = 1.71 V to 2.0 V, V_{DDINT} = max	1.25			V
		@ V_{DDEXT} = 2.1 V to 3.6 V, V_{DDINT} = max	1.7			V
V_{IL}	Lo-Level Input Voltage[2, 3]	@ $V_{DDEXT} \leq$ 2.0 V, V_{DDINT} = min			0.6	V
		@ $V_{DDEXT} \geq$ 2.0 V, V_{DDINT} = min			0.7	V
V_{OH}	Hi-Level Output Voltage[2, 4, 5]	@ V_{DDEXT} = 1.71 V to 2.0 V, I_{OH} = – 0.5 mA	1.35			V
		@ V_{DDEXT} = 2.1 V to 2.9 V, I_{OH} = – 0.5 mA	2.0			V
		@ V_{DDEXT} = 3.0 V to 3.6 V, I_{OH} = – 0.5 mA	2.4			V
		@ V_{DDEXT} = 1.71 V to 3.6 V, I_{OH} = – 100 µA[6]	V_{DDEXT} – 0.3			V
V_{OL}	Lo-Level Output Voltage[2, 4, 5]	@ V_{DDEXT} = 1.71 V to 3.6 V, I_{OL} = 2.0 mA			0.4	V
I_{IH}	Hi-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 3.6 V			10	µA
I_{IL}	Lo-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 0 V			10	µA
I_{OZH}	Three-State Leakage Current[7]	@ V_{DDEXT} = max, V_{IN} = 3.6 V[8]			10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DDEXT} = max, V_{IN} = 0 V[8]			10	µA
I_{DD}	Supply Current (Idle)[9]	@ V_{DDINT} = 1.8 V, t_{CK} = 12.5 ns, T_{AMB} = 25°C		6		mA
I_{DD}	Supply Current (Dynamic)[10]	@ V_{DDINT} = 1.8 V, t_{CK} = 12.5 ns[11], T_{AMB} = 25°C		25		mA

Parameter[1]	Description	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Supply Current (Idle)[9]	@ V_{DDINT} = 1.9 V, t_{CK} = 12.5 ns, T_{AMB} = 25°C		6.5		mA
I_{DD}	Supply Current (Dynamic)[10]	@ V_{DDINT} = 1.9 V, t_{CK} = 12.5 ns[11], T_{AMB} = 25°C		26		mA
I_{DD}	Supply Current (Power-Down)[12]	@ V_{DDINT} = 1.8 V, T_{AMB} = 25°C in Lowest Power Mode		100		µA
C_I	Input Pin Capacitance[3, 6]	@ V_{IN} = 1.8 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C			8	pF
C_O	Output Pin Capacitance[6, 7, 12, 13]	@ V_{IN} = 1.8 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C			8	pF

[1] Specifications subject to change without notice.
[2] Bidirectional pins: D23–0, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A13–1, PF7–0.
[3] Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.
[4] Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2–FL0, $\overline{\text{BGH}}$.
[5] Although specified for TTL outputs, all ADSP-218xN outputs are CMOS-compatible and will drive to V_{DDEXT} and GND, assuming no dc loads.
[6] Guaranteed but not tested.
[7] Three-statable pins: A13–A1, D23–D0, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1, PF7–PF0.
[8] 0 V on $\overline{\text{BR}}$.
[9] Idle refers to ADSP-218xN state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.
[10] I_{DD} measurement taken with all instructions executing from internal memory. 50% of the instructions are multifunction (Types 1, 4, 5, 12, 13, 14), 30% are Type 2 and Type 6, and 20% are idle instructions.
[11] V_{IN} = 0 V and 3 V. For typical values for supply currents, refer to *Power Dissipation* section.
[12] See *ADSP-218x DSP Hardware Reference* for details.
[13] Output pin capacitance is the capacitive load for any three-stated output pin.

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
Internal Supply Voltage (V_{DDINT})[1]	–0.3 V to +2.2 V
External Supply Voltage (V_{DDEXT})	–0.3 V to +4.0 V
Input Voltage[2]	–0.5 V to +4.0 V
Output Voltage Swing[3]	–0.5 V to V_{DDEXT} +0.5 V
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C

[1] Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2] Applies to Bidirectional pins (D23–0, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A13–1, PF7–0) and Input only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$).
[3] Applies to Output pins ($\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2–0, $\overline{\text{BGH}}$).

ESD SENSITIVITY

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-218xN features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

This section contains timing information for the DSP's external signals.

General Notes

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, parameters cannot be added up meaningfully to derive longer times.

Timing Notes

Switching characteristics specify how the processor changes its signals. Designers have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell what the processor will do in a given circumstance. Switching characteristics can also be used to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Frequency Dependency For Timing Specifications

t_{CK} is defined as 0.5 t_{CKI}. The ADSP-218xN uses an input clock with a frequency equal to half the instruction rate. For example, a 40 MHz input clock (which is equivalent to 25 ns) yields a 12.5 ns processor cycle (equivalent to 80 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain the specification value.

Example: t_{CKH} = 0.5 t_{CK} – 2 ns = 0.5 (12.5 ns) – 2 ns = 4.25 ns

Output Drive Currents

Figure 21 shows typical I-V characteristics for the output drivers on the ADSP-218xN series.The curves represent the current drive capability of the output drivers as a function of output voltage.

Figure 23 shows the typical power-down supply current.

Capacitive Loading

Figure 24 and Figure 25 show the capacitive loading characteristics of the ADSP-218xN.

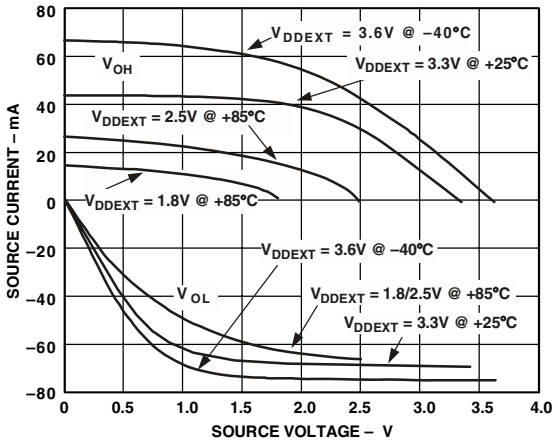

Figure 21. Typical Output Driver Characteristics for V_{DDEXT} at 3.6 V, 3.3 V, 2.5 V, and 1.8 V

Interrupts and Flags

Table 16. Interrupts and Flags

Parameter		Min	Max	Unit
Timing Requirements:				
t_{IFS}	$\overline{IRQx}$, FI, or PFx Setup before CLKOUT Low[1, 2, 3, 4]	$0.25t_{CK} + 10$		ns
t_{IFH}	$\overline{IRQx}$, FI, or PFx Hold after CLKOUT High[1, 2, 3, 4]	$0.25t_{CK}$		ns
Switching Characteristics:				
t_{FOH}	Flag Output Hold after CLKOUT Low[5]	$0.5t_{CK} - 5$		ns
t_{FOD}	Flag Output Delay from CLKOUT Low[5]		$0.5t_{CK} + 4$	ns

[1] If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to "Interrupt Controller Operation" in the *Program Control* chapter of the *ADSP-218x DSP Hardware Reference* for further information on interrupt servicing.)

[2] Edge-sensitive interrupts require pulse widths greater than 10 ns; level-sensitive interrupts must be held low until serviced.

[3] $\overline{IRQx}$ = $\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$, $\overline{IRQLE}$.

[4] PFx = PF0, PF1, PF2, PF3, PF4, PF5, PF6, PF7.

[5] Flag Outputs = PFx, FL0, FL1, FL2, FO.

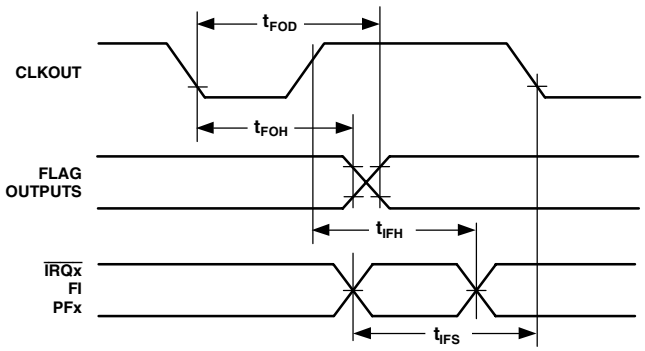

Figure 27. Interrupts and Flags

Bus Request–Bus Grant

Table 17. Bus Request–Bus Grant

Parameter		Min	Max	Unit
Timing Requirements:				
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	$0.25t_{CK} + 2$		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	$0.25t_{CK} + 8$		ns
Switching Characteristics:				
t_{SD}	CLKOUT High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable[2]		$0.25t_{CK} + 8$	ns
t_{SDB}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE}	$\overline{BG}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	$0.25t_{CK} - 3$		ns
t_{SDBH}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BGH}$ Low[3]	0		ns
t_{SEH}	$\overline{BGH}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable[3]	0		ns

[1] $\overline{BR}$ is an asynchronous signal. If $\overline{BR}$ meets the setup/hold requirements, it will be recognized during the current clock cycle; otherwise the signal will be recognized on the following cycle. Refer to the *ADSP-2100 Family User's Manual* for $\overline{BR}$/BG cycle relationships.

[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

[3] $\overline{BGH}$ is asserted when the bus is granted and the processor or BDMA requires control of the bus to continue.

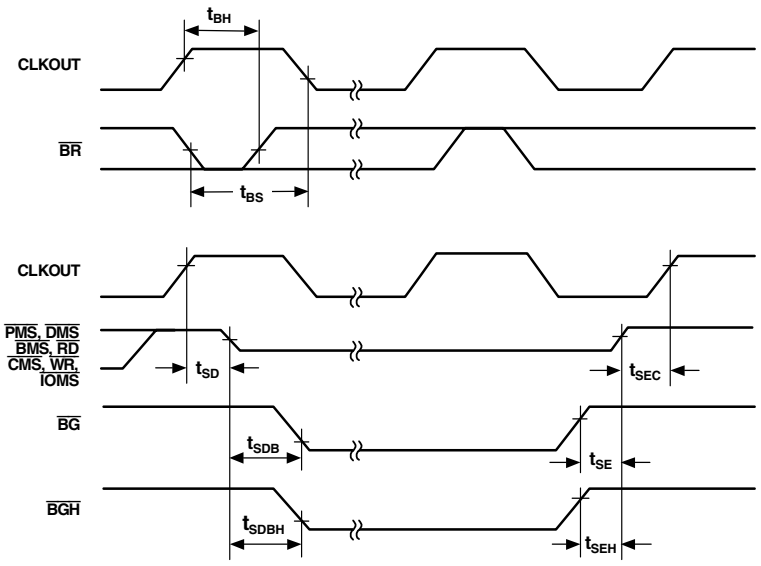

Figure 28. Bus Request–Bus Grant

Memory Read

Table 18. Memory Read

Parameter		Min	Max	Unit
Timing Requirements:				
t_{RDD}	$\overline{RD}$ Low to Data Valid[1]		$0.5t_{CK} - 5 + w$	ns
t_{AA}	A13–0, $\overline{xMS}$ to Data Valid[2]		$0.75t_{CK} - 6 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristics:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 3 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 2$	$0.25t_{CK} + 4$	ns
t_{ASR}	A13–0, $\overline{xMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 3$		ns
t_{RDA}	A13–0, $\overline{xMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 3$		ns

[1] w = wait states 3 t_{CK}.
[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

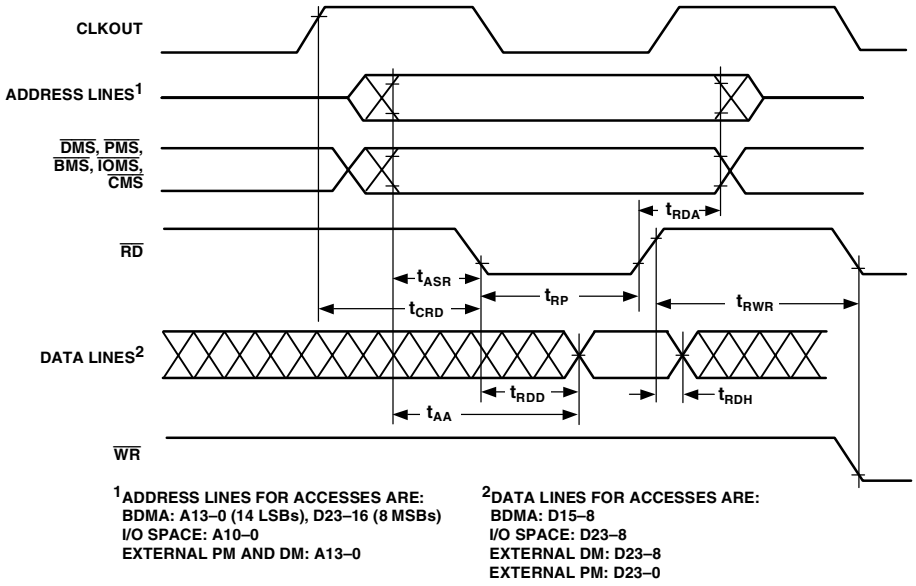

Figure 29. Memory Read

Memory Write

Table 19. Memory Write

Parameter		Min	Max	Unit
Switching Characteristics:				
t_{DW}	Data Setup before $\overline{WR}$ High[1]	$0.5t_{CK}$– 4 + w		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK}$ – 1		ns
t_{WP}	$\overline{WR}$ Pulse Width	$0.5t_{CK}$ – 3 + w		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A13–0, $\overline{xMS}$ Setup before $\overline{WR}$ Low[2]	$0.25t_{CK}$ – 3		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK}$ – 3		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK}$ – 2	$0.25t_{CK}$ + 4	ns
t_{AW}	A13–0, $\overline{xMS}$ Setup before $\overline{WR}$ Deasserted	$0.75t_{CK}$ – 5 + w		ns
t_{WRA}	A13–0, $\overline{xMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK}$ – 1		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK}$ – 3		ns

[1] w = wait states 3 t_{CK}.
[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

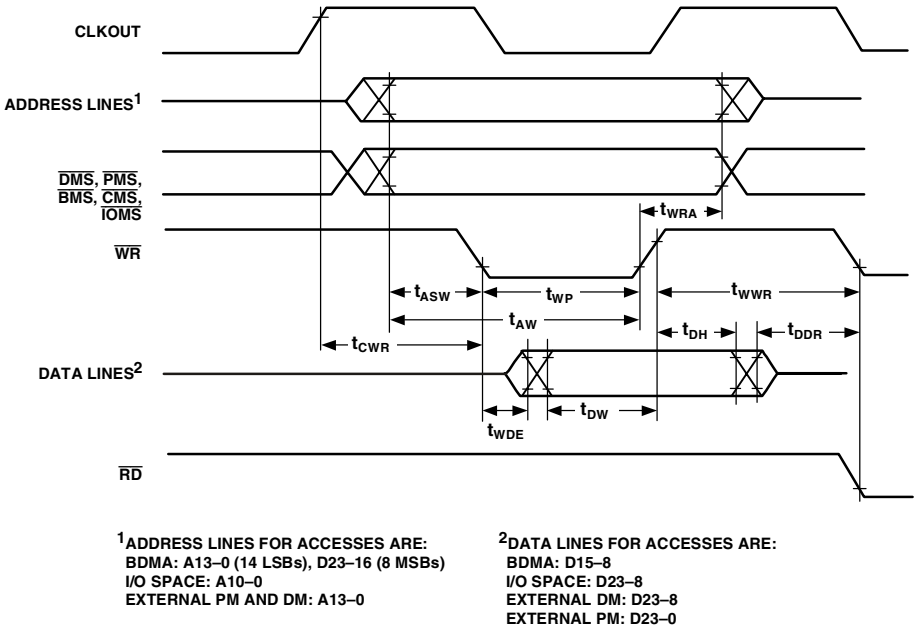

Figure 30. Memory Write

Serial Ports

Table 20. Serial Ports

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SCK}	SCLK Period	30		ns
t_{SCS}	DR/TFS/RFS Setup Before SCLK Low	4		ns
t_{SCH}	DR/TFS/RFS Hold After SCLK Low	7		ns
t_{SCP}	SCLKIN Width	12		ns
Switching Characteristics:				
t_{CC}	CLKOUT High to SCLKOUT	$0.25t_{CK}$	$0.25t_{CK} + 6$	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		7	ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		7	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS (Alt) to DT Enable	0		ns
t_{TDV}	TFS (Alt) to DT Valid		7	ns
t_{SCDD}	SCLK High to DT Disable		7	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		7	ns

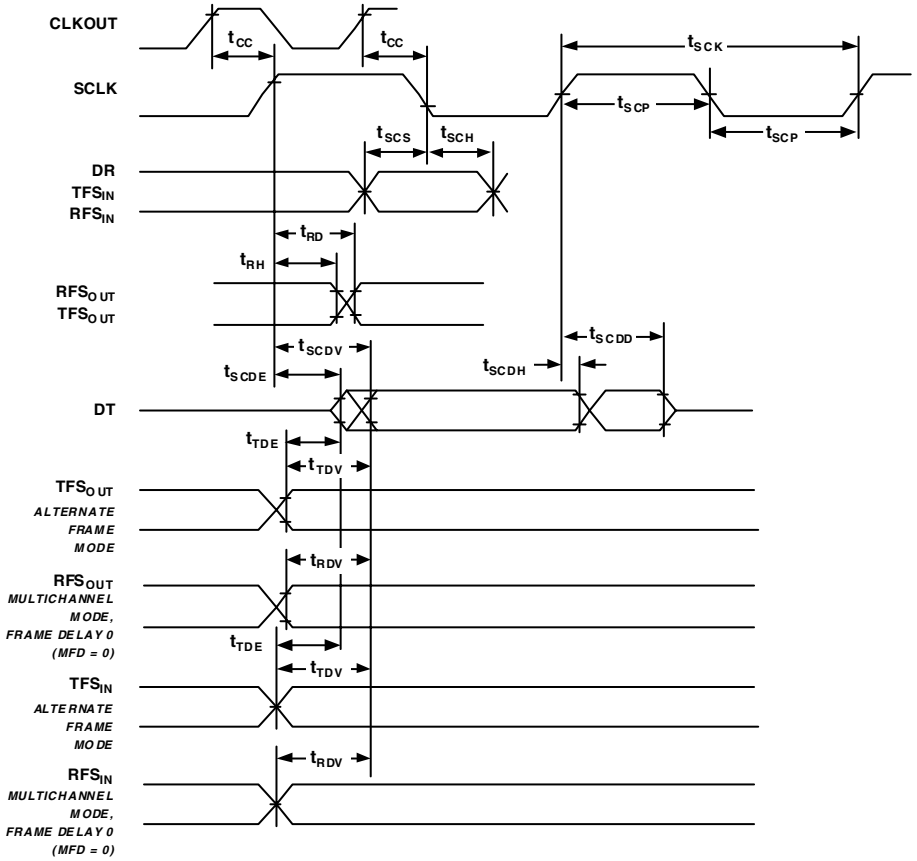

Figure 31. Serial Ports

IDMA Address Latch

Table 21. IDMA Address Latch

Parameter		Min	Max	Unit
Timing Requirements:				
t_{IALP}	Duration of Address Latch[1, 2]	10		ns
t_{IASU}	IAD15–0 Address Setup Before Address Latch End[2]	5		ns
t_{IAH}	IAD15–0 Address Hold After Address Latch End[2]	3		ns
t_{IKA}	$\overline{IACK}$ Low before Start of Address Latch[2, 3]	0		ns
t_{IALS}	Start of Write or Read After Address Latch End[2, 3]	3		ns
t_{IALD}	Address Latch Start After Address Latch End[1, 2]	2		ns

[1] Start of Address Latch = $\overline{IS}$ Low and IAL High.
[2] End of Address Latch = $\overline{IS}$ High or IAL Low.
[3] Start of Write or Read = $\overline{IS}$ Low and $\overline{IWR}$ Low or $\overline{IRD}$ Low.

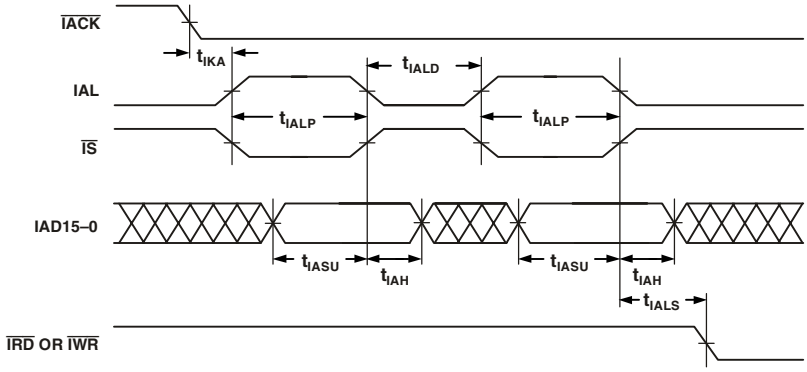

Figure 32. IDMA Address Latch

LQFP PACKAGE PINOUT

The LQFP package pinout is shown Figure 38 and in Table 27. Pin names in bold text in the table replace the plain-text-named functions when Mode C = 1. A + sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$. The multiplexed pins DT1/FO, TFS1/$\overline{\text{IRQ1}}$, RFS1/$\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default, upon reset.

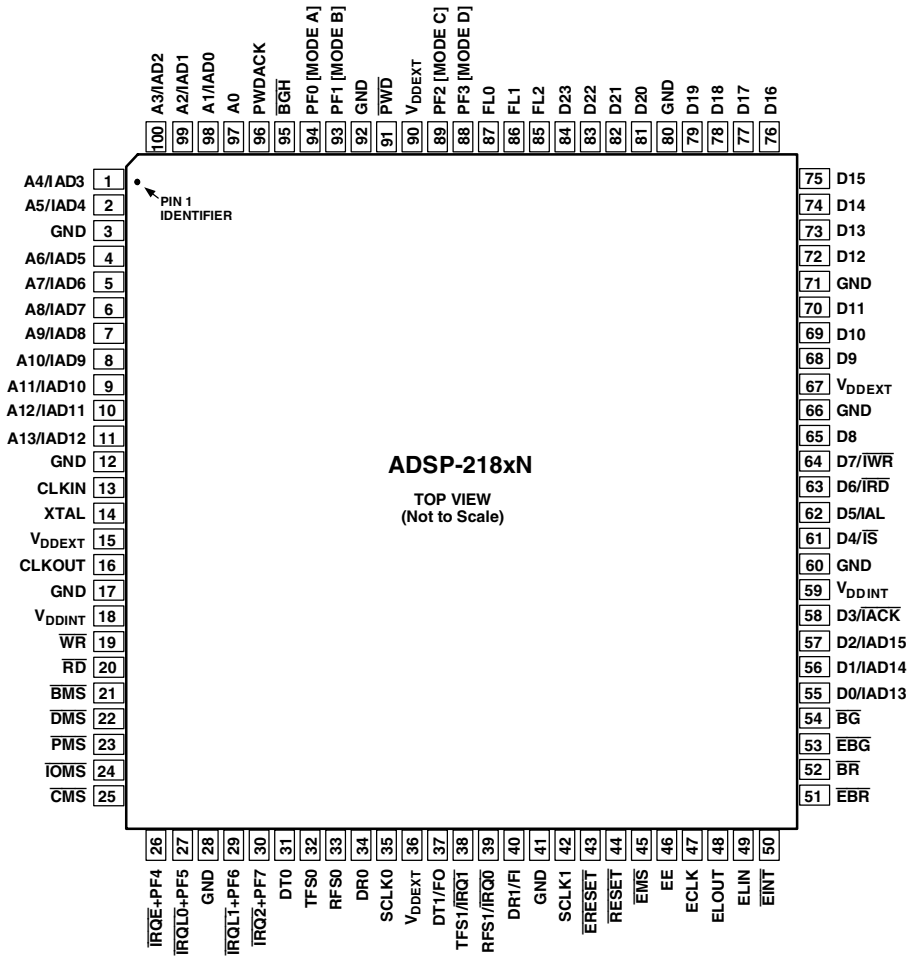

Figure 38. 100-Lead LQFP Pin Configuration

Table 27. LQFP Package Pinout

Pin No.	Pin Name
1	A4/**IAD3**
2	A5/**IAD4**
3	GND
4	A6/**IAD5**
5	A7/**IAD6**
6	A8/**IAD7**
7	A9/**IAD8**
8	A10/**IAD9**
9	A11/**IAD10**
10	A12/**IAD11**
11	A13/**IAD12**
12	GND
13	CLKIN
14	XTAL
15	V_{DDEXT}
16	CLKOUT
17	GND
18	V_{DDINT}
19	$\overline{WR}$
20	$\overline{RD}$
21	$\overline{BMS}$
22	$\overline{DMS}$
23	$\overline{PMS}$
24	$\overline{IOMS}$
25	$\overline{CMS}$
26	$\overline{IRQE}$ + PF4
27	$\overline{IRQL0}$ + PF5
28	GND
29	$\overline{IRQL1}$ + PF6
30	$\overline{IRQ2}$ + PF7
31	DT0
32	TFS0
33	RFS0
34	DR0
35	SCLK0
36	V_{DDEXT}
37	DT1/FO
38	TFS1/$\overline{IRQ1}$
39	RFS1/$\overline{IRQ0}$
40	DR1/FI
41	GND
42	SCLK1
43	$\overline{ERESET}$
44	$\overline{RESET}$
45	$\overline{EMS}$
46	EE
47	ECLK
48	ELOUT
49	ELIN
50	$\overline{EINT}$

Table 27. LQFP Package Pinout (Continued)

Pin No.	Pin Name
51	$\overline{EBR}$
52	$\overline{BR}$
53	$\overline{EBG}$
54	$\overline{BG}$
55	D0/**IAD13**
56	D1/**IAD14**
57	D2/**IAD15**
58	D3/$\overline{\textbf{IACK}}$
59	V_{DDINT}
60	GND
61	D4/$\overline{\textbf{IS}}$
62	D5/**IAL**
63	D6/$\overline{\textbf{IRD}}$
64	D7/$\overline{\textbf{IWR}}$
65	D8
66	GND
67	V_{DDEXT}
68	D9
69	D10
70	D11
71	GND
72	D12
73	D13
74	D14
75	D15
76	D16
77	D17
78	D18
79	D19
80	GND
81	D20
82	D21
83	D22
84	D23
85	FL2
86	FL1
87	FL0
88	PF3 [Mode D]
89	PF2 [Mode C]
90	V_{DDEXT}
91	$\overline{PWD}$
92	GND
93	PF1 [Mode B]
94	PF0 [Mode A]
95	$\overline{BGH}$
96	PWDACK
97	A0
98	A1/**IAD0**
99	A2/**IAD1**
100	A3/**IAD2**

Table 28. BGA Package Pinout

Ball No.	Pin Name
A01	A2/**IAD1**
A02	A1/**IAD0**
A03	GND
A04	A0
A05	NC
A06	GND
A07	NC
A08	NC
A09	NC
A10	D22
A11	GND
A12	GND
B01	A4/**IAD3**
B02	A3/**IAD2**
B03	GND
B04	NC
B05	NC
B06	GND
B07	V_{DDEXT}
B08	D23
B09	D20
B10	D18
B11	D17
B12	D16
C01	PWDACK
C02	A6/**IAD5**
C03	$\overline{RD}$
C04	A5/**IAD4**
C05	A7/**IAD6**
C06	$\overline{PWD}$
C07	V_{DDEXT}
C08	D21
C09	D19
C10	D15
C11	NC
C12	D14
D01	NC
D02	$\overline{WR}$
D03	NC
D04	$\overline{BGH}$
D05	A9/**IAD8**
D06	PF1 [MODE B]
D07	PF2 [MODE C]
D08	NC
D09	D13
D10	D12
D11	NC
D12	GND
E01	V_{DDEXT}

Table 28. BGA Package Pinout (Continued)

Ball No.	Pin Name
E02	V_{DDEXT}
E03	A8/**IAD7**
E04	FL0
E05	PF0 [MODE A]
E06	FL2
E07	PF3 [MODE D]
E08	GND
E09	GND
E10	V_{DDEXT}
E11	GND
E12	D10
F01	A13/**IAD12**
F02	NC
F03	A12/**IAD11**
F04	A11/**IAD10**
F05	FL1
F06	NC
F07	NC
F08	D7/$\overline{\textbf{IWR}}$
F09	D11
F10	D8
F11	NC
F12	D9
G01	XTAL
G02	NC
G03	GND
G04	A10/**IAD9**
G05	NC
G06	NC
G07	NC
G08	D6/$\overline{\textbf{IRD}}$
G09	D5/**IAL**
G10	NC
G11	NC
G12	D4/$\overline{\textbf{IS}}$
H01	CLKIN
H02	GND
H03	GND
H04	GND
H05	V_{DDINT}
H06	DT0
H07	TFS0
H08	D2/**IAD15**
H09	D3/$\overline{\textbf{IACK}}$
H10	GND
H11	NC
H12	GND
J01	CLKOUT
J02	V_{DDINT}

Table 28. BGA Package Pinout (Continued)

Ball No.	Pin Name
J03	NC
J04	V_{DDEXT}
J05	V_{DDEXT}
J06	SCLK0
J07	D0/**IAD13**
J08	RFS1/$\overline{IRQ0}$
J09	$\overline{BG}$
J10	D1/**IAD14**
J11	V_{DDINT}
J12	V_{DDINT}
K01	NC
K02	NC
K03	NC
K04	$\overline{BMS}$
K05	$\overline{DMS}$
K06	RFS0
K07	TFS1/$\overline{IRQ1}$
K08	SCLK1
K09	$\overline{ERESET}$
K10	$\overline{EBR}$
K11	$\overline{BR}$
K12	$\overline{EBG}$
L01	$\overline{IRQE}$ + PF4
L02	NC
L03	$\overline{IRQL1}$ + PF6
L04	$\overline{IOMS}$
L05	GND
L06	$\overline{PMS}$
L07	DR0
L08	GND
L09	$\overline{RESET}$
L10	ELIN
L11	ELOUT
L12	$\overline{EINT}$
M01	$\overline{IRQL0}$ + PF5
M02	$\overline{IRQL2}$ + PF7
M03	NC
M04	$\overline{CMS}$
M05	GND
M06	DT1/FO
M07	DR1/FI
M08	GND
M09	NC
M10	$\overline{EMS}$
M11	EE
M12	ECLK

OUTLINE DIMENSIONS

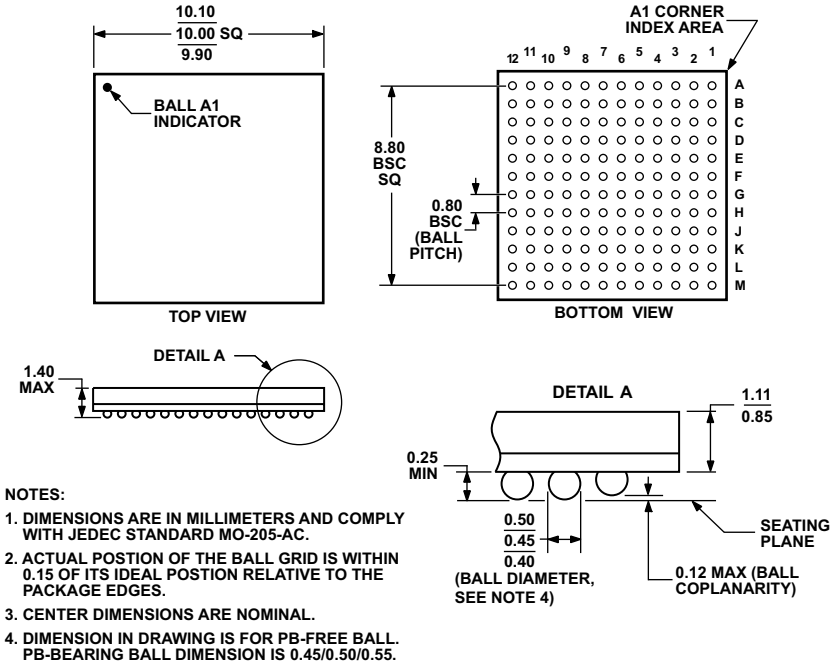

Figure 40. 144-Ball BGA [CSP_BGA] (BC-144-6)

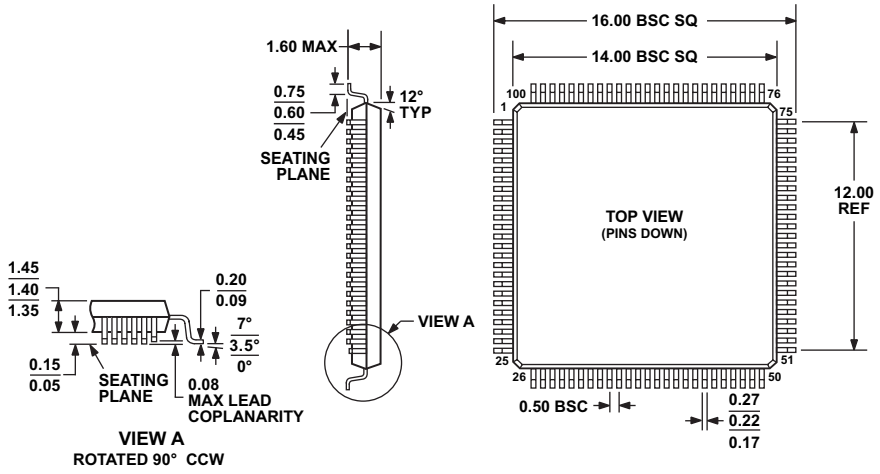

Figure 41. 100-Lead Low Profile Quad Flat Package [LQFP] (ST-100-1)

SURFACE MOUNT DESIGN

Table 29 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard*.

Table 29. BGA Data for Use with Surface Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
144-Ball BGA (BC-144-6)	Solder Mask Defined	0.40 mm diameter	0.50 mm diameter

ORDERING GUIDE

Model	Temperature Range[1]	Instruction Rate (MHz)	Package Description	Package Option
ADSP-2184NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2184NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2184NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2184NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2184NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2185NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2185NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2185NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2185NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2185NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2185NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2186NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2186NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2186NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2186NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2186NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2186NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2187NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2187NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2187NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2187NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2187NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2187NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2188NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2188NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2188NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2188NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2188NKCAZ-320[2]	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2188NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2188NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2189NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2189NBCAZ-320[2]	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2189NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2189NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2189NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2189NKCAZ-320[2]	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2189NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2189NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1

[1] Ranges shown represent ambient temperature.
[2] Z = Pb-free part.