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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, Serial Port
Clock Rate	80MHz
Non-Volatile Memory	External
On-Chip RAM	192kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.90V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2189nbstz-320

GENERAL DESCRIPTION

The ADSP-218xN series consists of six single chip microcomputers optimized for digital signal processing applications. The high-level block diagram for the ADSP-218xN series members appears on the previous page. All series members are pin-compatible and are differentiated solely by the amount of on-chip SRAM. This feature, combined with ADSP-21xx code compatibility, provides a great deal of flexibility in the design decision. Specific family members are shown in Table 1.

Table 1. ADSP-218xN DSP Microcomputer Family

Device	Program Memory (K words)	Data Memory (K words)
ADSP-2184N	4	4
ADSP-2185N	16	16
ADSP-2186N	8	8
ADSP-2187N	32	32
ADSP-2188N	48	56
ADSP-2189N	32	48

ADSP-218xN series members combine the ADSP-2100 family base architecture (three computational units, data address generators, and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, Flag I/O, extensive interrupt capabilities, and on-chip program and data memory.

ADSP-218xN series members integrate up to 256K bytes of on-chip memory configured as up to 48K words (24-bit) of program RAM, and up to 56K words (16-bit) of data RAM. Power-down circuitry is also provided to meet the low power needs of battery-operated portable equipment. The ADSP-218xN is available in a 100-lead LQFP package and 144-ball BGA.

Fabricated in a high-speed, low-power, 0.18 µm CMOS process, ADSP-218xN series members operate with a 12.5 ns instruction cycle time. Every instruction can execute in a single processor cycle.

The ADSP-218xN's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle, ADSP-218xN series members can:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computational operation

This takes place while the processor continues to:

- Receive and transmit data through the two serial ports
- Receive and/or transmit data through the internal DMA port
- Receive and/or transmit data through the byte DMA port
- Decrement timer

ARCHITECTURE OVERVIEW

The ADSP-218xN series instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-218xN assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

The functional block diagram is an overall block diagram of the ADSP-218xN series. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add, and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations.

The shifter can be used to efficiently implement numeric format control, including multiword and block floating-point representations.

The internal result (R) bus connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls, and returns in a single cycle. With internal loop counters and loop stacks, ADSP-218xN series members execute looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Five internal buses provide efficient data transfer:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

Table 3. Interrupt Priority and Interrupt Vector Addresses

Source Of Interrupt	Interrupt Vector Address (Hex)
Reset (or Power-Up with PUCR = 1)	0x0000 (Highest Priority)
Power-Down (Nonmaskable)	0x002C
$\overline{\text{IRQ2}}$	0x0004
$\overline{\text{IRQL1}}$	0x0008
$\overline{\text{IRQL0}}$	0x000C
SPORT0 Transmit	0x0010
SPORT0 Receive	0x0014
$\overline{\text{IRQE}}$	0x0018
BDMA Interrupt	0x001C
SPORT1 Transmit or $\overline{\text{IRQ1}}$	0x0020
SPORT1 Receive or $\overline{\text{IRQ0}}$	0x0024
Timer	0x0028 (Lowest Priority)

Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially. Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The power-down interrupt is nonmaskable.

ADSP-218xN series members mask all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect serial port autobuffering or DMA transfers.

The interrupt control register, ICNTL, controls interrupt nesting and defines the $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ external interrupts to be either edge- or level-sensitive. The $\overline{\text{IRQE}}$ pin is an external edge-sensitive interrupt and can be forced and cleared. The $\overline{\text{IRQL0}}$ and $\overline{\text{IRQL1}}$ pins are external level sensitive interrupts.

The IFC register is a write-only register used to force and clear interrupts. On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are 12 levels deep to allow interrupt, loop, and subroutine nesting. The following instructions allow global enable or disable servicing of the interrupts (including power-down), regardless of the state of IMASK:

```
ENA INTS;
DIS INTS;
```

Disabling the interrupts does not affect serial port autobuffering or DMA. When the processor is reset, interrupt servicing is enabled.

LOW-POWER OPERATION

ADSP-218xN series members have three low-power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

Power-Down

ADSP-218xN series members have a low-power feature that lets the processor enter a very low-power dormant state through hardware or software control. Following is a brief list of power-down features. Refer to the *ADSP-218x DSP Hardware Reference*, "System Interface" chapter, for detailed information about the power-down feature.

- Quick recovery from power-down. The processor begins executing instructions in as few as 200 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the lowest power rating and 200 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits approximately 4096 CLKIN cycles for the crystal oscillator to start or stabilize), and letting the oscillator run to allow 200 CLKIN cycle start-up.
- Power-down is initiated by either the power-down pin ($\overline{\text{PWD}}$) or the software power-down force bit. Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt also can be used as a nonmaskable, edge-sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{\text{RESET}}$ pin also can be used to terminate power-down.
- Power-down acknowledge pin (PWDACK) indicates when the processor has entered power-down.

Idle

When the ADSP-218xN is in the Idle Mode, the processor waits indefinitely in a low-power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. In Idle mode IDMA, BDMA, and autobuffer cycle steals still occur.

Slow Idle

The IDLE instruction is enhanced on ADSP-218xN series members to let the processor's internal clock signal be slowed, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the IDLE instruction.

The format of the instruction is:

```
IDLE (n);
```

where n = 16, 32, 64, or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals,

such as SCLK, CLKOUT, and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard IDLE instruction.

When the IDLE (n) instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts. The one-cycle response time of the standard idle state is increased by n, the clock divisor. When an enabled interrupt is received, ADSP-218xN series members remain in the idle state for up to a maximum of n processor cycles (n = 16, 32, 64, or 128) before resuming normal operation.

When the IDLE (n) instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of n processor cycles).

SYSTEM INTERFACE

Figure 2 shows typical basic system configurations with the ADSP-218xN series, two serial devices, a byte-wide EPROM, and optional external program and data overlay memories (mode-selectable). Programmable wait state generation allows the processor to connect easily to slow peripheral devices. ADSP-218xN series members also provide four external interrupts and two serial ports or six external interrupts and one serial port. Host Memory Mode allows access to the full external data bus, but limits addressing to a single address bit (A0). Through the use of external hardware, additional system peripherals can be added in this mode to generate and latch address signals.

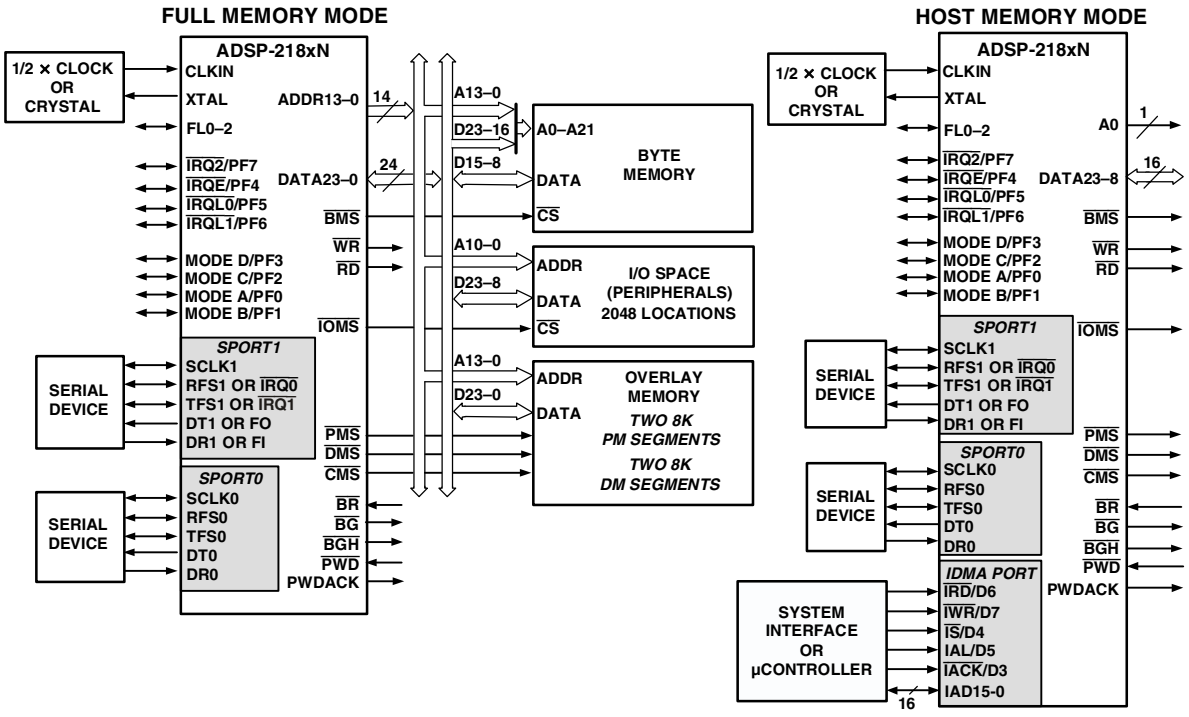

Figure 2. Basic System Interface

Clock Signals

ADSP-218xN series members can be clocked by either a crystal or a TTL-compatible clock signal.

The CLKIN input cannot be halted, changed during operation, nor operated below the specified frequency during normal operation. The only exception is while the processor is in the power-down state. For additional information, refer to the *ADSP-218x DSP Hardware Reference*, for detailed information on this power-down feature.

If an external clock is used, it should be a TTL-compatible signal running at half the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL pin must be left unconnected.

ADSP-218xN series members use an input clock with a frequency equal to half the instruction rate; a 40 MHz input clock yields a 12.5 ns processor cycle (which is equivalent to 80 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled.

Because ADSP-218xN series members include an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 3. Capacitor values are dependent on crystal type and should be specified by the crystal manufacturer. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used. To provide an adequate feedback path around the internal amplifier circuit, place a resistor in parallel with the circuit, as shown in Figure 3.

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate. This can be enabled and disabled by the CLKODIS bit in the SPORT0 Autobuffer Control Register.

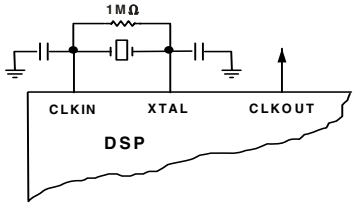

Figure 3. External Crystal Connections

RESET

The $\overline{\text{RESET}}$ signal initiates a master reset of the ADSP-218xN. The $\overline{\text{RESET}}$ signal must be asserted during the power-up sequence to assure proper initialization. $\overline{\text{RESET}}$ during initial power-up must be held long enough to allow the internal clock to stabilize. If $\overline{\text{RESET}}$ is activated any time after power-up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked, but does not include the crystal oscillator start-up time. During this power-up sequence the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulse-width specification (t_{RSP}).

The $\overline{\text{RESET}}$ input contains some hysteresis; however, if an RC circuit is used to generate the $\overline{\text{RESET}}$ signal, the use of an external Schmitt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts, and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, if there is no pending bus request and the chip is configured for booting, the boot-loading sequence is performed. The first instruction is fetched from on-chip program memory location 0x0000 once boot loading completes.

POWER SUPPLIES

ADSP-218xN series members have separate power supply connections for the internal (V_{DDINT}) and external (V_{DDEXT}) power supplies. The internal supply must meet the 1.8 V requirement. The external supply can be connected to a 1.8 V, 2.5 V, or 3.3 V supply. All external supply pins must be connected to the same supply. All input and I/O pins can tolerate input voltages up to 3.6 V, regardless of the external supply voltage. This feature provides maximum flexibility in mixing 1.8 V, 2.5 V, or 3.3 V components.

MEMORY ARCHITECTURE

The ADSP-218xN series provides a variety of memory and peripheral interface options. The key functional groups are Program Memory, Data Memory, Byte Memory, and I/O. Refer to Figure 4 through Figure 9, Table 4 on Page 11, and Table 5 on Page 11 for PM and DM memory allocations in the ADSP-218xN series.

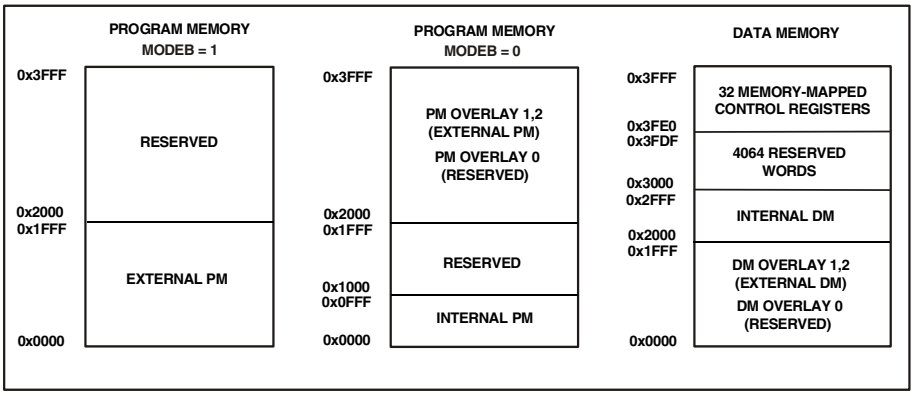

Figure 4. ADSP-2184 Memory Architecture

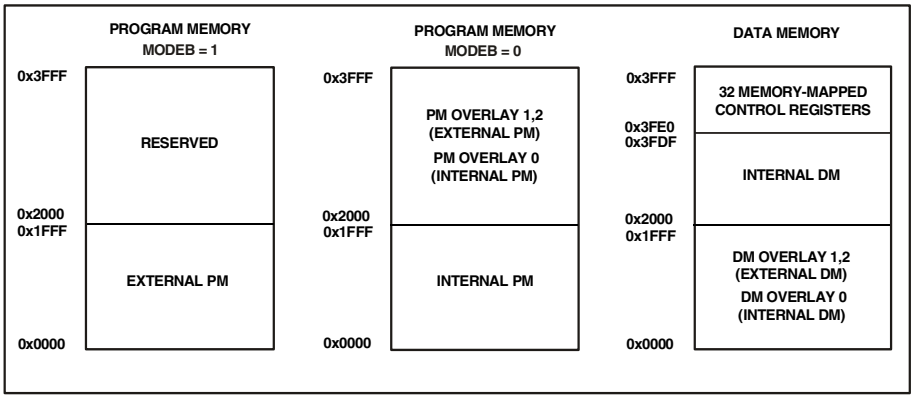

Figure 5. ADSP-2185 Memory Architecture

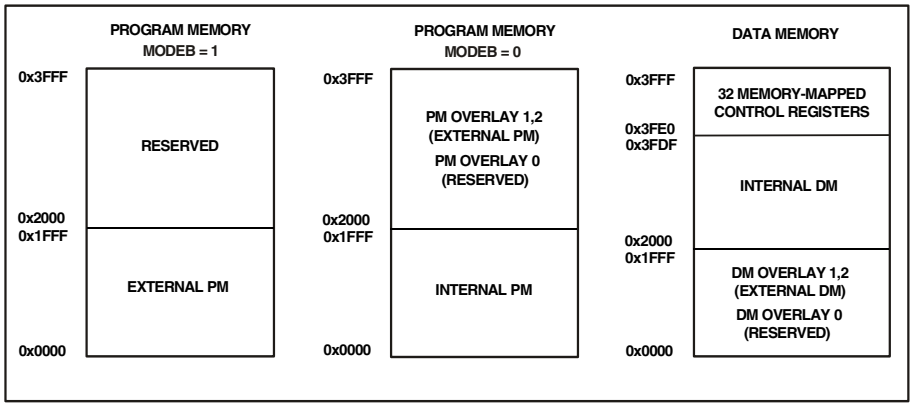

Figure 6. ADSP-2186 Memory Architecture

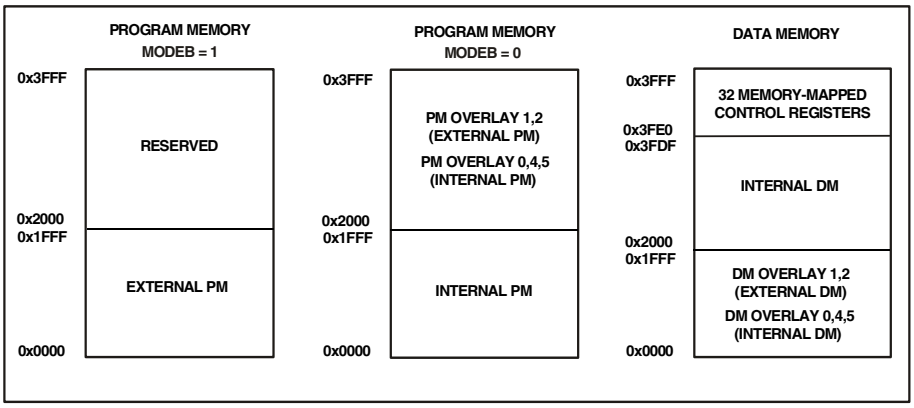

Figure 7. ADSP-2187 Memory Architecture

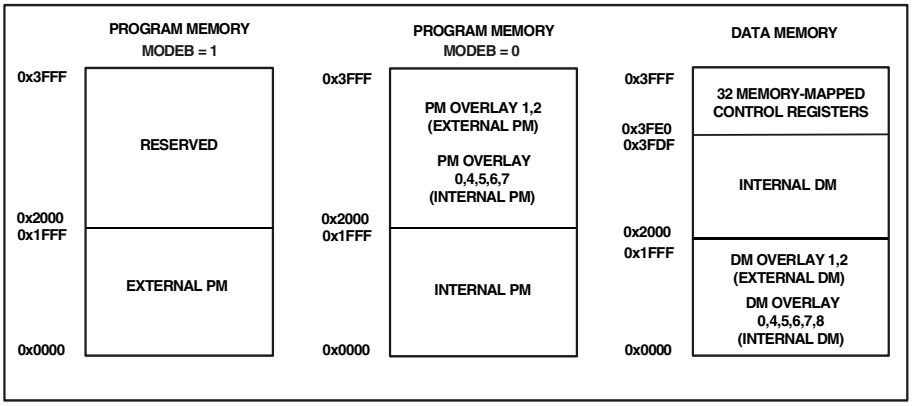

Figure 8. ADSP-2188 Memory Architecture

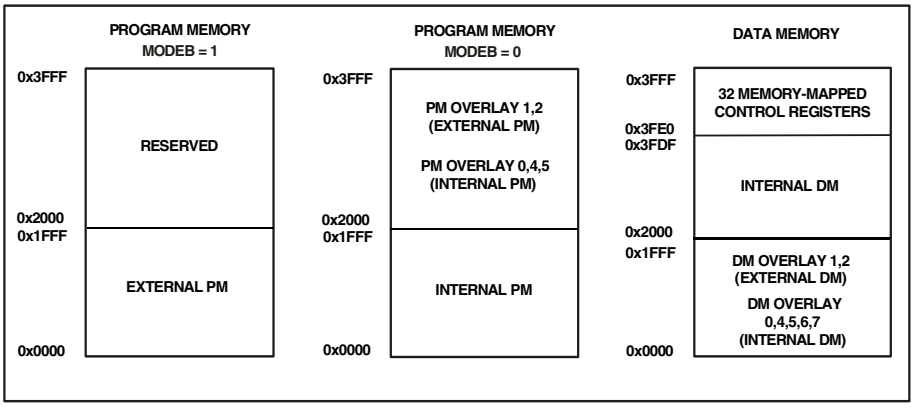

Figure 9. ADSP-2189 Memory Architecture

Program Memory

Program Memory (Full Memory Mode) is a 24-bit-wide space for storing both instruction opcodes and data. The member DSPs of this series have up to 48K words of Program Memory RAM on chip, and the capability of accessing up to two 8K external memory overlay spaces, using the external data bus.

Program Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0). External program execution is not available in host mode due to a restricted data bus that is only 16 bits wide.

Table 4. PMOVLAY Bits

Processor	PMOVLAY	Memory	A13	A12–0
ADSP-2184N	No Internal Overlay Region	Not Applicable	Not Applicable	Not Applicable
ADSP-2185N	0	Internal Overlay	Not Applicable	Not Applicable
ADSP-2186N	No Internal Overlay Region	Not Applicable	Not Applicable	Not Applicable
ADSP-2187N	0, 4, 5	Internal Overlay	Not Applicable	Not Applicable
ADSP-2188N	0, 4, 5, 6, 7	Internal Overlay	Not Applicable	Not Applicable
ADSP-2189N	0, 4, 5	Internal Overlay	Not Applicable	Not Applicable
All Processors	1	External Overlay 1	0	13 LSBs of Address Between 0x2000 and 0x3FFF
All Processors	2	External Overlay 2	1	13 LSBs of Address Between 0x2000 and 0x3FFF

Data Memory

Data Memory (Full Memory Mode) is a 16-bit-wide space used for the storage of data variables and for memory-mapped control registers. The ADSP-218xN series has up to 56K words of Data Memory RAM on-chip. Part of this space is used by 32 memory-mapped registers. Support also exists for up to two 8K external memory overlay spaces through the external data bus.

All internal accesses complete in one cycle. Accesses to external memory are timed using the wait states specified by the DWAIT register and the wait state mode bit.

Data Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0).

Table 5. DMOVLAY Bits

Processor	DMOVLAY	Memory	A13	A12–0
ADSP-2184N	No Internal Overlay Region	Not Applicable	Not Applicable	Not Applicable
ADSP-2185N	0	Internal Overlay	Not Applicable	Not Applicable
ADSP-2186N	No Internal Overlay Region	Not Applicable	Not Applicable	Not Applicable
ADSP-2187N	0, 4, 5	Internal Overlay	Not Applicable	Not Applicable
ADSP-2188N	0, 4, 5, 6, 7, 8	Internal Overlay	Not Applicable	Not Applicable
ADSP-2189N	0, 4, 5, 6, 7	Internal Overlay	Not Applicable	Not Applicable
All Processors	1	External Overlay 1	0	13 LSBs of Address Between 0x0000 and 0x1FFF
All Processors	2	External Overlay 2	1	13 LSBs of Address Between 0x0000 and 0x1FFF

Memory-Mapped Registers (New to the ADSP-218xM and N series)

ADSP-218xN series members have three memory-mapped registers that differ from other ADSP-21xx Family DSPs. The slight modifications to these registers (Wait State Control, Programmable Flag and Composite Select Control, and System Control) provide the ADSP-218xN's wait state and $\overline{\text{BMS}}$ control features. Default bit values at reset are shown; if no value is shown, the bit is undefined at reset. Reserved bits are shown on a grey field. These bits should always be written with zeros.

I/O Space (Full Memory Mode)

ADSP-218xN series members support an additional external memory space called I/O space. This space is designed to support simple connections to peripherals (such as data converters and external registers) or to bus interface ASIC data registers. I/O space supports 2048 locations of 16-bit wide data. The lower eleven bits of the external address bus are used; the upper three bits are undefined.

Two instructions were added to the core ADSP-2100 Family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated three-bit wait state registers,

IOWAIT0–3 as shown in Figure 10, which in combination with the wait state mode bit, specify up to 15 wait states to be automatically generated for each of four regions. The wait states act on address ranges, as shown in Table 6.

Note: In Full Memory Mode, all 2048 locations of I/O space are directly addressable. In Host Memory Mode, only address pin A0 is available; therefore, additional logic is required externally to achieve complete addressability of the 2048 I/O space locations.

Table 6. Wait States

Address Range	Wait State Register
0x000–0x1FF	IOWAIT0 and Wait State Mode Select Bit
0x200–0x3FF	IOWAIT1 and Wait State Mode Select Bit
0x400–0x5FF	IOWAIT2 and Wait State Mode Select Bit
0x600–0x7FF	IOWAIT3 and Wait State Mode Select Bit

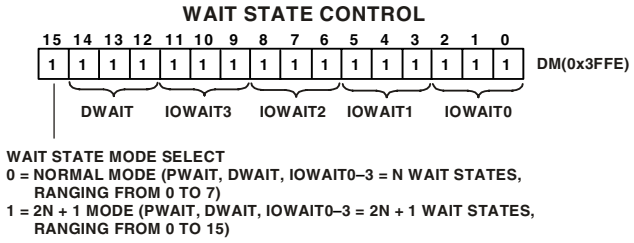

Figure 10. Wait State Control Register

Composite Memory Select

ADSP-218xN series members have a programmable memory select signal that is useful for generating memory select signals for memories mapped to more than one space. The $\overline{\text{CMS}}$ signal is generated to have the same timing as each of the individual memory select signals ($\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$) but can combine their functionality. Each bit in the CMSSEL register, when set, causes the $\overline{\text{CMS}}$ signal to be asserted when the selected memory select is asserted. For example, to use a 32K word memory to act as both program and data memory, set the $\overline{\text{PMS}}$ and $\overline{\text{DMS}}$ bits in the CMSSEL register and use the $\overline{\text{CMS}}$ pin to drive the chip select of the memory, and use either $\overline{\text{DMS}}$ or $\overline{\text{PMS}}$ as the additional address bit.

The $\overline{\text{CMS}}$ pin functions like the other memory select signals with the same timing and bus request logic. A 1 in the enable bit causes the assertion of the $\overline{\text{CMS}}$ signal at the same time as the selected memory select signal. All enable bits default to 1 at reset, except the $\overline{\text{BMS}}$ bit.

See Figure 11 and Figure 12 for illustration of the programmable flag and composite control register and the system control register.

Byte Memory Select

The ADSP-218xN's $\overline{\text{BMS}}$ disable feature combined with the $\overline{\text{CMS}}$ pin allows use of multiple memories in the byte memory space. For example, an EPROM could be attached to the $\overline{\text{BMS}}$

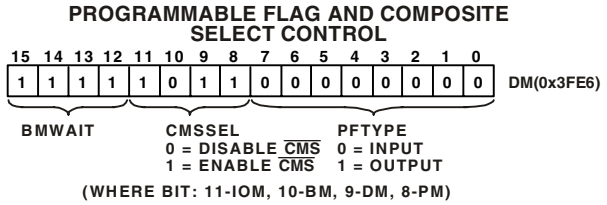

Figure 11. Programmable Flag and Composite Control Register

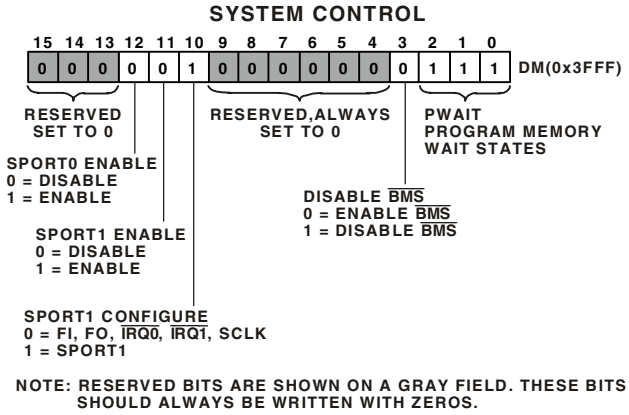

Figure 12. System Control Register

select, and a flash memory could be connected to $\overline{\text{CMS}}$. Because at reset $\overline{\text{BMS}}$ is enabled, the EPROM would be used for booting. After booting, software could disable $\overline{\text{BMS}}$ and set the $\overline{\text{CMS}}$ signal to respond to $\overline{\text{BMS}}$, enabling the flash memory.

Byte Memory

The byte memory space is a bidirectional, 8-bit-wide, external memory space used to store programs and data. Byte memory is accessed using the BDMA feature. The byte memory space consists of 256 pages, each of which is 16K × 8 bits.

The byte memory space on the ADSP-218xN series supports read and write operations as well as four different data formats. The byte memory uses data bits 15–8 for data. The byte memory uses data bits 23–16 and address bits 13–0 to create a 22-bit address. This allows up to a 4 megabit × 8 (32 megabit) ROM or RAM to be used without glue logic. All byte memory accesses are timed by the BMWAIT register and the wait state mode bit.

Byte Memory DMA (BDMA, Full Memory Mode)

The byte memory DMA controller (Figure 13) allows loading and storing of program instructions and data using the byte memory space. The BDMA circuit is able to access the byte memory space while the processor is operating normally and steals only one DSP cycle per 8-, 16-, or 24-bit word transferred.

The IDMA port has a 16-bit multiplexed address and data bus and supports 24-bit program memory. The IDMA port is completely asynchronous and can be written while the ADSP-218xN is operating at full speed.

The DSP memory address is latched and then automatically incremented after each IDMA transaction. An external device can therefore access a block of sequentially addressed memory by specifying only the starting address of the block. This increases throughput as the address does not have to be sent for each memory access.

IDMA port access occurs in two phases. The first is the IDMA Address Latch cycle. When the acknowledge is asserted, a 14-bit address and 1-bit destination type can be driven onto the bus by an external device. The address specifies an on-chip memory location, the destination type specifies whether it is a DM or PM access. The falling edge of the IDMA address latch signal (IAL) or the missing edge of the IDMA select signal ($\overline{IS}$) latches this value into the IDMAA register.

Once the address is stored, data can be read from, or written to, the ADSP-218xN's on-chip memory. Asserting the select line ($\overline{IS}$) and the appropriate read or write line ($\overline{IRD}$ and $\overline{IWR}$ respectively) signals the ADSP-218xN that a particular transaction is required. In either case, there is a one-processor-cycle delay for synchronization. The memory access consumes one additional processor cycle.

Once an access has occurred, the latched address is automatically incremented, and another access can occur.

Through the IDMAA register, the DSP can also specify the starting address and data format for DMA operation. Asserting the IDMA port select ($\overline{IS}$) and address latch enable (IAL) directs the ADSP-218xN to write the address onto the IAD14–0 bus into the IDMA Control Register (Figure 14). If Bit 15 is set to 0, IDMA latches the address. If Bit 15 is set to 1, IDMA latches into the OVLAY register. This register, also shown in Figure 14, is memory-mapped at address DM (0x3FE0). Note that the latched address (IDMAA) cannot be read back by the host.

When Bit 14 in 0x3FE7 is set to zero, short reads use the timing shown in Figure 36 on Page 38. When Bit 14 in 0x3FE7 is set to 1, timing in Figure 37 on Page 39 applies for short reads in short read only mode. Set IDDMOVLAY and IDPMOVLAY bits in the IDMA overlay register as indicated in Table 8. Refer to the *ADSP-218x DSP Hardware Reference* for additional details.

Note: In full memory mode all locations of 4M-byte memory space are directly addressable. In host memory mode, only address pin A0 is available, requiring additional external logic to provide address information for the byte.

Bootstrap Loading (Booting)

ADSP-218xN series members have two mechanisms to allow automatic loading of the internal program memory after reset. The method for booting is controlled by the Mode A, B, and C configuration bits.

When the mode pins specify BDMA booting, the ADSP-218xN initiates a BDMA boot sequence when reset is released.

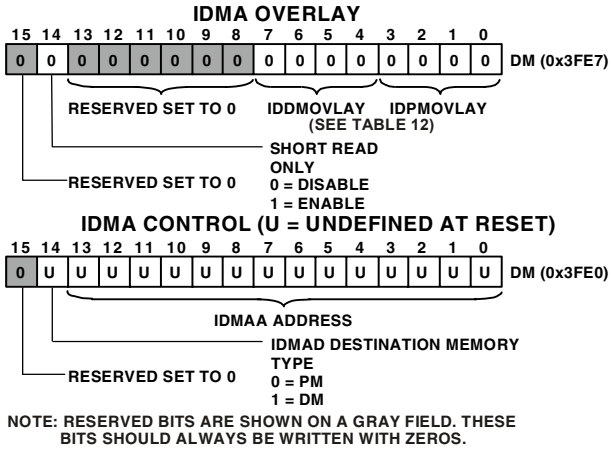

Figure 14. IDMA OVLAY/Control Registers

The BDMA interface is set up during reset to the following defaults when BDMA booting is specified: the BDIR, BMPAGE, BIAD, and BEAD registers are set to 0, the BTYPE register is set to 0 to specify program memory 24-bit words, and the BWCOUNT register is set to 32. This causes 32 words of on-chip program memory to be loaded from byte memory. These 32 words are used to set up the BDMA to load in the remaining program code. The BCR bit is also set to 1, which causes program execution to be held off until all 32 words are loaded into on-chip program memory. Execution then begins at address 0.

The ADSP-2100 Family development software (Revision 5.02 and later) fully supports the BDMA booting feature and can generate byte memory space-compatible boot code.

The IDLE instruction can also be used to allow the processor to hold off execution while booting continues through the BDMA interface. For BDMA accesses while in Host Mode, the addresses to boot memory must be constructed externally to the ADSP-218xN. The only memory address bit provided by the processor is A0.

IDMA Port Booting

ADSP-218xN series members can also boot programs through its internal DMA port. If Mode C = 1, Mode B = 0, and Mode A = 1, the ADSP-218xN boots from the IDMA port. IDMA feature can load as much on-chip memory as desired. Program execution is held off until the host writes to on-chip program memory location 0.

BUS REQUEST AND BUS GRANT

ADSP-218xN series members can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the Bus Request

- Fill and dump memory
- Source level debugging

The VisualDSP++ IDE lets programmers define and manage DSP software development. The dialog boxes and property pages let programmers configure and manage all of the ADSP-218xN development tools, including the syntax highlighting in the VisualDSP++ editor. This capability controls how the development tools process inputs and generate outputs.

The ADSP-2189M EZ-KIT Lite®† provides developers with a cost-effective method for initial evaluation of the powerful ADSP-218xN DSP family architecture. The ADSP-2189M EZ-KIT Lite includes a stand-alone ADSP-2189M DSP board supported by an evaluation suite of VisualDSP++. With this EZ-KIT Lite, users can learn about DSP hardware and software development and evaluate potential applications of the ADSP-218xN series. The ADSP-2189M EZ-KIT Lite provides an evaluation suite of the VisualDSP++ development environment with the C compiler, assembler, and linker. The size of the DSP executable that can be built using the EZ-KIT Lite tools is limited to 8K words.

The EZ-KIT Lite includes the following features:

- 75 MHz ADSP-2189M
- Full 16-Bit Stereo Audio I/O with AD73322 Codec
- RS-232 Interface
- EZ-ICE Connector for Emulator Control
- DSP Demonstration Programs
- Evaluation Suite of VisualDSP++

The ADSP-218x EZ-ICE®‡ Emulator provides an easier and more cost-effective method for engineers to develop and optimize DSP systems, shortening product development cycles for faster time-to-market. ADSP-218xN series members integrate on-chip emulation support with a 14-pin ICE-Port interface. This interface provides a simpler target board connection that requires fewer mechanical clearance considerations than other ADSP-2100 Family EZ-ICEs. ADSP-218xN series members need not be removed from the target system when using the EZ-ICE, nor are any adapters needed. Due to the small footprint of the EZ-ICE connector, emulation can be supported in final board designs.The EZ-ICE performs a full range of functions, including:

- In-target operation
- Up to 20 breakpoints
- Single-step or full-speed operation
- Registers and memory values can be examined and altered
- PC upload and download functions
- Instruction-level emulation of program booting and execution
- Complete assembly and disassembly of instructions
- C source-level debugging

Designing an EZ-ICE-Compatible System

ADSP-218xN series members have on-chip emulation support and an ICE-Port, a special set of pins that interface to the EZ-ICE. These features allow in-circuit emulation without replacing the target system processor by using only a 14-pin connection from the target system to the EZ-ICE. Target systems must have a 14-pin connector to accept the EZ-ICE's in-circuit probe, a 14-pin plug.

Note: The EZ-ICE uses the same V_{DD} voltage as the V_{DD} voltage used for V_{DDEXT}. Because the input pins of the ADSP-218xN series members are tolerant to input voltages up to 3.6 V, regardless of the value of V_{DDEXT}, the voltage setting for the EZ-ICE must not exceed 3.3 V.

Issuing the chip reset command during emulation causes the DSP to perform a full chip reset, including a reset of its memory mode. Therefore, it is vital that the mode pins are set correctly PRIOR to issuing a chip reset command from the emulator user interface. If a passive method of maintaining mode information is being used (as discussed in Setting Memory Mode on Page 5), it does not matter that the mode information is latched by an emulator reset. However, if the $\overline{\text{RESET}}$ pin is being used as a method of setting the value of the mode pins, the effects of an emulator reset must be taken into consideration.

One method of ensuring that the values located on the mode pins are those desired is to construct a circuit like the one shown in Figure 15. This circuit forces the value located on the Mode A pin to logic high, regardless of whether it is latched via the $\overline{\text{RESET}}$ or $\overline{\text{ERESET}}$ pin.

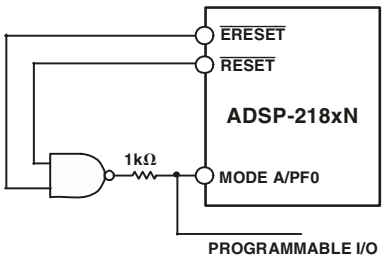

Figure 15. Mode A Pin/EZ-ICE Circuit

The ICE-Port interface consists of the following ADSP-218xN pins: $\overline{\text{EBR}}$, $\overline{\text{EINT}}$, EE, $\overline{\text{EBG}}$, ECLK, $\overline{\text{ERESET}}$, ELIN, $\overline{\text{EMS}}$, and ELOUT.

These ADSP-218xN pins must be connected only to the EZ-ICE connector in the target system. These pins have no function except during emulation, and do not require pull-up or pull-down resistors. The traces for these signals between the ADSP-218xN and the connector must be kept as short as possible, no longer than 3 inches.

The following pins are also used by the EZ-ICE: $\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{RESET}}$, and GND.

† EZ-KIT Lite is a registered trademark of Analog Devices, Inc.
‡ EZ-ICE is a registered trademark of Analog Devices, Inc.

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter[1]	K Grade (Commercial)		B Grade (Industrial)		Unit
	Min	Max	Min	Max	
V_{DDINT}	1.71	1.89	1.8	2.0	V
V_{DDEXT}	1.71	3.6	1.8	3.6	V
V_{INPUT}[2]	V_{IL} = – 0.3	V_{IH} = + 3.6	V_{IL} = – 0.3	V_{IH} = + 3.6	V
T_{AMB}	0	70	–40	+85	°C

[1] Specifications subject to change without notice.

[2] The ADSP-218xN is 3.3 V tolerant (always accepts up to 3.6 V max V_{IH}), but voltage compliance (on outputs, V_{OH}) depends on the input V_{DDEXT}, because V_{OH} (max) approximately equals V_{DDEXT} (max). This 3.3 V tolerance applies to bidirectional pins (D23–D0, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A13–A1, PF7–PF0) and input-only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$).

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Hi-Level Input Voltage[2, 3]	@ V_{DDEXT} = 1.71 V to 2.0 V, V_{DDINT} = max	1.25			V
		@ V_{DDEXT} = 2.1 V to 3.6 V, V_{DDINT} = max	1.7			V
V_{IL}	Lo-Level Input Voltage[2, 3]	@ $V_{DDEXT} \leq$ 2.0 V, V_{DDINT} = min			0.6	V
		@ $V_{DDEXT} \geq$ 2.0 V, V_{DDINT} = min			0.7	V
V_{OH}	Hi-Level Output Voltage[2, 4, 5]	@ V_{DDEXT} = 1.71 V to 2.0 V, I_{OH} = – 0.5 mA	1.35			V
		@ V_{DDEXT} = 2.1 V to 2.9 V, I_{OH} = – 0.5 mA	2.0			V
		@ V_{DDEXT} = 3.0 V to 3.6 V, I_{OH} = – 0.5 mA	2.4			V
		@ V_{DDEXT} = 1.71 V to 3.6 V, I_{OH} = – 100 µA[6]	V_{DDEXT} – 0.3			V
V_{OL}	Lo-Level Output Voltage[2, 4, 5]	@ V_{DDEXT} = 1.71 V to 3.6 V, I_{OL} = 2.0 mA			0.4	V
I_{IH}	Hi-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 3.6 V			10	µA
I_{IL}	Lo-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 0 V			10	µA
I_{OZH}	Three-State Leakage Current[7]	@ V_{DDEXT} = max, V_{IN} = 3.6 V[8]			10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DDEXT} = max, V_{IN} = 0 V[8]			10	µA
I_{DD}	Supply Current (Idle)[9]	@ V_{DDINT} = 1.8 V, t_{CK} = 12.5 ns, T_{AMB} = 25°C		6		mA
I_{DD}	Supply Current (Dynamic)[10]	@ V_{DDINT} = 1.8 V, t_{CK} = 12.5 ns[11], T_{AMB} = 25°C		25		mA

ENVIRONMENTAL CONDITIONS

Table 14. Thermal Resistance

Rating Description[1]	Symbol	LQFP (°C/W)	BGA (°C/W)
Thermal Resistance (Case-to-Ambient)	θ_{CA}	48	63.3
Thermal Resistance (Junction-to-Ambient)	θ_{JA}	50	70.7
Thermal Resistance (Junction-to-Case)	θ_{JC}	2	7.4

[1] Where the Ambient Temperature Rating (T_{AMB}) is:
$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W

TEST CONDITIONS

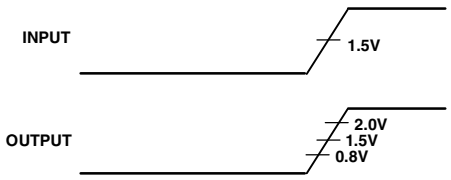

Figure 18. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

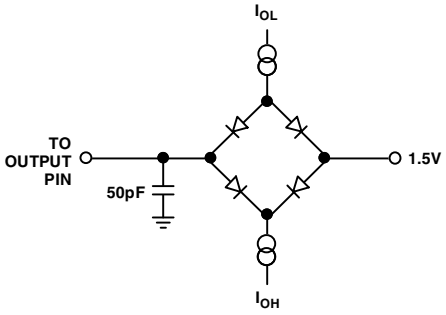

Figure 19. Equivalent Loading for AC Measurements (Including All Fixtures)

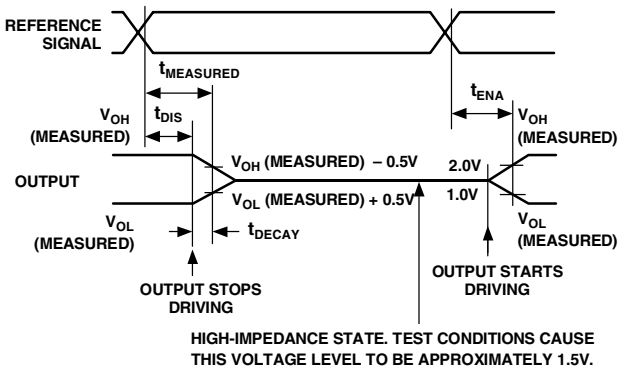

Figure 20. Output Enable/Disable

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 20. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitive load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 20. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

TIMING SPECIFICATIONS

This section contains timing information for the DSP's external signals.

General Notes

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, parameters cannot be added up meaningfully to derive longer times.

Timing Notes

Switching characteristics specify how the processor changes its signals. Designers have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell what the processor will do in a given circumstance. Switching characteristics can also be used to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Frequency Dependency For Timing Specifications

t_{CK} is defined as 0.5 t_{CKI}. The ADSP-218xN uses an input clock with a frequency equal to half the instruction rate. For example, a 40 MHz input clock (which is equivalent to 25 ns) yields a 12.5 ns processor cycle (equivalent to 80 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain the specification value.

Example: t_{CKH} = 0.5 t_{CK} – 2 ns = 0.5 (12.5 ns) – 2 ns = 4.25 ns

Output Drive Currents

Figure 21 shows typical I-V characteristics for the output drivers on the ADSP-218xN series.The curves represent the current drive capability of the output drivers as a function of output voltage.

Figure 23 shows the typical power-down supply current.

Capacitive Loading

Figure 24 and Figure 25 show the capacitive loading characteristics of the ADSP-218xN.

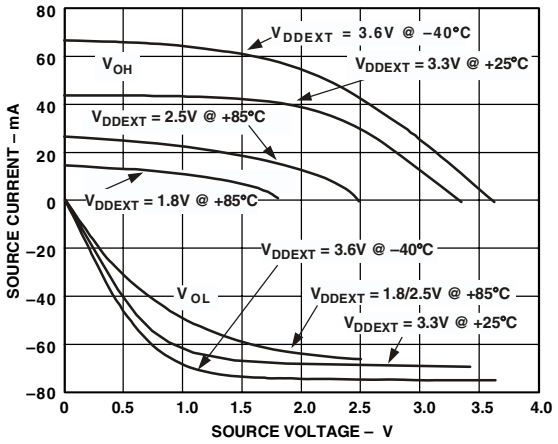

Figure 21. Typical Output Driver Characteristics for V_{DDEXT} at 3.6 V, 3.3 V, 2.5 V, and 1.8 V

Bus Request–Bus Grant

Table 17. Bus Request–Bus Grant

Parameter		Min	Max	Unit
Timing Requirements:				
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	$0.25t_{CK} + 2$		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	$0.25t_{CK} + 8$		ns
Switching Characteristics:				
t_{SD}	CLKOUT High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable[2]		$0.25t_{CK} + 8$	ns
t_{SDB}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE}	$\overline{BG}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	$0.25t_{CK} - 3$		ns
t_{SDBH}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BGH}$ Low[3]	0		ns
t_{SEH}	$\overline{BGH}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable[3]	0		ns

[1] $\overline{BR}$ is an asynchronous signal. If $\overline{BR}$ meets the setup/hold requirements, it will be recognized during the current clock cycle; otherwise the signal will be recognized on the following cycle. Refer to the *ADSP-2100 Family User's Manual* for $\overline{BR}$/BG cycle relationships.

[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

[3] $\overline{BGH}$ is asserted when the bus is granted and the processor or BDMA requires control of the bus to continue.

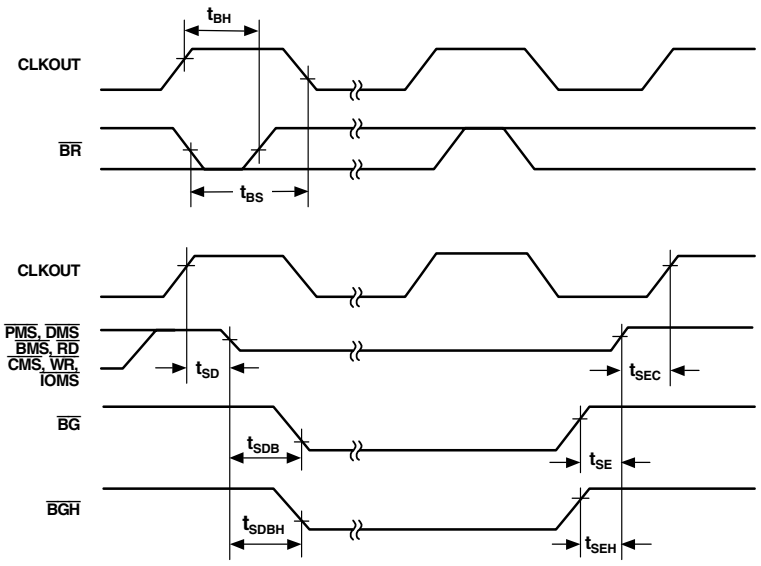

Figure 28. Bus Request–Bus Grant

Memory Write

Table 19. Memory Write

Parameter		Min	Max	Unit
Switching Characteristics:				
t_{DW}	Data Setup before $\overline{WR}$ High[1]	$0.5t_{CK}$– 4 + w		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK}$ – 1		ns
t_{WP}	$\overline{WR}$ Pulse Width	$0.5t_{CK}$ – 3 + w		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A13–0, $\overline{xMS}$ Setup before $\overline{WR}$ Low[2]	$0.25t_{CK}$ – 3		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK}$ – 3		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK}$ – 2	$0.25t_{CK}$ + 4	ns
t_{AW}	A13–0, $\overline{xMS}$ Setup before $\overline{WR}$ Deasserted	$0.75t_{CK}$ – 5 + w		ns
t_{WRA}	A13–0, $\overline{xMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK}$ – 1		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK}$ – 3		ns

[1] w = wait states 3 t_{CK}.
[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

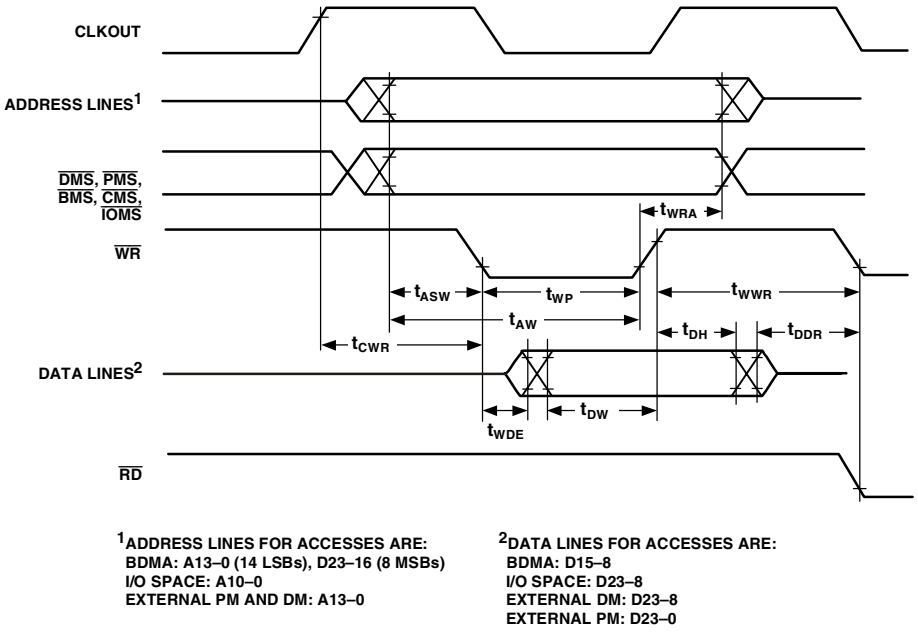

Figure 30. Memory Write

Serial Ports

Table 20. Serial Ports

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SCK}	SCLK Period	30		ns
t_{SCS}	DR/TFS/RFS Setup Before SCLK Low	4		ns
t_{SCH}	DR/TFS/RFS Hold After SCLK Low	7		ns
t_{SCP}	SCLKIN Width	12		ns
Switching Characteristics:				
t_{CC}	CLKOUT High to SCLKOUT	$0.25t_{CK}$	$0.25t_{CK} + 6$	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		7	ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		7	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS (Alt) to DT Enable	0		ns
t_{TDV}	TFS (Alt) to DT Valid		7	ns
t_{SCDD}	SCLK High to DT Disable		7	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		7	ns

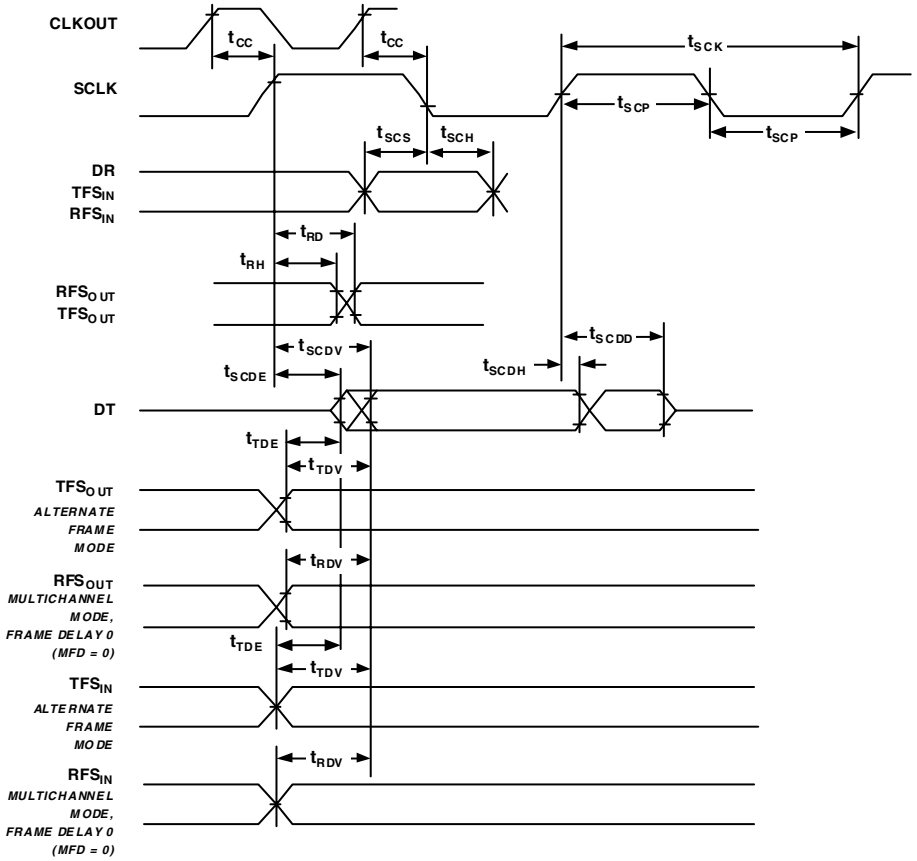

Figure 31. Serial Ports

IDMA Write, Short Write Cycle

Table 22. IDMA Write, Short Write Cycle

Parameter		Min	Max	Unit
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low Before Start of Write[1]	0		ns
t_{IWP}	Duration of Write[1, 2]	10		ns
t_{IDSU}	IAD15–0 Data Setup Before End of Write[2, 3, 4]	3		ns
t_{IDH}	IAD15–0 Data Hold After End of Write[2, 3, 4]	2		ns
Switching Characteristic:				
t_{IKHW}	Start of Write to $\overline{IACK}$ High		10	ns

[1] Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2] End of Write = $\overline{IS}$ High or $\overline{IWR}$ High.
[3] If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[4] If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.

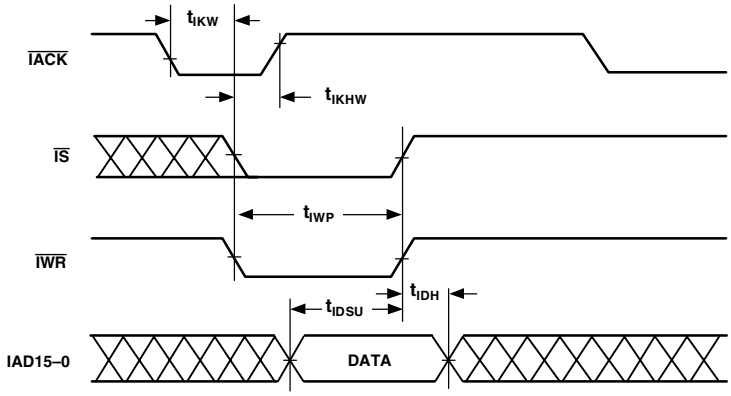

Figure 33. IDMA Write, Short Write Cycle

IDMA Read, Long Read Cycle

Table 24. IDMA Read, Long Read Cycle

Parameter		Min	Max	Unit
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low Before Start of Read[1]	0		ns
t_{IRK}	End of read After $\overline{IACK}$ Low[2]	2		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High After Start of Read[1]		10	ns
t_{IKDS}	IAD15–0 Data Setup Before $\overline{IACK}$ Low	$0.5t_{CK} - 3$		ns
t_{IKDH}	IAD15–0 Data Hold After End of Read[2]	0		ns
t_{IKDD}	IAD15–0 Data Disabled After End of Read[2]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled After Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid After Start of Read		11	ns
t_{IRDH1}	IAD15–0 Previous Data Hold After Start of Read (DM/PM1)[3]	$2t_{CK} - 5$		ns
t_{IRDH2}	IAD15–0 Previous Data Hold After Start of Read (PM2)[4]	$t_{CK} - 5$		ns

[1] Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[2] End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.
[3] DM read or first half of PM read.
[4] Second half of PM read.

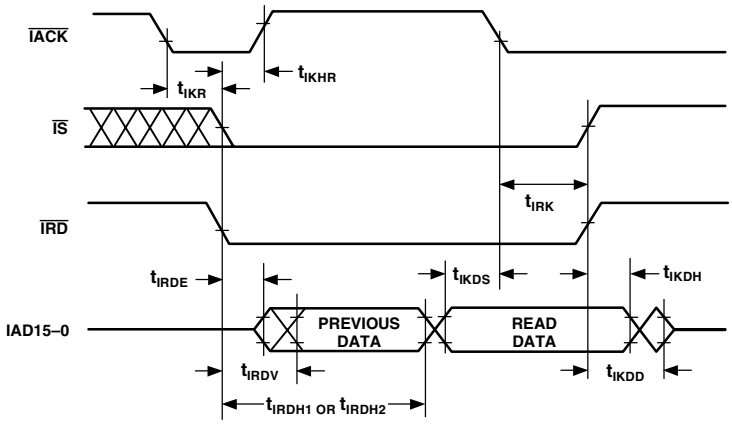

Figure 35. IDMA Read, Long Read Cycle

OUTLINE DIMENSIONS

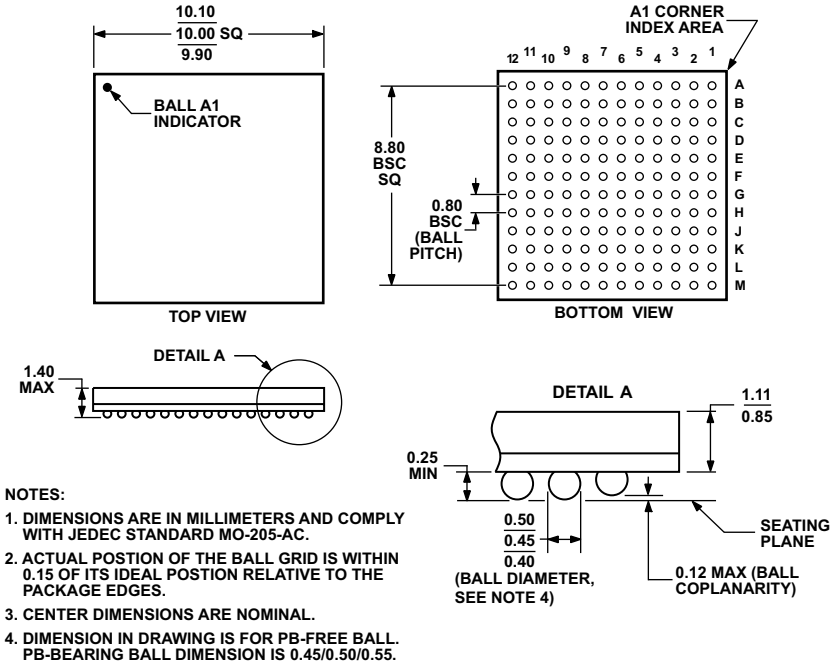

Figure 40. 144-Ball BGA [CSP_BGA] (BC-144-6)

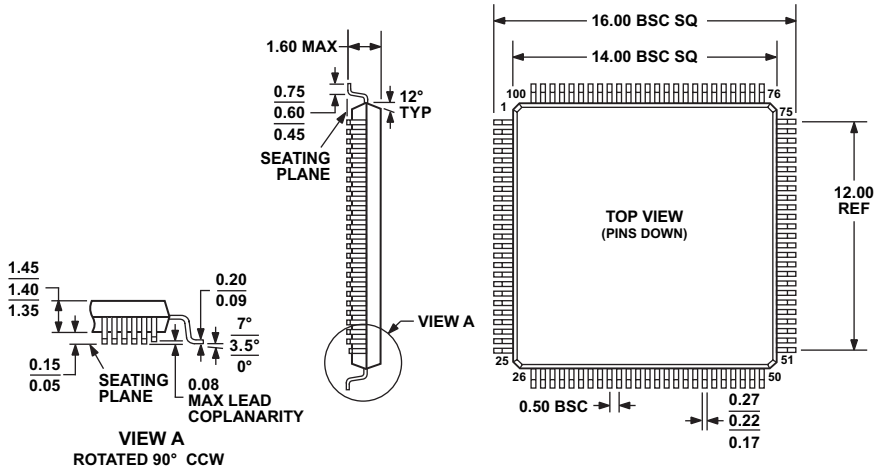

Figure 41. 100-Lead Low Profile Quad Flat Package [LQFP] (ST-100-1)

SURFACE MOUNT DESIGN

Table 29 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard*.

Table 29. BGA Data for Use with Surface Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
144-Ball BGA (BC-144-6)	Solder Mask Defined	0.40 mm diameter	0.50 mm diameter