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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, Serial Port
Clock Rate	80MHz
Non-Volatile Memory	External
On-Chip RAM	192kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.80V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA, CSPBGA
Supplier Device Package	144-CSPBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2189nkcaz-320

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REVISION HISTORY

8/06—Rev. 0 to Rev. A

Miscellaneous Format Updates..... Universal

Applied Corrections or Additional Information to:

MEMORY ARCHITECTURE

The ADSP-218xN series provides a variety of memory and peripheral interface options. The key functional groups are Program Memory, Data Memory, Byte Memory, and I/O. Refer to Figure 4 through Figure 9, Table 4 on Page 11, and Table 5 on Page 11 for PM and DM memory allocations in the ADSP-218xN series.

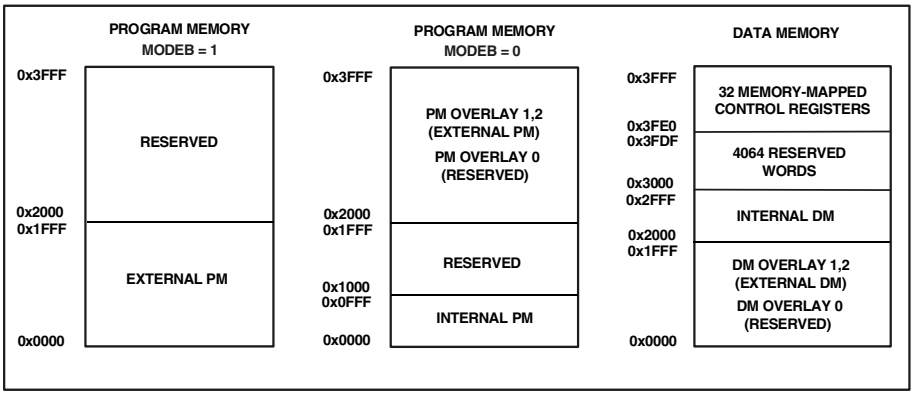

Figure 4. ADSP-2184 Memory Architecture

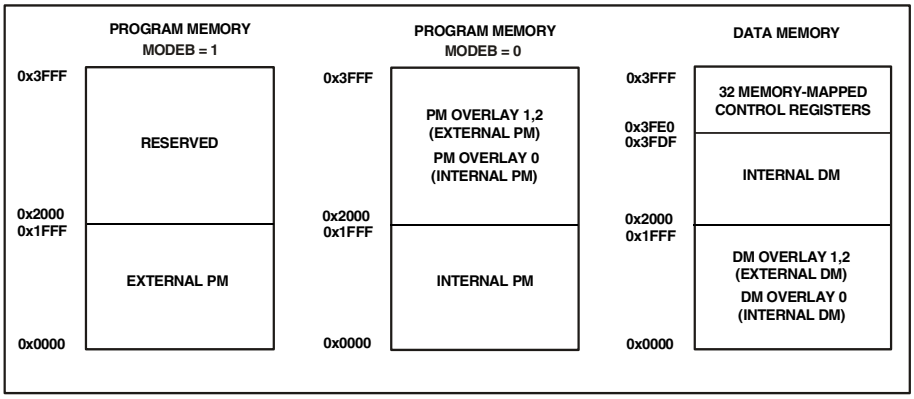

Figure 5. ADSP-2185 Memory Architecture

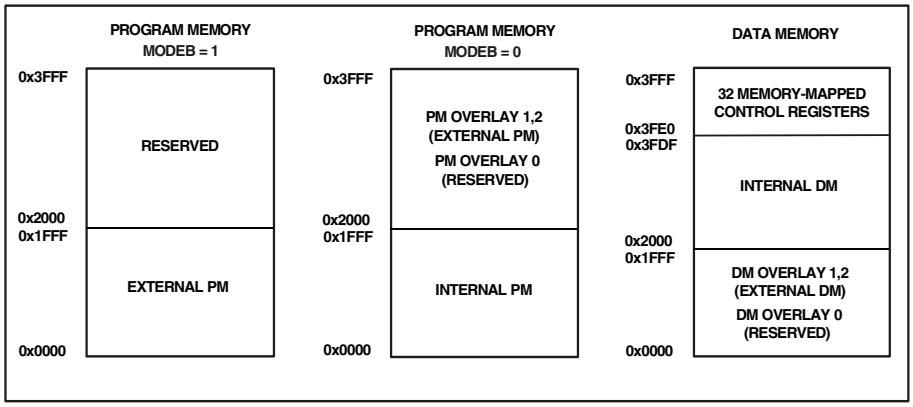

Figure 6. ADSP-2186 Memory Architecture

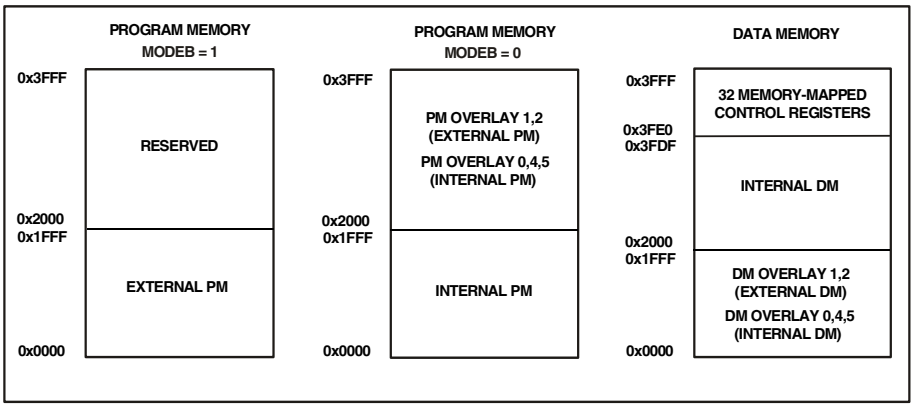

Figure 7. ADSP-2187 Memory Architecture

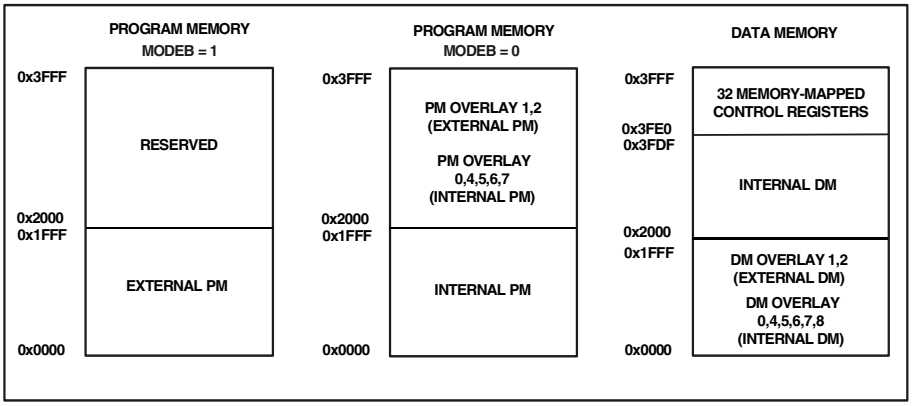

Figure 8. ADSP-2188 Memory Architecture

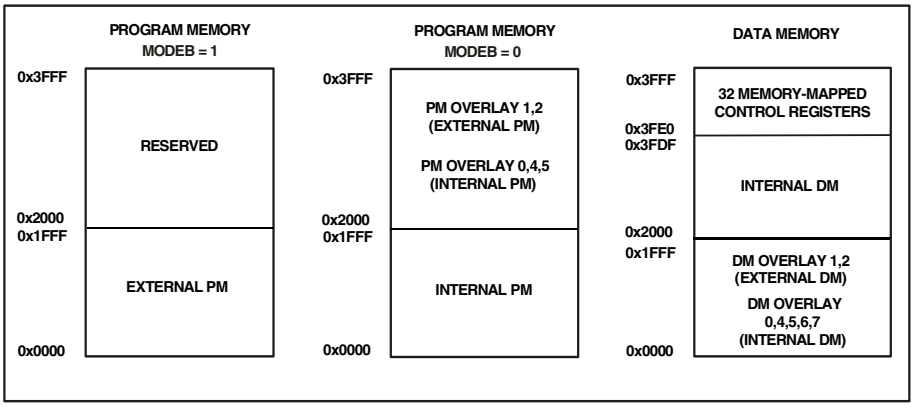

Figure 9. ADSP-2189 Memory Architecture

Program Memory

Program Memory (Full Memory Mode) is a 24-bit-wide space for storing both instruction opcodes and data. The member DSPs of this series have up to 48K words of Program Memory RAM on chip, and the capability of accessing up to two 8K external memory overlay spaces, using the external data bus.

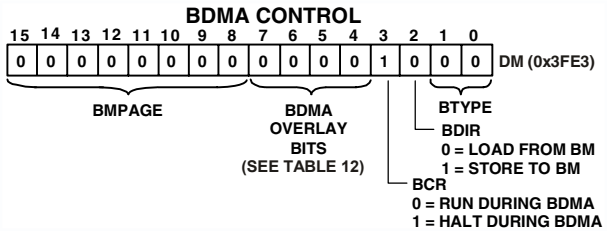

Figure 13. BDMA Control Register

The BDMA circuit supports four different data formats that are selected by the BTYPE register field. The appropriate number of 8-bit accesses are done from the byte memory space to build the word size selected. Table 7 shows the data formats supported by the BDMA circuit.

Table 7. Data Formats

BTYPE	Internal Memory Space	Word Size	Alignment
00	Program Memory	24	Full Word
01	Data Memory	16	Full Word
10	Data Memory	8	MSBs
11	Data Memory	8	LSBs

Unused bits in the 8-bit data memory formats are filled with 0s. The BIAD register field is used to specify the starting address for the on-chip memory involved with the transfer. The 14-bit BEAD register specifies the starting address for the external byte memory space. The 8-bit BMPAGE register specifies the starting page for the external byte memory space. The BDIR register field selects the direction of the transfer. Finally, the 14-bit BWCOUNT register specifies the number of DSP words to transfer and initiates the BDMA circuit transfers.

BDMA accesses can cross page boundaries during sequential addressing. A BDMA interrupt is generated on the completion of the number of transfers specified by the BWCOUNT register.

The BWCOUNT register is updated after each transfer so it can be used to check the status of the transfers. When it reaches zero, the transfers have finished and a BDMA interrupt is generated. The BMPAGE and BEAD registers must not be accessed by the DSP during BDMA operations.

The source or destination of a BDMA transfer will always be on-chip program or data memory.

When the BWCOUNT register is written with a nonzero value the BDMA circuit starts executing byte memory accesses with wait states set by BMWAIT. These accesses continue until the count reaches zero. When enough accesses have occurred to create a destination word, it is transferred to or from on-chip memory. The transfer takes one DSP cycle. DSP accesses to external memory have priority over BDMA byte memory accesses.

The BDMA Context Reset bit (BCR) controls whether the processor is held off while the BDMA accesses are occurring. Setting the BCR bit to 0 allows the processor to continue operations. Setting the BCR bit to 1 causes the processor to stop execution while the BDMA accesses are occurring, to clear the context of the processor, and start execution at address 0 when the BDMA accesses have completed.

The BDMA overlay bits specify the OVLAY memory blocks to be accessed for internal memory. Set these bits as indicated in Figure 13.

Note: BDMA cannot access external overlay memory regions 1 and 2.

The BMWAIT field, which has four bits on ADSP-218xN series members, allows selection up to 15 wait states for BDMA transfers.

Internal Memory DMA Port (IDMA Port; Host Memory Mode)

The IDMA Port provides an efficient means of communication between a host system and ADSP-218xN series members. The port is used to access the on-chip program memory and data memory of the DSP with only one DSP cycle per word overhead. The IDMA port cannot, however, be used to write to the DSP's memory-mapped control registers. A typical IDMA transfer process is shown as follows:

1. Host starts IDMA transfer.
2. Host checks $\overline{\text{IACK}}$ control line to see if the DSP is busy.
3. Host uses $\overline{\text{IS}}$ and IAL control lines to latch either the DMA starting address (IDMAA) or the PM/DM OVLAY selection into the DSP's IDMA control registers. If Bit 15 = 1, the values of Bits 7–0 represent the IDMA overlay; Bits 14–8 must be set to 0. If Bit 15 = 0, the value of Bits 13–0 represent the starting address of internal memory to be accessed and Bit 14 reflects PM or DM for access. Set IDDMOVLAY and IDPMOVLAY bits in the IDMA overlay register as indicted in Table 8.
4. Host uses $\overline{\text{IS}}$ and $\overline{\text{IRD}}$ (or $\overline{\text{IWR}}$) to read (or write) DSP internal memory (PM or DM).
5. Host checks $\overline{\text{IACK}}$ line to see if the DSP has completed the previous IDMA operation.
6. Host ends IDMA transfer.

Table 8. IDMA/BDMA Overlay Bits

Processor	IDMA/BDMA PMOVLAY	IDMA/BDMA DMOVLAY
ADSP-2184N	0	0
ADSP-2185N	0	0
ADSP-2186N	0	0
ADSP-2187N	0, 4, 5	0, 4, 5
ADSP-2188N	0, 4, 5, 6, 7	0, 4, 5, 6, 7, 8
ADSP-2189N	0, 4, 5	0, 4, 5, 6, 7

Table 9. Common-Mode Pins (Continued)

Pin Name	No. of Pins	I/O	Function
V_{DDINT}	4	I	Internal V_{DD} (1.8 V) Power (BGA)
V_{DDEXT}	7	I	External V_{DD} (1.8 V, 2.5 V, or 3.3 V) Power (BGA)
GND	20	I	Ground (BGA)
EZ-Port	9	I/O	For Emulation Use

[1] Interrupt/Flag pins retain both functions concurrently. If IMASK is set to enable the corresponding interrupts, the DSP will vector to the appropriate interrupt vector address when the pin is asserted, either by external devices or set as a programmable flag.
[2] SPORT configuration determined by the DSP System Control Register. Software configurable.

MEMORY INTERFACE PINS

ADSP-218xN series members can be used in one of two modes: Full Memory Mode, which allows BDMA operation with full external overlay memory and I/O capability, or Host Mode, which allows IDMA operation with limited external addressing capabilities.

The operating mode is determined by the state of the Mode C pin during $\overline{\text{RESET}}$ and cannot be changed while the processor is running. Table 10 and Table 11 list the active signals at specific pins of the DSP during either of the two operating modes (Full Memory or Host). A signal in one table shares a pin with a signal from the other table, with the active signal determined by the mode that is set. For the shared pins and their alternate signals (e.g., A4/IAD3), refer to the package pinouts in Table 27 on Page 41 and Table 28 on Page 43.

Table 10. Full Memory Mode Pins (Mode C = 0)

Pin Name	No. of Pins	I/O	Function
A13–0	14	O	Address Output Pins for Program, Data, Byte, and I/O Spaces
D23–0	24	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces (8 MSBs are also used as Byte Memory Addresses.)

Table 11. Host Mode Pins (Mode C = 1)

Pin Name	No. of Pins	I/O	Function
IAD15–0	16	I/O	IDMA Port Address/Data Bus
A0	1	O	Address Pin for External I/O, Program, Data, or Byte Access[1]
D23–8	16	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces
$\overline{\text{IWR}}$	1	I	IDMA Write Enable
$\overline{\text{IRD}}$	1	I	IDMA Read Enable
IAL	1	I	IDMA Address Latch Pin
$\overline{\text{IS}}$	1	I	IDMA Select
$\overline{\text{IACK}}$	1	O	IDMA Port Acknowledge Configurable in Mode D; Open Drain

[1] In Host Mode, external peripheral addresses can be decoded using the A0, $\overline{\text{CMS}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, and $\overline{\text{IOMS}}$ signals.

TERMINATING UNUSED PINS

Table 12 shows the recommendations for terminating unused pins.

Table 12. Unused Pin Terminations

Pin Name[1]	I/O 3-State (Z)[2]	Reset State	Hi-Z[3] Caused By	Unused Configuration
XTAL	O	O		Float
CLKOUT	O	O		Float[4]
A13–1 or	O (Z)	Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
IAD12–0	I/O (Z)	Hi-Z	$\overline{\text{IS}}$	Float
A0	O (Z)	Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float

Table 12. Unused Pin Terminations (Continued)

Pin Name[1]	I/O 3-State (Z)[2]	Reset State	Hi-Z[3] Caused By	Unused Configuration
$\overline{\text{ERESET}}$	I	I		Float
$\overline{\text{EMS}}$	O	O		Float
$\overline{\text{EINT}}$	I	I		Float
ECLK	I	I		Float
ELIN	I	I		Float
ELOUT	O	O		Float

[1] CLKIN, $\overline{\text{RESET}}$, and PF3 – 0/Mode D – A are not included in this table because these pins must be used.
[2] All bidirectional pins have three-stated outputs. When the pin is configured as an output, the output is Hi-Z (high impedance) when inactive.
[3] Hi-Z = High Impedance.
[4] If the CLKOUT pin is not used, turn it OFF, using CLKODIS in SPORT0 autobuffer control register.
[5] If the Interrupt/Programmable Flag pins are not used, there are two options: Option 1: When these pins are configured as INPUTS at reset and function as interrupts and input flag pins, pull the pins High (inactive). Option 2: Program the unused pins as OUTPUTS, set them to 1 prior to enabling interrupts, and let pins float.

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter[1]	K Grade (Commercial)		B Grade (Industrial)		Unit
	Min	Max	Min	Max	
V_{DDINT}	1.71	1.89	1.8	2.0	V
V_{DDEXT}	1.71	3.6	1.8	3.6	V
V_{INPUT}[2]	V_{IL} = – 0.3	V_{IH} = + 3.6	V_{IL} = – 0.3	V_{IH} = + 3.6	V
T_{AMB}	0	70	–40	+85	°C

[1] Specifications subject to change without notice.

[2] The ADSP-218xN is 3.3 V tolerant (always accepts up to 3.6 V max V_{IH}), but voltage compliance (on outputs, V_{OH}) depends on the input V_{DDEXT}, because V_{OH} (max) approximately equals V_{DDEXT} (max). This 3.3 V tolerance applies to bidirectional pins (D23–D0, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A13–A1, PF7–PF0) and input-only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$).

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Hi-Level Input Voltage[2, 3]	@ V_{DDEXT} = 1.71 V to 2.0 V, V_{DDINT} = max	1.25			V
		@ V_{DDEXT} = 2.1 V to 3.6 V, V_{DDINT} = max	1.7			V
V_{IL}	Lo-Level Input Voltage[2, 3]	@ $V_{DDEXT} \leq$ 2.0 V, V_{DDINT} = min			0.6	V
		@ $V_{DDEXT} \geq$ 2.0 V, V_{DDINT} = min			0.7	V
V_{OH}	Hi-Level Output Voltage[2, 4, 5]	@ V_{DDEXT} = 1.71 V to 2.0 V, I_{OH} = – 0.5 mA	1.35			V
		@ V_{DDEXT} = 2.1 V to 2.9 V, I_{OH} = – 0.5 mA	2.0			V
		@ V_{DDEXT} = 3.0 V to 3.6 V, I_{OH} = – 0.5 mA	2.4			V
		@ V_{DDEXT} = 1.71 V to 3.6 V, I_{OH} = – 100 µA[6]	V_{DDEXT} – 0.3			V
V_{OL}	Lo-Level Output Voltage[2, 4, 5]	@ V_{DDEXT} = 1.71 V to 3.6 V, I_{OL} = 2.0 mA			0.4	V
I_{IH}	Hi-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 3.6 V			10	µA
I_{IL}	Lo-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 0 V			10	µA
I_{OZH}	Three-State Leakage Current[7]	@ V_{DDEXT} = max, V_{IN} = 3.6 V[8]			10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DDEXT} = max, V_{IN} = 0 V[8]			10	µA
I_{DD}	Supply Current (Idle)[9]	@ V_{DDINT} = 1.8 V, t_{CK} = 12.5 ns, T_{AMB} = 25°C		6		mA
I_{DD}	Supply Current (Dynamic)[10]	@ V_{DDINT} = 1.8 V, t_{CK} = 12.5 ns[11], T_{AMB} = 25°C		25		mA

ENVIRONMENTAL CONDITIONS

Table 14. Thermal Resistance

Rating Description[1]	Symbol	LQFP (°C/W)	BGA (°C/W)
Thermal Resistance (Case-to-Ambient)	θ_{CA}	48	63.3
Thermal Resistance (Junction-to-Ambient)	θ_{JA}	50	70.7
Thermal Resistance (Junction-to-Case)	θ_{JC}	2	7.4

[1] Where the Ambient Temperature Rating (T_{AMB}) is:
$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W

TEST CONDITIONS

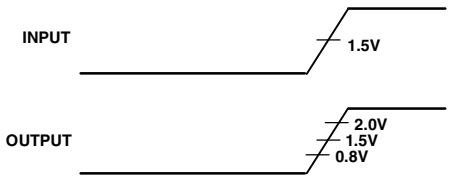

Figure 18. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

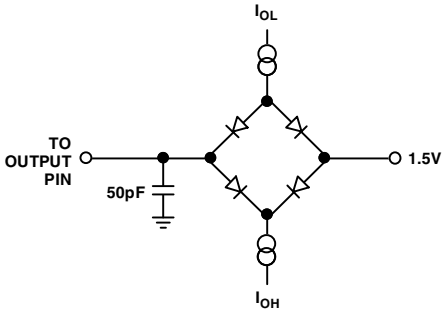

Figure 19. Equivalent Loading for AC Measurements (Including All Fixtures)

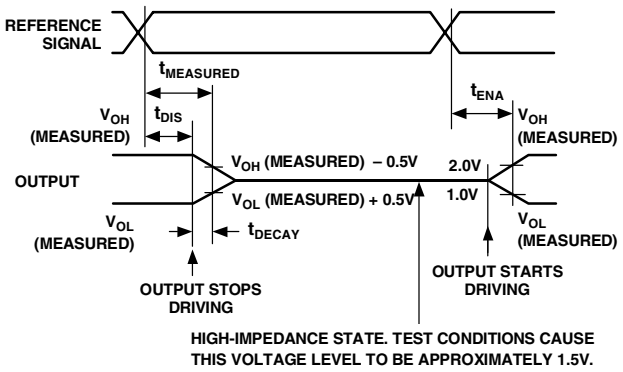

Figure 20. Output Enable/Disable

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 20. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitive load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 20. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

TIMING SPECIFICATIONS

This section contains timing information for the DSP's external signals.

General Notes

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, parameters cannot be added up meaningfully to derive longer times.

Timing Notes

Switching characteristics specify how the processor changes its signals. Designers have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell what the processor will do in a given circumstance. Switching characteristics can also be used to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Frequency Dependency For Timing Specifications

t_{CK} is defined as 0.5 t_{CKI}. The ADSP-218xN uses an input clock with a frequency equal to half the instruction rate. For example, a 40 MHz input clock (which is equivalent to 25 ns) yields a 12.5 ns processor cycle (equivalent to 80 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain the specification value.

Example: t_{CKH} = 0.5 t_{CK} – 2 ns = 0.5 (12.5 ns) – 2 ns = 4.25 ns

Output Drive Currents

Figure 21 shows typical I-V characteristics for the output drivers on the ADSP-218xN series.The curves represent the current drive capability of the output drivers as a function of output voltage.

Figure 23 shows the typical power-down supply current.

Capacitive Loading

Figure 24 and Figure 25 show the capacitive loading characteristics of the ADSP-218xN.

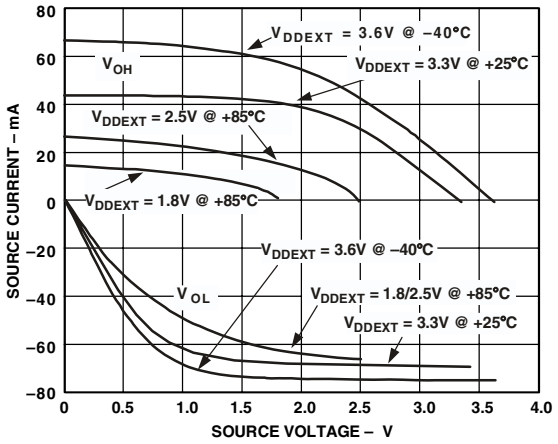

Figure 21. Typical Output Driver Characteristics for V_{DDEXT} at 3.6 V, 3.3 V, 2.5 V, and 1.8 V

Interrupts and Flags

Table 16. Interrupts and Flags

Parameter		Min	Max	Unit
Timing Requirements:				
t_{IFS}	$\overline{IRQx}$, FI, or PFx Setup before CLKOUT Low[1, 2, 3, 4]	$0.25t_{CK} + 10$		ns
t_{IFH}	$\overline{IRQx}$, FI, or PFx Hold after CLKOUT High[1, 2, 3, 4]	$0.25t_{CK}$		ns
Switching Characteristics:				
t_{FOH}	Flag Output Hold after CLKOUT Low[5]	$0.5t_{CK} - 5$		ns
t_{FOD}	Flag Output Delay from CLKOUT Low[5]		$0.5t_{CK} + 4$	ns

[1] If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to "Interrupt Controller Operation" in the *Program Control* chapter of the *ADSP-218x DSP Hardware Reference* for further information on interrupt servicing.)

[2] Edge-sensitive interrupts require pulse widths greater than 10 ns; level-sensitive interrupts must be held low until serviced.

[3] $\overline{IRQx}$ = $\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$, $\overline{IRQLE}$.

[4] PFx = PF0, PF1, PF2, PF3, PF4, PF5, PF6, PF7.

[5] Flag Outputs = PFx, FL0, FL1, FL2, FO.

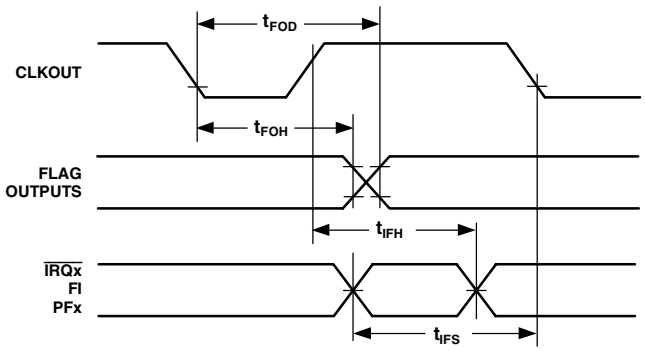

Figure 27. Interrupts and Flags

Bus Request–Bus Grant

Table 17. Bus Request–Bus Grant

Parameter		Min	Max	Unit
Timing Requirements:				
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	$0.25t_{CK} + 2$		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	$0.25t_{CK} + 8$		ns
Switching Characteristics:				
t_{SD}	CLKOUT High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable[2]		$0.25t_{CK} + 8$	ns
t_{SDB}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE}	$\overline{BG}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	$0.25t_{CK} - 3$		ns
t_{SDBH}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BGH}$ Low[3]	0		ns
t_{SEH}	$\overline{BGH}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable[3]	0		ns

[1] $\overline{BR}$ is an asynchronous signal. If $\overline{BR}$ meets the setup/hold requirements, it will be recognized during the current clock cycle; otherwise the signal will be recognized on the following cycle. Refer to the *ADSP-2100 Family User's Manual* for $\overline{BR}$/BG cycle relationships.

[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

[3] $\overline{BGH}$ is asserted when the bus is granted and the processor or BDMA requires control of the bus to continue.

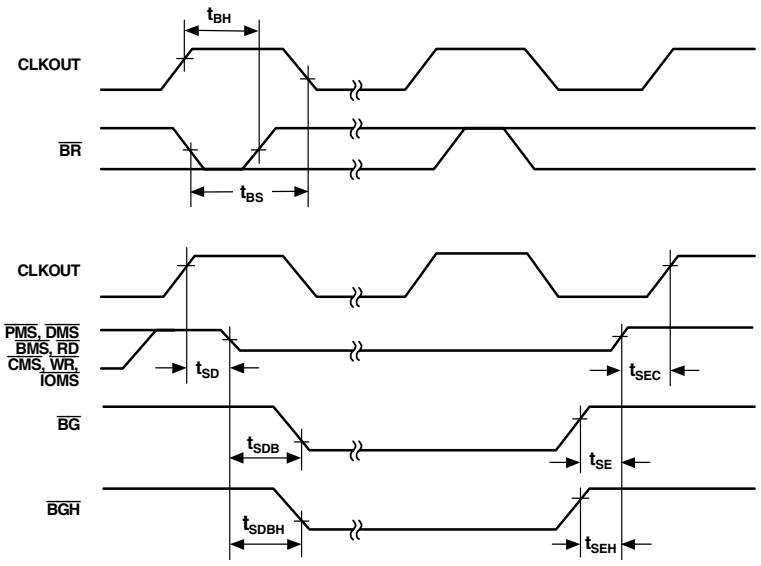

Figure 28. Bus Request–Bus Grant

Memory Read

Table 18. Memory Read

Parameter		Min	Max	Unit
Timing Requirements:				
t_{RDD}	$\overline{RD}$ Low to Data Valid[1]		$0.5t_{CK} - 5 + w$	ns
t_{AA}	A13–0, $\overline{xMS}$ to Data Valid[2]		$0.75t_{CK} - 6 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristics:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 3 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 2$	$0.25t_{CK} + 4$	ns
t_{ASR}	A13–0, $\overline{xMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 3$		ns
t_{RDA}	A13–0, $\overline{xMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 3$		ns

[1] w = wait states 3 t_{CK}.
[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

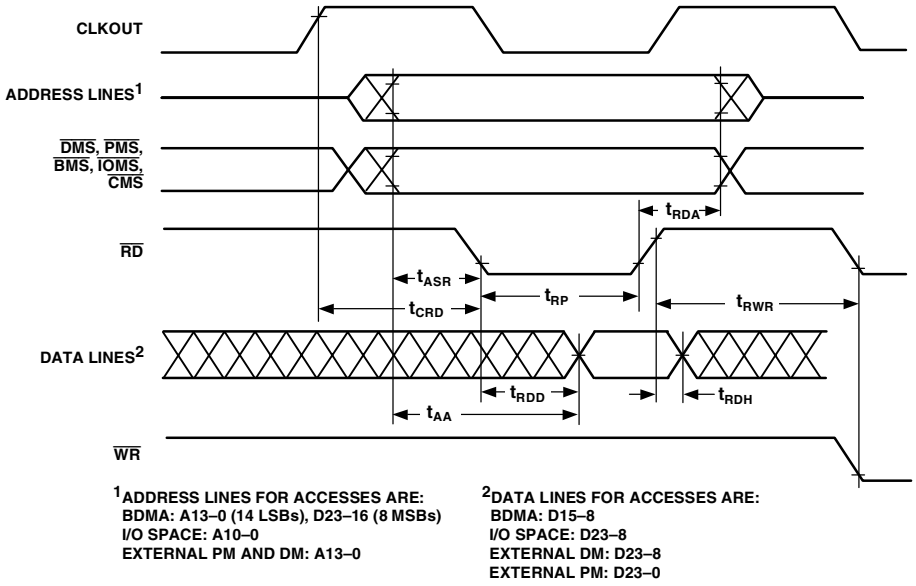

Figure 29. Memory Read

Memory Write

Table 19. Memory Write

Parameter		Min	Max	Unit
Switching Characteristics:				
t_{DW}	Data Setup before $\overline{WR}$ High[1]	$0.5t_{CK}$– 4 + w		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK}$ – 1		ns
t_{WP}	$\overline{WR}$ Pulse Width	$0.5t_{CK}$ – 3 + w		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A13–0, $\overline{xMS}$ Setup before $\overline{WR}$ Low[2]	$0.25t_{CK}$ – 3		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK}$ – 3		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK}$ – 2	$0.25t_{CK}$ + 4	ns
t_{AW}	A13–0, $\overline{xMS}$ Setup before $\overline{WR}$ Deasserted	$0.75t_{CK}$ – 5 + w		ns
t_{WRA}	A13–0, $\overline{xMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK}$ – 1		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK}$ – 3		ns

[1] w = wait states 3 t_{CK}.
[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

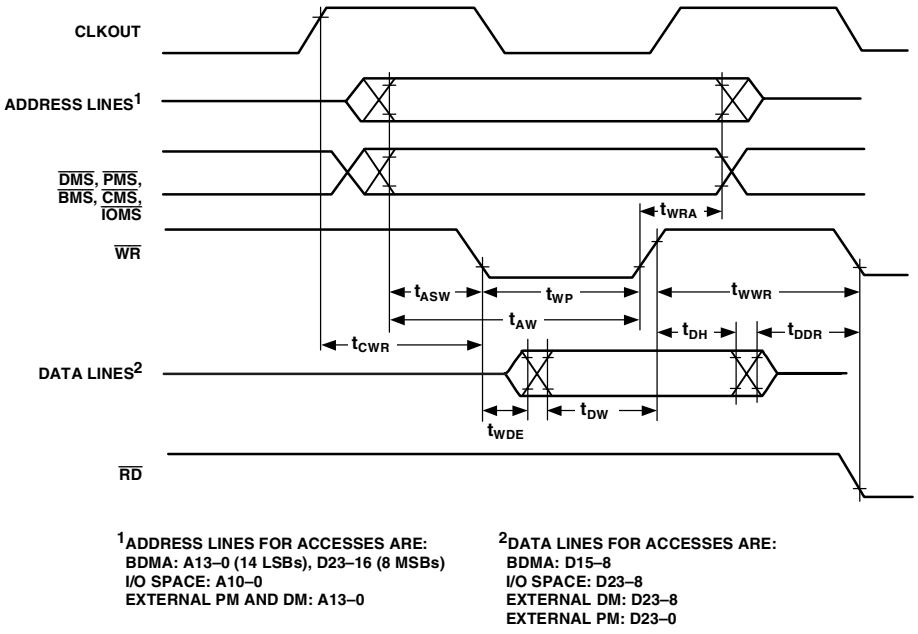

Figure 30. Memory Write

Serial Ports

Table 20. Serial Ports

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SCK}	SCLK Period	30		ns
t_{SCS}	DR/TFS/RFS Setup Before SCLK Low	4		ns
t_{SCH}	DR/TFS/RFS Hold After SCLK Low	7		ns
t_{SCP}	SCLKIN Width	12		ns
Switching Characteristics:				
t_{CC}	CLKOUT High to SCLKOUT	$0.25t_{CK}$	$0.25t_{CK} + 6$	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		7	ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		7	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS (Alt) to DT Enable	0		ns
t_{TDV}	TFS (Alt) to DT Valid		7	ns
t_{SCDD}	SCLK High to DT Disable		7	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		7	ns

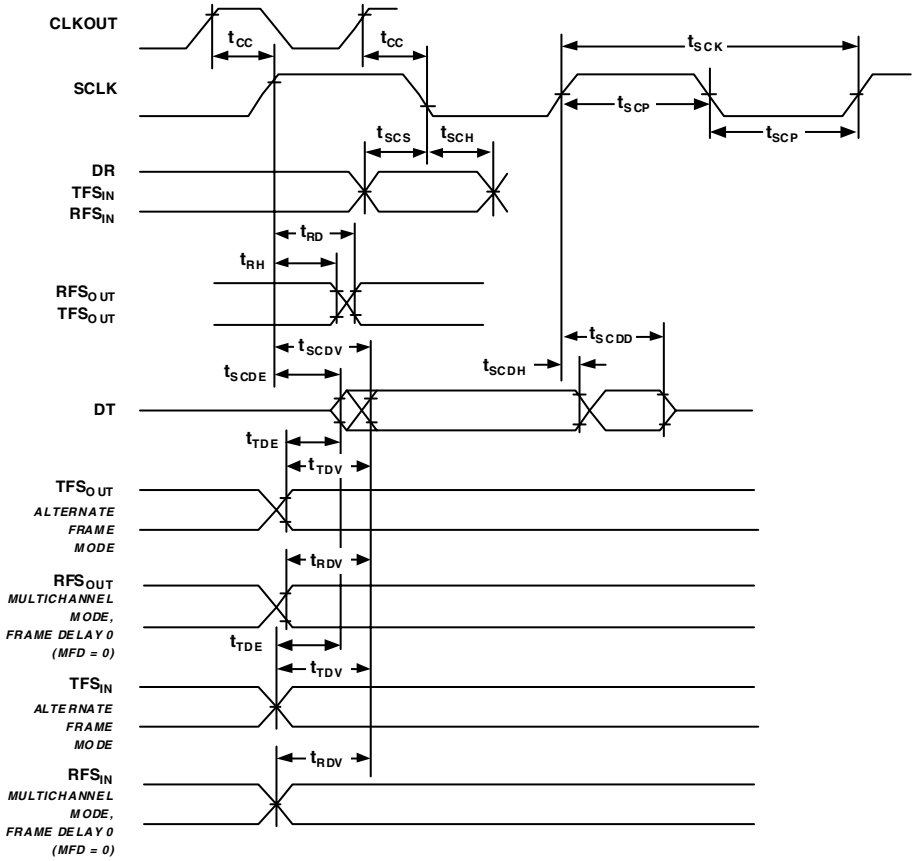

Figure 31. Serial Ports

IDMA Write, Short Write Cycle

Table 22. IDMA Write, Short Write Cycle

Parameter		Min	Max	Unit
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low Before Start of Write[1]	0		ns
t_{IWP}	Duration of Write[1, 2]	10		ns
t_{IDSU}	IAD15–0 Data Setup Before End of Write[2, 3, 4]	3		ns
t_{IDH}	IAD15–0 Data Hold After End of Write[2, 3, 4]	2		ns
Switching Characteristic:				
t_{IKHW}	Start of Write to $\overline{IACK}$ High		10	ns

[1] Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2] End of Write = $\overline{IS}$ High or $\overline{IWR}$ High.
[3] If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[4] If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.

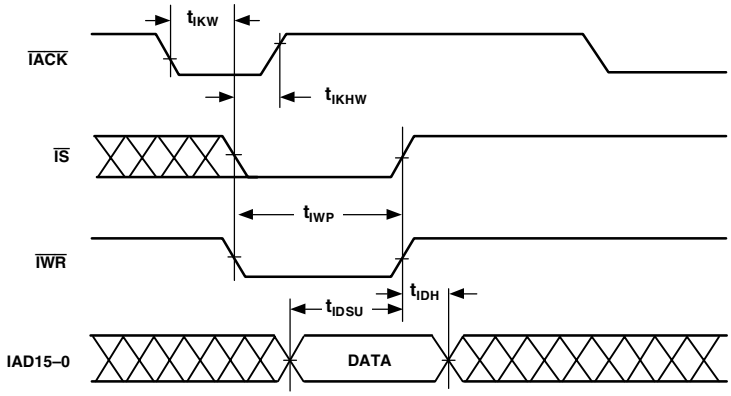

Figure 33. IDMA Write, Short Write Cycle

IDMA Write, Long Write Cycle

Table 23. IDMA Write, Long Write Cycle

Parameter		Min	Max	Unit
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low Before Start of Write[1]	0		ns
t_{IKSU}	IAD15–0 Data Setup Before End of Write[2, 3, 4]	$0.5t_{CK} + 5$		ns
t_{IKH}	IAD15–0 Data Hold After End of Write[2, 3, 4]	0		ns
Switching Characteristics:				
t_{IKLW}	Start of Write to $\overline{IACK}$ Low[4]	$1.5t_{CK}$		ns
t_{IKHW}	Start of Write to $\overline{IACK}$ High		10	ns

[1] Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2] If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[3] If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.
[4] This is the earliest time for $\overline{IACK}$ Low from Start of Write. For IDMA Write cycle relationships, please refer to the *ADSP-2100 Family User's Manual*.

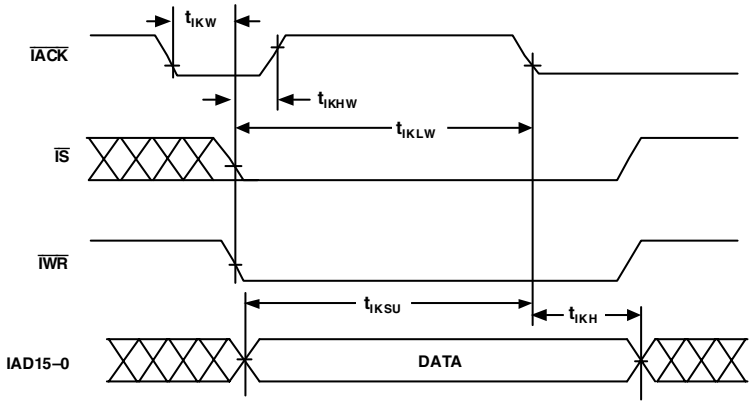

Figure 34. IDMA Write, Long Write Cycle

IDMA Read, Short Read Cycle

Table 25. IDMA Read, Short Read Cycle

Parameter[1, 2]		Min	Max	Unit
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low Before Start of Read[3]	0		ns
t_{IRP1}	Duration of Read (DM/PM1)[4]	10	$2t_{CK} - 5$	ns
t_{IRP2}	Duration of Read (PM2)[5]	10	$t_{CK} - 5$	ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High After Start of Read[3]		10	ns
t_{IKDH}	IAD15–0 Data Hold After End of Read[6]	0		ns
t_{IKDD}	IAD15–0 Data Disabled After End of Read[6]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled After Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid After Start of Read		10	ns

[1] Short Read Only must be disabled in the IDMA overlay memory mapped register. This mode is disabled by clearing (=0) Bit 14 of the IDMA overlay register, and is disabled by default upon reset.
[2] Consider using the Short Read Only mode, instead, because Short Read mode is not applicable at high clock frequencies.
[3] Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[4] DM Read or first half of PM Read.
[5] Second half of PM Read.
[6] End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

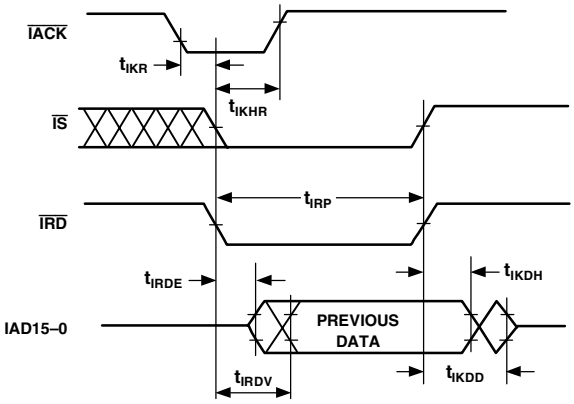

Figure 36. IDMA Read, Short Read Cycle

IDMA Read, Short Read Cycle in Short Read Only Mode

Table 26. IDMA Read, Short Read Cycle in Short Read Only Mode

Parameter[1]		Min	Max	Unit
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low Before Start of Read[2]	0		ns
t_{IRP}	Duration of Read[3]	10		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High After Start of Read[2]		10	ns
t_{IKDH}	IAD15–0 Previous Data Hold After End of Read[3]	0		ns
t_{IKDD}	IAD15–0 Previous Data Disabled After End of Read[3]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled After Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid After Start of Read		10	ns

[1] Short Read Only is enabled by setting Bit 14 of the IDMA overlay Register to 1 (0x3FE7). Short Read Only can be enabled by the processor core writing to the register or by an external host writing to the register. Disabled by default.
[2] Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low. Previous data remains until end of read.
[3] End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

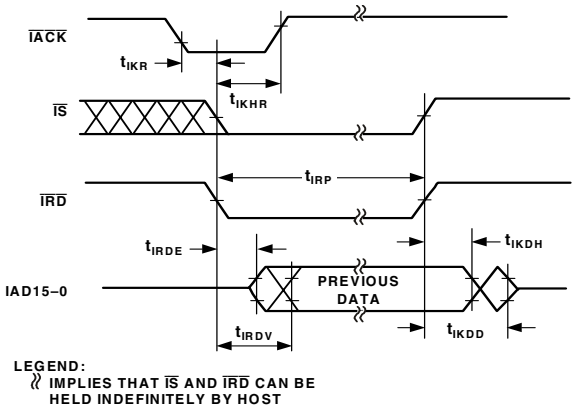

Figure 37. IDMA Read, Short Read Cycle in Short Read Only Mode

ORDERING GUIDE

Model	Temperature Range[1]	Instruction Rate (MHz)	Package Description	Package Option
ADSP-2184NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2184NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2184NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2184NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2184NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2185NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2185NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2185NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2185NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2185NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2185NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2186NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2186NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2186NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2186NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2186NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2186NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2187NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2187NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2187NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2187NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2187NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2187NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2188NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2188NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2188NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2188NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2188NKCAZ-320[2]	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2188NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2188NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2189NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2189NBCAZ-320[2]	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2189NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2189NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2189NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2189NKCAZ-320[2]	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2189NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2189NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1

[1] Ranges shown represent ambient temperature.
[2] Z = Pb-free part.

C02666-0-8/06(A)