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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, Serial Port
Clock Rate	80MHz
Non-Volatile Memory	External
On-Chip RAM	192kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.80V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2189nkstz-320

such as SCLK, CLKOUT, and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard IDLE instruction.

When the IDLE (n) instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts. The one-cycle response time of the standard idle state is increased by n, the clock divisor. When an enabled interrupt is received, ADSP-218xN series members remain in the idle state for up to a maximum of n processor cycles (n = 16, 32, 64, or 128) before resuming normal operation.

When the IDLE (n) instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of n processor cycles).

SYSTEM INTERFACE

Figure 2 shows typical basic system configurations with the ADSP-218xN series, two serial devices, a byte-wide EPROM, and optional external program and data overlay memories (mode-selectable). Programmable wait state generation allows the processor to connect easily to slow peripheral devices. ADSP-218xN series members also provide four external interrupts and two serial ports or six external interrupts and one serial port. Host Memory Mode allows access to the full external data bus, but limits addressing to a single address bit (A0). Through the use of external hardware, additional system peripherals can be added in this mode to generate and latch address signals.

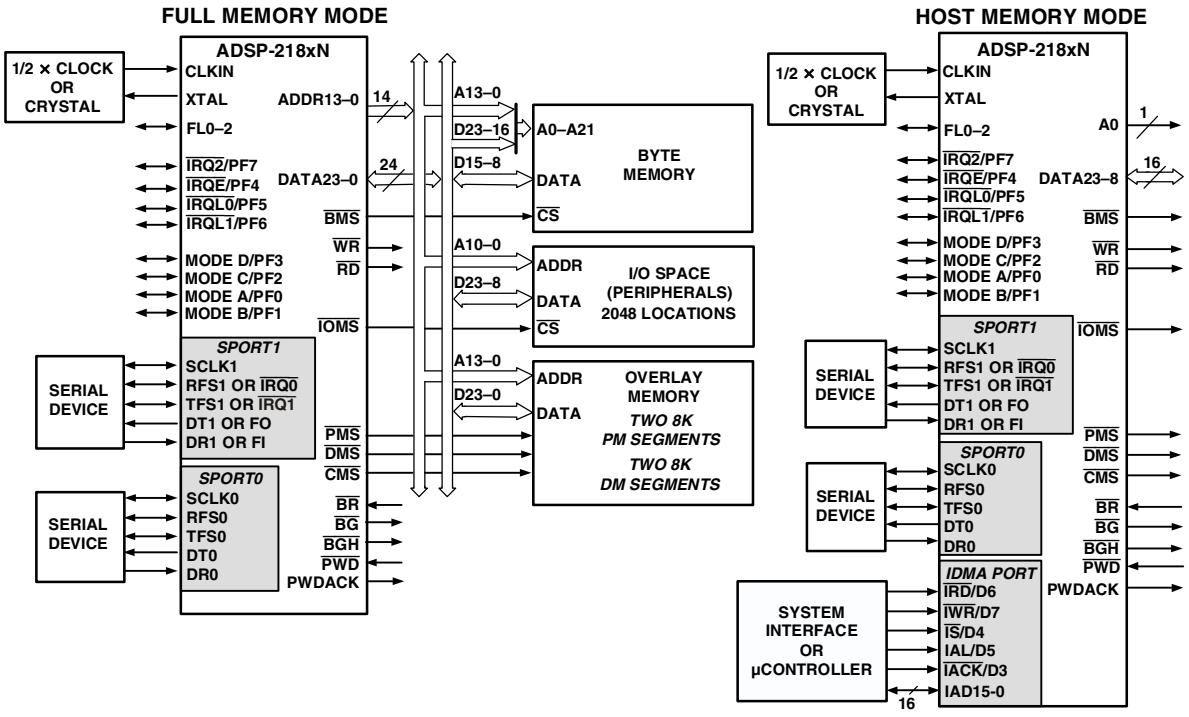

Figure 2. Basic System Interface

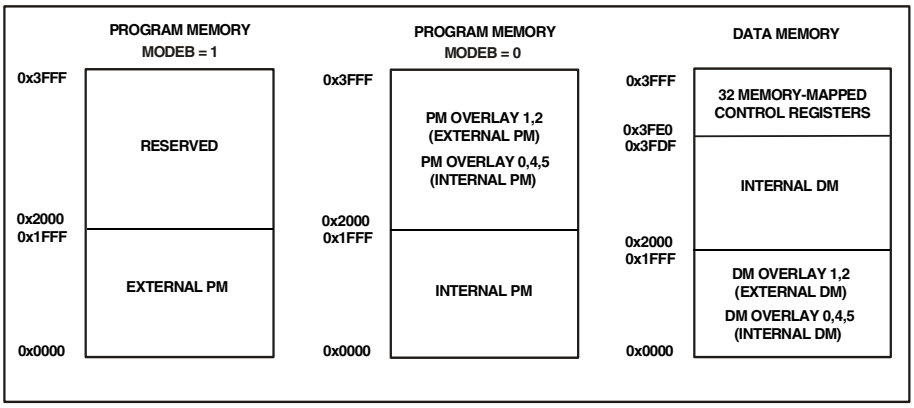

Figure 7. ADSP-2187 Memory Architecture

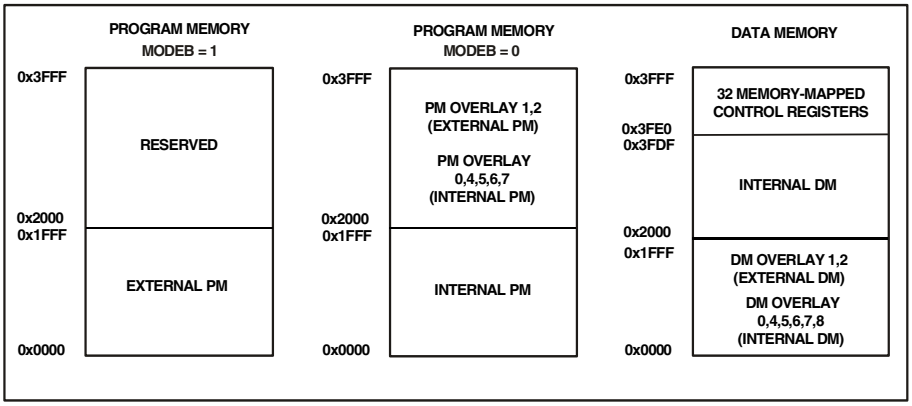

Figure 8. ADSP-2188 Memory Architecture

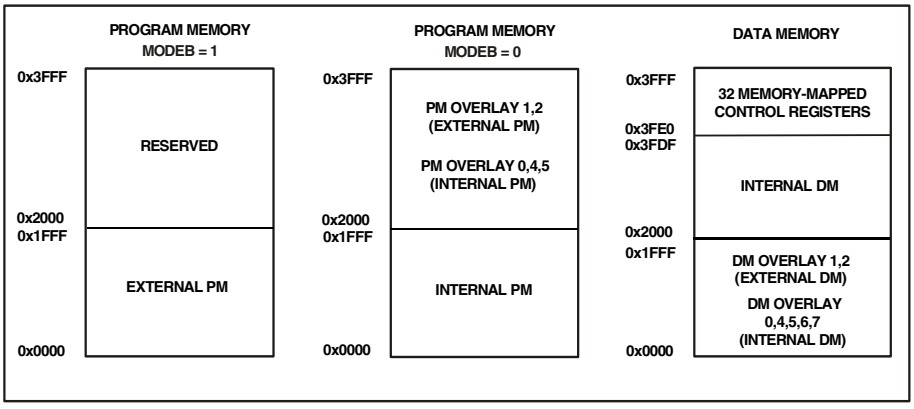

Figure 9. ADSP-2189 Memory Architecture

Program Memory

Program Memory (Full Memory Mode) is a 24-bit-wide space for storing both instruction opcodes and data. The member DSPs of this series have up to 48K words of Program Memory RAM on chip, and the capability of accessing up to two 8K external memory overlay spaces, using the external data bus.

The EZ-ICE uses the EE (emulator enable) signal to take control of the ADSP-218xN in the target system. This causes the processor to use its $\overline{\text{ERESET}}$, $\overline{\text{EBR}}$, and $\overline{\text{EBG}}$ pins instead of the $\overline{\text{RESET}}$, $\overline{\text{BR}}$, and $\overline{\text{BG}}$ pins. The $\overline{\text{BG}}$ output is three-stated. These signals do not need to be jumper-isolated in the system.

The EZ-ICE connects to the target system via a ribbon cable and a 14-pin female plug. The female plug is plugged onto the 14-pin connector (a pin strip header) on the target board.

Target Board Connector for EZ-ICE Probe

The EZ-ICE connector (a standard pin strip header) is shown in Figure 16. This connector must be added to the target board design to use the EZ-ICE. Be sure to allow enough room in the system to fit the EZ-ICE probe onto the 14-pin connector.

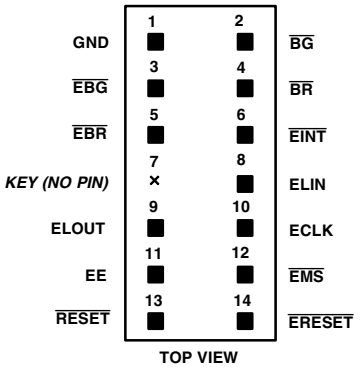

Figure 16. Target Board Connector for EZ-ICE

The 14-pin, 2-row pin strip header is keyed at the Pin 7 location—Pin 7 must be removed from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inch. The pin strip header must have at least 0.15 inch clearance on all sides to accept the EZ-ICE probe plug.

Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec.

Target Memory Interface

For the target system to be compatible with the EZ-ICE emulator, it must comply with the following memory interface guidelines:

Design the Program Memory (PM), Data Memory (DM), Byte Memory (BM), I/O Memory (IOM), and Composite Memory (CM) external interfaces to comply with worst-case device timing requirements and switching characteristics as specified in this data sheet. The performance of the EZ-ICE may approach published worst-case specification for some memory access timing requirements and switching characteristics.

Note: If the target does not meet the worst-case chip specification for memory access parameters, the circuitry may not be able to be emulated at the desired CLKIN frequency. Depending on the severity of the specification violation, the system may be difficult to manufacture, as DSP components statistically vary in switching characteristic and timing requirements, within published limits.

Restriction: All memory strobe signals on the ADSP-218xN ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{CMS}}$, and $\overline{\text{IOMS}}$) used in the target system must have 10 kΩ pull-up resistors connected when the EZ-ICE is being used. The pull-up resistors are necessary because there are no internal pull-ups to guarantee their state during prolonged three-state conditions resulting from typical EZ-ICE debugging sessions. These resistors may be removed when the EZ-ICE is not being used.

Target System Interface Signals

When the EZ-ICE board is installed, the performance on some system signals changes. Design the system to be compatible with the following system interface signal changes introduced by the EZ-ICE board:

- EZ-ICE emulation introduces an 8 ns propagation delay between the target circuitry and the DSP on the $\overline{\text{RESET}}$ signal.
- EZ-ICE emulation introduces an 8 ns propagation delay between the target circuitry and the DSP on the $\overline{\text{BR}}$ signal.
- EZ-ICE emulation ignores $\overline{\text{RESET}}$ and $\overline{\text{BR}}$, when single-stepping.
- EZ-ICE emulation ignores $\overline{\text{RESET}}$ and $\overline{\text{BR}}$ when in Emulator Space (DSP halted).
- EZ-ICE emulation ignores the state of target $\overline{\text{BR}}$ in certain modes. As a result, the target system may take control of the DSP's external memory bus only if bus grant ($\overline{\text{BG}}$) is asserted by the EZ-ICE board's DSP.

ADDITIONAL INFORMATION

This data sheet provides a general overview of ADSP-218xN series functionality. For additional information on the architecture and instruction set of the processor, refer to the *ADSP-218x DSP Hardware Reference and the* ADSP-218x DSP Instruction Set Reference.

Table 12. Unused Pin Terminations (Continued)

Pin Name[1]	I/O 3-State (Z)[2]	Reset State	Hi-Z[3] Caused By	Unused Configuration
D23–8	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
D7 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IWR}$	I	I		High (Inactive)
D6 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IRD}$	I	I	$\overline{BR}$, $\overline{EBR}$	High (Inactive)
D5 or	I/O (Z)	Hi-Z		Float
IAL	I	I		Low (Inactive)
D4 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IS}$	I	I		High (Inactive)
D3 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IACK}$				Float
D2–0 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
IAD15–13	I/O (Z)	Hi-Z	$\overline{IS}$	Float
$\overline{PMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{DMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IOMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{CMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{RD}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{WR}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BR}$	I	I		High (Inactive)
$\overline{BG}$	O (Z)	O	EE	Float
$\overline{BGH}$	O	O		Float
$\overline{IRQ2}$/*PF7*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float[5]
$\overline{IRQL1}$/*PF6*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float[5]
$\overline{IRQL0}$/*PF5*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float[5]
$\overline{IRQE}$/*PF4*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float[5]
$\overline{PWD}$	I	I		High
SCLK0	I/O	I		Input = High or Low, Output = Float
RFS0	I/O	I		High or Low
DR0	I	I		High or Low
TFS0	I/O	I		High or Low
DT0	O	O		Float
SCLK1	I/O	I		Input = High or Low, Output = Float
RFS1/$\overline{IRQ0}$	I/O	I		High or Low
DR1/FI	I	I		High or Low
TFS1/$\overline{IRQ1}$	I/O	I		High or Low
DT1/FO	O	O		Float
EE	I	I		Float
$\overline{EBR}$	I	I		Float
$\overline{EBG}$	O	O		Float

Table 12. Unused Pin Terminations (Continued)

Pin Name[1]	I/O 3-State (Z)[2]	Reset State	Hi-Z[3] Caused By	Unused Configuration
$\overline{\text{ERESET}}$	I	I		Float
$\overline{\text{EMS}}$	O	O		Float
$\overline{\text{EINT}}$	I	I		Float
ECLK	I	I		Float
ELIN	I	I		Float
ELOUT	O	O		Float

[1] CLKIN, $\overline{\text{RESET}}$, and PF3 – 0/Mode D – A are not included in this table because these pins must be used.
[2] All bidirectional pins have three-stated outputs. When the pin is configured as an output, the output is Hi-Z (high impedance) when inactive.
[3] Hi-Z = High Impedance.
[4] If the CLKOUT pin is not used, turn it OFF, using CLKODIS in SPORT0 autobuffer control register.
[5] If the Interrupt/Programmable Flag pins are not used, there are two options: Option 1: When these pins are configured as INPUTS at reset and function as interrupts and input flag pins, pull the pins High (inactive). Option 2: Program the unused pins as OUTPUTS, set them to 1 prior to enabling interrupts, and let pins float.

Parameter[1]	Description	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Supply Current (Idle)[9]	@ V_{DDINT} = 1.9 V, t_{CK} = 12.5 ns, T_{AMB} = 25°C		6.5		mA
I_{DD}	Supply Current (Dynamic)[10]	@ V_{DDINT} = 1.9 V, t_{CK} = 12.5 ns[11], T_{AMB} = 25°C		26		mA
I_{DD}	Supply Current (Power-Down)[12]	@ V_{DDINT} = 1.8 V, T_{AMB} = 25°C in Lowest Power Mode		100		µA
C_I	Input Pin Capacitance[3, 6]	@ V_{IN} = 1.8 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C			8	pF
C_O	Output Pin Capacitance[6, 7, 12, 13]	@ V_{IN} = 1.8 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C			8	pF

[1] Specifications subject to change without notice.
[2] Bidirectional pins: D23–0, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A13–1, PF7–0.
[3] Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.
[4] Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2–FL0, $\overline{\text{BGH}}$.
[5] Although specified for TTL outputs, all ADSP-218xN outputs are CMOS-compatible and will drive to V_{DDEXT} and GND, assuming no dc loads.
[6] Guaranteed but not tested.
[7] Three-statable pins: A13–A1, D23–D0, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1, PF7–PF0.
[8] 0 V on $\overline{\text{BR}}$.
[9] Idle refers to ADSP-218xN state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.
[10] I_{DD} measurement taken with all instructions executing from internal memory. 50% of the instructions are multifunction (Types 1, 4, 5, 12, 13, 14), 30% are Type 2 and Type 6, and 20% are idle instructions.
[11] V_{IN} = 0 V and 3 V. For typical values for supply currents, refer to *Power Dissipation* section.
[12] See *ADSP-218x DSP Hardware Reference* for details.
[13] Output pin capacitance is the capacitive load for any three-stated output pin.

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
Internal Supply Voltage (V_{DDINT})[1]	–0.3 V to +2.2 V
External Supply Voltage (V_{DDEXT})	–0.3 V to +4.0 V
Input Voltage[2]	–0.5 V to +4.0 V
Output Voltage Swing[3]	–0.5 V to V_{DDEXT} +0.5 V
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C

[1] Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2] Applies to Bidirectional pins (D23–0, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A13–1, PF7–0) and Input only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$).
[3] Applies to Output pins ($\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2–0, $\overline{\text{BGH}}$).

ESD SENSITIVITY

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-218xN features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

This section contains timing information for the DSP's external signals.

General Notes

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, parameters cannot be added up meaningfully to derive longer times.

Timing Notes

Switching characteristics specify how the processor changes its signals. Designers have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell what the processor will do in a given circumstance. Switching characteristics can also be used to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Frequency Dependency For Timing Specifications

t_{CK} is defined as 0.5 t_{CKI}. The ADSP-218xN uses an input clock with a frequency equal to half the instruction rate. For example, a 40 MHz input clock (which is equivalent to 25 ns) yields a 12.5 ns processor cycle (equivalent to 80 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain the specification value.

Example: t_{CKH} = 0.5 t_{CK} – 2 ns = 0.5 (12.5 ns) – 2 ns = 4.25 ns

Output Drive Currents

Figure 21 shows typical I-V characteristics for the output drivers on the ADSP-218xN series.The curves represent the current drive capability of the output drivers as a function of output voltage.

Figure 23 shows the typical power-down supply current.

Capacitive Loading

Figure 24 and Figure 25 show the capacitive loading characteristics of the ADSP-218xN.

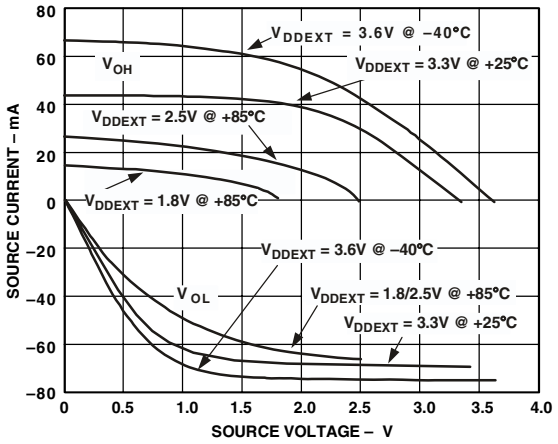

Figure 21. Typical Output Driver Characteristics for V_{DDEXT} at 3.6 V, 3.3 V, 2.5 V, and 1.8 V

Memory Read

Table 18. Memory Read

Parameter		Min	Max	Unit
Timing Requirements:				
t_{RDD}	$\overline{RD}$ Low to Data Valid[1]		$0.5t_{CK} - 5 + w$	ns
t_{AA}	A13–0, $\overline{xMS}$ to Data Valid[2]		$0.75t_{CK} - 6 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristics:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 3 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 2$	$0.25t_{CK} + 4$	ns
t_{ASR}	A13–0, $\overline{xMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 3$		ns
t_{RDA}	A13–0, $\overline{xMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 3$		ns

[1] w = wait states 3 t_{CK}.
[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

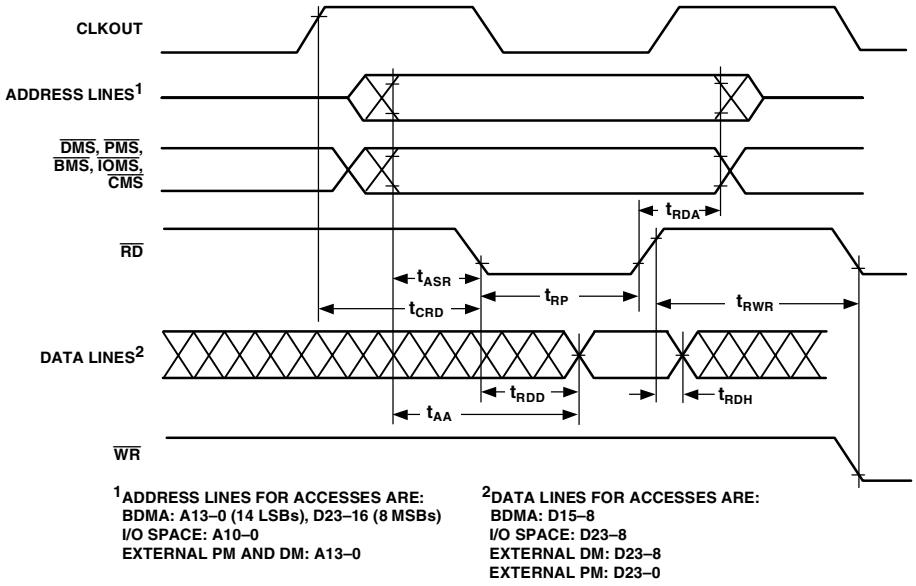

Figure 29. Memory Read

Memory Write

Table 19. Memory Write

Parameter		Min	Max	Unit
Switching Characteristics:				
t_{DW}	Data Setup before $\overline{WR}$ High[1]	$0.5t_{CK}$– 4 + w		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK}$ – 1		ns
t_{WP}	$\overline{WR}$ Pulse Width	$0.5t_{CK}$ – 3 + w		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A13–0, $\overline{xMS}$ Setup before $\overline{WR}$ Low[2]	$0.25t_{CK}$ – 3		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK}$ – 3		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK}$ – 2	$0.25t_{CK}$ + 4	ns
t_{AW}	A13–0, $\overline{xMS}$ Setup before $\overline{WR}$ Deasserted	$0.75t_{CK}$ – 5 + w		ns
t_{WRA}	A13–0, $\overline{xMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK}$ – 1		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK}$ – 3		ns

[1] w = wait states 3 t_{CK}.
[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

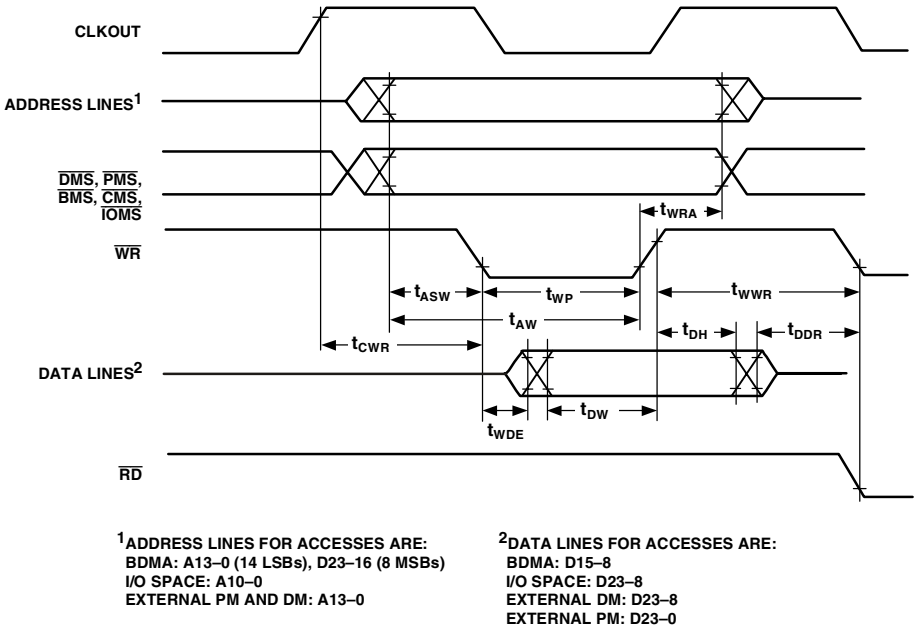

Figure 30. Memory Write

IDMA Address Latch

Table 21. IDMA Address Latch

Parameter		Min	Max	Unit
Timing Requirements:				
t_{IALP}	Duration of Address Latch[1, 2]	10		ns
t_{IASU}	IAD15–0 Address Setup Before Address Latch End[2]	5		ns
t_{IAH}	IAD15–0 Address Hold After Address Latch End[2]	3		ns
t_{IKA}	$\overline{IACK}$ Low before Start of Address Latch[2, 3]	0		ns
t_{IALS}	Start of Write or Read After Address Latch End[2, 3]	3		ns
t_{IALD}	Address Latch Start After Address Latch End[1, 2]	2		ns

[1] Start of Address Latch = $\overline{IS}$ Low and IAL High.
[2] End of Address Latch = $\overline{IS}$ High or IAL Low.
[3] Start of Write or Read = $\overline{IS}$ Low and $\overline{IWR}$ Low or $\overline{IRD}$ Low.

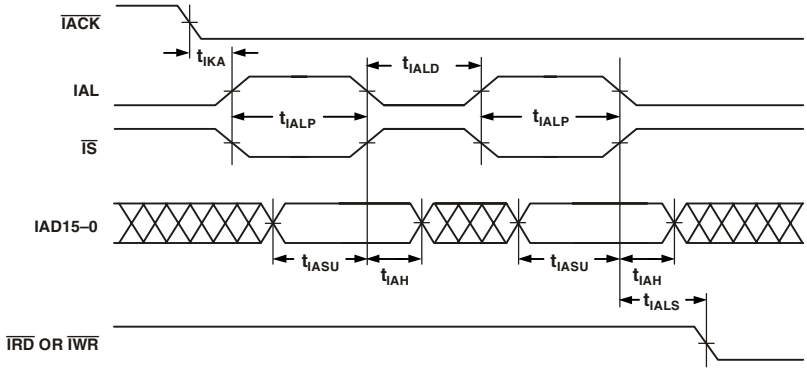

Figure 32. IDMA Address Latch

IDMA Write, Short Write Cycle

Table 22. IDMA Write, Short Write Cycle

Parameter		Min	Max	Unit
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low Before Start of Write[1]	0		ns
t_{IWP}	Duration of Write[1, 2]	10		ns
t_{IDSU}	IAD15–0 Data Setup Before End of Write[2, 3, 4]	3		ns
t_{IDH}	IAD15–0 Data Hold After End of Write[2, 3, 4]	2		ns
Switching Characteristic:				
t_{IKHW}	Start of Write to $\overline{IACK}$ High		10	ns

[1] Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2] End of Write = $\overline{IS}$ High or $\overline{IWR}$ High.
[3] If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[4] If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.

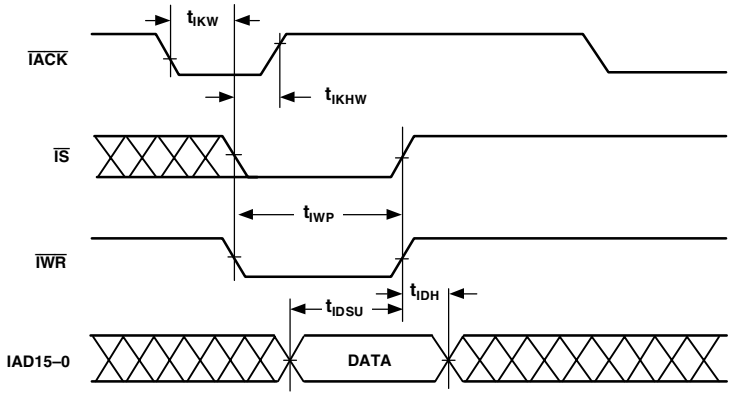

Figure 33. IDMA Write, Short Write Cycle

IDMA Write, Long Write Cycle

Table 23. IDMA Write, Long Write Cycle

Parameter		Min	Max	Unit
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low Before Start of Write[1]	0		ns
t_{IKSU}	IAD15–0 Data Setup Before End of Write[2, 3, 4]	$0.5t_{CK} + 5$		ns
t_{IKH}	IAD15–0 Data Hold After End of Write[2, 3, 4]	0		ns
Switching Characteristics:				
t_{IKLW}	Start of Write to $\overline{IACK}$ Low[4]	$1.5t_{CK}$		ns
t_{IKHW}	Start of Write to $\overline{IACK}$ High		10	ns

[1] Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2] If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[3] If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.
[4] This is the earliest time for $\overline{IACK}$ Low from Start of Write. For IDMA Write cycle relationships, please refer to the *ADSP-2100 Family User's Manual*.

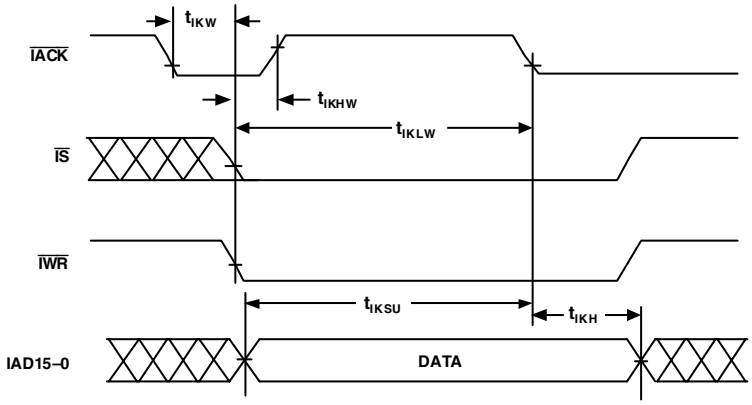

Figure 34. IDMA Write, Long Write Cycle

IDMA Read, Short Read Cycle in Short Read Only Mode

Table 26. IDMA Read, Short Read Cycle in Short Read Only Mode

Parameter[1]		Min	Max	Unit
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low Before Start of Read[2]	0		ns
t_{IRP}	Duration of Read[3]	10		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High After Start of Read[2]		10	ns
t_{IKDH}	IAD15–0 Previous Data Hold After End of Read[3]	0		ns
t_{IKDD}	IAD15–0 Previous Data Disabled After End of Read[3]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled After Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid After Start of Read		10	ns

[1] Short Read Only is enabled by setting Bit 14 of the IDMA overlay Register to 1 (0x3FE7). Short Read Only can be enabled by the processor core writing to the register or by an external host writing to the register. Disabled by default.
[2] Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low. Previous data remains until end of read.
[3] End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

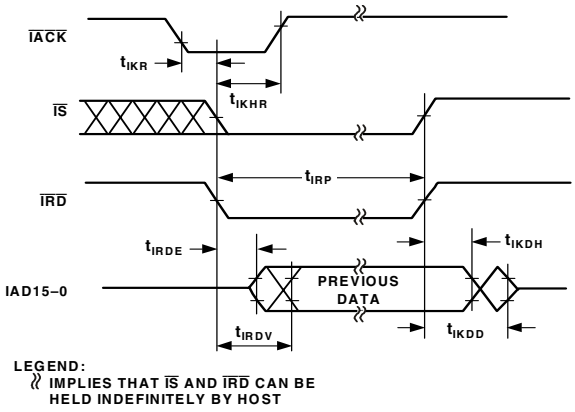

Figure 37. IDMA Read, Short Read Cycle in Short Read Only Mode

LQFP PACKAGE PINOUT

The LQFP package pinout is shown Figure 38 and in Table 27. Pin names in bold text in the table replace the plain-text-named functions when Mode C = 1. A + sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$. The multiplexed pins DT1/FO, TFS1/$\overline{\text{IRQ1}}$, RFS1/$\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default, upon reset.

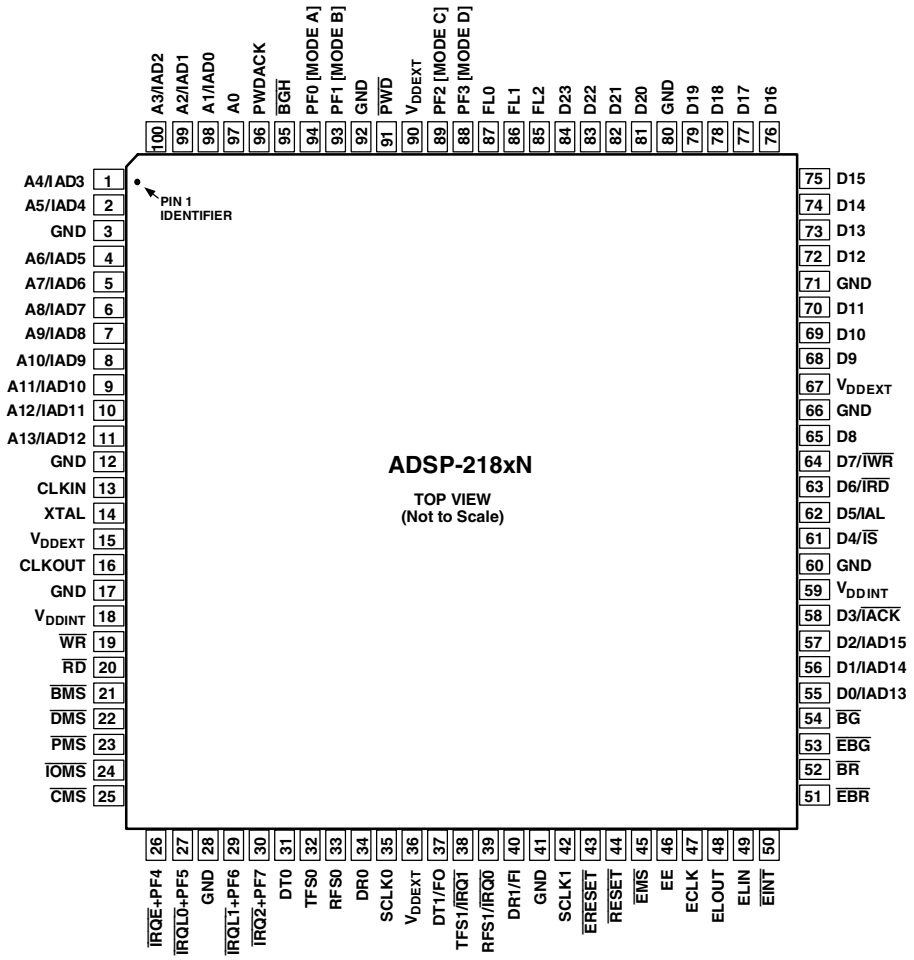

Figure 38. 100-Lead LQFP Pin Configuration

Table 27. LQFP Package Pinout

Pin No.	Pin Name
1	A4/**IAD3**
2	A5/**IAD4**
3	GND
4	A6/**IAD5**
5	A7/**IAD6**
6	A8/**IAD7**
7	A9/**IAD8**
8	A10/**IAD9**
9	A11/**IAD10**
10	A12/**IAD11**
11	A13/**IAD12**
12	GND
13	CLKIN
14	XTAL
15	V_{DDEXT}
16	CLKOUT
17	GND
18	V_{DDINT}
19	$\overline{WR}$
20	$\overline{RD}$
21	$\overline{BMS}$
22	$\overline{DMS}$
23	$\overline{PMS}$
24	$\overline{IOMS}$
25	$\overline{CMS}$
26	$\overline{IRQE}$ + PF4
27	$\overline{IRQL0}$ + PF5
28	GND
29	$\overline{IRQL1}$ + PF6
30	$\overline{IRQ2}$ + PF7
31	DT0
32	TFS0
33	RFS0
34	DR0
35	SCLK0
36	V_{DDEXT}
37	DT1/FO
38	TFS1/$\overline{IRQ1}$
39	RFS1/$\overline{IRQ0}$
40	DR1/FI
41	GND
42	SCLK1
43	$\overline{ERESET}$
44	$\overline{RESET}$
45	$\overline{EMS}$
46	EE
47	ECLK
48	ELOUT
49	ELIN
50	$\overline{EINT}$

Table 27. LQFP Package Pinout (Continued)

Pin No.	Pin Name
51	$\overline{EBR}$
52	$\overline{BR}$
53	$\overline{EBG}$
54	$\overline{BG}$
55	D0/**IAD13**
56	D1/**IAD14**
57	D2/**IAD15**
58	D3/$\overline{\textbf{IACK}}$
59	V_{DDINT}
60	GND
61	D4/$\overline{\textbf{IS}}$
62	D5/**IAL**
63	D6/$\overline{\textbf{IRD}}$
64	D7/$\overline{\textbf{IWR}}$
65	D8
66	GND
67	V_{DDEXT}
68	D9
69	D10
70	D11
71	GND
72	D12
73	D13
74	D14
75	D15
76	D16
77	D17
78	D18
79	D19
80	GND
81	D20
82	D21
83	D22
84	D23
85	FL2
86	FL1
87	FL0
88	PF3 [Mode D]
89	PF2 [Mode C]
90	V_{DDEXT}
91	$\overline{PWD}$
92	GND
93	PF1 [Mode B]
94	PF0 [Mode A]
95	$\overline{BGH}$
96	PWDACK
97	A0
98	A1/**IAD0**
99	A2/**IAD1**
100	A3/**IAD2**

BGA PACKAGE PINOUT

The BGA package pinout is shown in Figure 39 and in Table 28. Pin names in bold text in the table replace the plain text named functions when Mode C = 1. A + sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$. The multiplexed pins DT1/FO, TFS1/$\overline{\text{IRQ1}}$, RFS1/$\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default upon reset.

12	11	10	9	8	7	6	5	4	3	2	1	
GND	GND	D22	NC	NC	NC	GND	NC	A0	GND	A1/IAD0	A2/IAD1	A
D16	D17	D18	D20	D23	V_{DDEXT}	GND	NC	NC	GND	A3/IAD2	A4/IAD3	B
D14	NC	D15	D19	D21	V_{DDEXT}	$\overline{\text{PWD}}$	A7/IAD6	A5/IAD4	$\overline{\text{RD}}$	A6/IAD5	PWDACK	C
GND	NC	D12	D13	NC	PF2 [MODE C]	PF1 [MODE B]	A9/IAD8	$\overline{\text{BGH}}$	NC	$\overline{\text{WR}}$	NC	D
D10	GND	V_{DDEXT}	GND	GND	PF3 [MODE D]	FL2	PF0 [MODE A]	FL0	A8/IAD7	V_{DDEXT}	V_{DDEXT}	E
D9	NC	D8	D11	D7/$\overline{\text{IWR}}$	NC	NC	FL1	A11/IAD10	A12/IAD11	NC	A13/IAD12	F
D4/$\overline{\text{IS}}$	NC	NC	D5/IAL	D6/$\overline{\text{IRD}}$	NC	NC	NC	A10/IAD9	GND	NC	XTAL	G
GND	NC	GND	D3/$\overline{\text{IACK}}$	D2/IAD15	TFS0	DT0	V_{DDINT}	GND	GND	GND	CLKIN	H
V_{DDINT}	V_{DDINT}	D1/IAD14	$\overline{\text{BG}}$	RFS1/$\overline{\text{IRQ0}}$	D0/IAD13	SCLK0	V_{DDEXT}	V_{DDEXT}	NC	V_{DDINT}	CLKOUT	J
$\overline{\text{EBG}}$	$\overline{\text{BR}}$	$\overline{\text{EBR}}$	$\overline{\text{ERESET}}$	SCLK1	TFS1/$\overline{\text{IRQ1}}$	RFS0	$\overline{\text{DMS}}$	$\overline{\text{BMS}}$	NC	NC	NC	K
$\overline{\text{EINT}}$	ELOUT	ELIN	$\overline{\text{RESET}}$	GND	DR0	$\overline{\text{PMS}}$	GND	$\overline{\text{IOMS}}$	$\overline{\text{IRQL1}}$ + PF6	NC	$\overline{\text{IRQE}}$ + PF4	L
ECLK	EE	$\overline{\text{EMS}}$	NC	GND	DR1/FI	DT1/FO	GND	$\overline{\text{CMS}}$	NC	$\overline{\text{IRQ2}}$ + PF7	$\overline{\text{IRQL0}}$ + PF5	M

Figure 39. 144-Ball BGA Package Pinout (Bottom View)

Table 28. BGA Package Pinout (Continued)

Ball No.	Pin Name
J03	NC
J04	V_{DDEXT}
J05	V_{DDEXT}
J06	SCLK0
J07	D0/**IAD13**
J08	RFS1/$\overline{IRQ0}$
J09	$\overline{BG}$
J10	D1/**IAD14**
J11	V_{DDINT}
J12	V_{DDINT}
K01	NC
K02	NC
K03	NC
K04	$\overline{BMS}$
K05	$\overline{DMS}$
K06	RFS0
K07	TFS1/$\overline{IRQ1}$
K08	SCLK1
K09	$\overline{ERESET}$
K10	$\overline{EBR}$
K11	$\overline{BR}$
K12	$\overline{EBG}$
L01	$\overline{IRQE}$ + PF4
L02	NC
L03	$\overline{IRQL1}$ + PF6
L04	$\overline{IOMS}$
L05	GND
L06	$\overline{PMS}$
L07	DR0
L08	GND
L09	$\overline{RESET}$
L10	ELIN
L11	ELOUT
L12	$\overline{EINT}$
M01	$\overline{IRQL0}$ + PF5
M02	$\overline{IRQL2}$ + PF7
M03	NC
M04	$\overline{CMS}$
M05	GND
M06	DT1/FO
M07	DR1/FI
M08	GND
M09	NC
M10	$\overline{EMS}$
M11	EE
M12	ECLK

OUTLINE DIMENSIONS

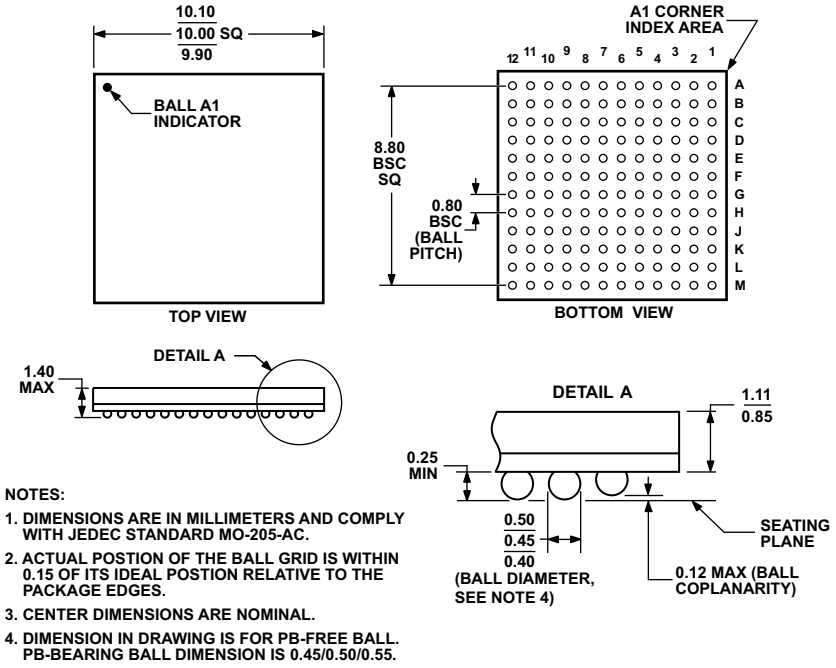

Figure 40. 144-Ball BGA [CSP_BGA] (BC-144-6)

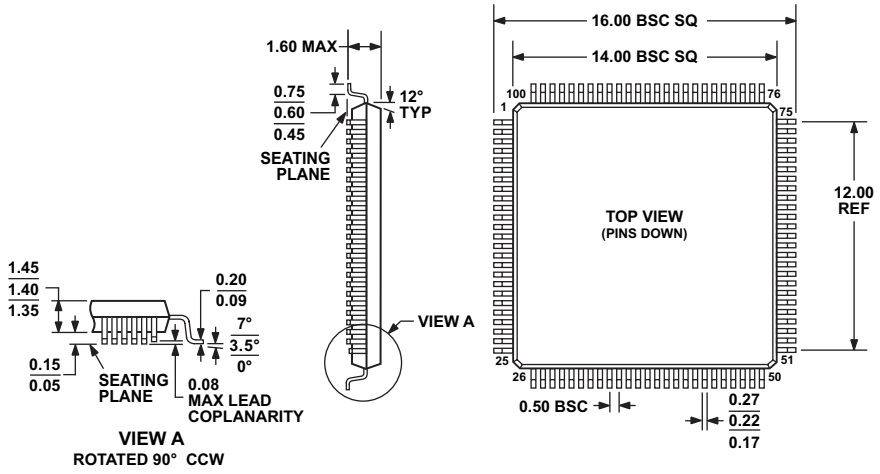

Figure 41. 100-Lead Low Profile Quad Flat Package [LQFP] (ST-100-1)

SURFACE MOUNT DESIGN

Table 29 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard*.

Table 29. BGA Data for Use with Surface Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
144-Ball BGA (BC-144-6)	Solder Mask Defined	0.40 mm diameter	0.50 mm diameter

ORDERING GUIDE

Model	Temperature Range[1]	Instruction Rate (MHz)	Package Description	Package Option
ADSP-2184NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2184NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2184NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2184NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2184NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2185NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2185NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2185NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2185NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2185NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2185NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2186NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2186NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2186NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2186NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2186NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2186NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2187NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2187NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2187NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2187NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2187NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2187NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2188NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2188NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2188NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2188NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2188NKCAZ-320[2]	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2188NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2188NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2189NBCA-320	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2189NBCAZ-320[2]	–40°C to +85°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2189NBST-320	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2189NBSTZ-320[2]	–40°C to +85°C	80	100-Lead LQFP	ST-100-1
ADSP-2189NKCA-320	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2189NKCAZ-320[2]	0°C to 70°C	80	144-Ball CSP_BGA	BC-144-6
ADSP-2189NKST-320	0°C to 70°C	80	100-Lead LQFP	ST-100-1
ADSP-2189NKSTZ-320[2]	0°C to 70°C	80	100-Lead LQFP	ST-100-1

[1] Ranges shown represent ambient temperature.
[2] Z = Pb-free part.