Renesas Electronics America Inc - R5F56104VNFP#V0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	117
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 2x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56104vnfp-v0

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
C6	VSS							
C7		P94					AN12	
C8	BSCANP							
C9		PG3						
C10		PD2		D2				
C11		P62		CS2#-A/ CS6#-A				
C12	VSS							
C13		PD7		D7				
C14		PE3		D11				
C15		PE5	IRQ5-A	D13				
D1		P65	IRQ15-A					
D2		P01	IRQ9-A		TMCI2	RxD6		
D3	AVSS							
D4		P40	IRQ8-B				AN0	
D5		P44	IRQ12-B				AN4	
D6		P91					AN9	
D7		P95					AN13	
D8		PG0						
D9		PG4						
D10		PD3		D3				
D11		P64		CS4#-B				
D12		PE4		D12				
D13		PE6	IRQ6-A	D14				
D14		PE7	IRQ7-A	D15				
D15		PG5						
E1	VSS							
E2	WDTOVF#							TDO
E3	EMLE							
E4		P00	IRQ8-A		TMRI2	TxD6		
E12	VCC							
E13		PG7						
E14		PG6						
E15	VSS							
F1	MD1							
F2	MD0							
F3	VCL							
F4	MDE							
F12		PA3		A3	PO19/ TIOCC6/ TIOCD6/ TCLKF			

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
M6		P37			PO15/ TIOCA2/ TIOCB2/ TCLKD-A			
M7		P57		WAIT#				TRDATA3
M8		P83						
M9		P81						TRSYNC
M10		P51		WR1#/BC1#				
M11		PH4						
M12		PC7		A23/ CS4#-D/ CS7#-D		TxD5		
M13	VSS							
M14		PC0		A16				
M15		PB6		A14	PO30/ TIOCA11			
N1		P25			PO5/ TIOCA4/ TMCI1	RxD1		
N2		P24			PO4/ TIOCA4/ TIOCB4/ TMRI1			
N3		P20			PO0/ TIOCA3/ TIOCB3/ TMRI0	TxD0		
N4		P16	IRQ6-B		TCLKC-B	RxD3/SDA0		
N5		P12	IRQ2-B			RxD2		
N6		P36			PO14/ TIOCA2			
N7		P56						TRDATA2
N8	VSS							
N9		P80						
N10		P50		WR0#/WR#				
N11	VSS							
N12		P76	IRQ14-A					
N13		PH2						
N14		PC2		A18				
N15		PC1		A17				
P1		P23			PO3/ TIOCC3/ TIOCD3			

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
32		P25			PO5/ TIOCA4/ TMCI1	RxD1		
33		P24			PO4/ TIOCA4/ TIOCB4/ TMRI1			
34		P23			PO3/ TIOCC3/ TIOCD3			
35		P22			PO2/ TIOCC3/ TMO0	SCK0		
36		P21			PO1/ TIOCA3/ TMCI0	RxD0		
37		P20			PO0/ TIOCA3/ TIOCB3/ TMRI0	TxD0		
38		P17	IRQ7-B		TCLKD-B	TxD3/SCL0	ADTRG1#	
39	PLLVCC							
40		P16	IRQ6-B		TCLKC-B	RxD3/SDA0		
41	PLLVSS							
42		P15	IRQ5-B		TCLKB-B	SCK3/SCL1		
43		P14	IRQ4-B		TCLKA-B	SDA1		
44		P13	IRQ3-B			TxD2	ADTRG0#	
45		P12	IRQ2-B			RxD2		
46		P11	IRQ1-B			SCK2		
47		P10	IRQ0-B					
48		P37			PO15/ TIOCA2/ TIOCB2/ TCLKD-A			
49		P36			PO14/ TIOCA2			
50		P35			PO13/ TIOCA1/ TIOCB1/ TCLKC-A			
51		P84						
52		P57		WAIT#				TRDATA3
53		P56						TRDATA2
54		P55						TRDATA1

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
85		PB1		A9	PO25/ TIOCA9/ TIOCB9			
86		P74					ADTRG3#	
87		P73						
88		P72						
89		P71		CS4#-C/ CS5#-C/ CS6#-C/ CS7#-C				
90		P70		CS3#-B			ADTRG2#	
91	VCC							
92		PB0		A8	PO24/ TIOCA9			
93	VSS							
94		PA7		A7	PO23/ TIOCA8/ TIOCB8/ TCLKH			
95		PA6		A6	PO22/ TIOCA8			
96		PA5		A5	PO21/ TIOCA7/ TIOCB7/ TCLKG			
97		PA4		A4	PO20/ TIOCA7			
98		PA3		A3	PO19/ TIOCC6/ TIOCD6/ TCLKF			
99		PA2		A2	PO18/ TIOCC6/ TCLKE			
100		PA1		A1	PO17/ TIOCA6/ TIOCB6			
101		PA0		A0/BC0#	PO16/ TIOCA6			
102		PE7	IRQ7-A	D15				
103		PE6	IRQ6-A	D14				
104		PE5	IRQ5-A	D13				
105		PE4		D12				
106		PE3		D11				
107		PE2		D10				

Classifications	Pin Name	I/O	Description
Bus control	RD#	Output	Strobe signal which indicates that reading from the external address space is in progress.
	WR0#	Output	Strobe signal which indicates that the lower-order byte (D0 to D7) is valid in writing to the external address space, in byte strobe mode.
	WR1#	Output	Strobe signal which indicates that the higher-order byte (D8 to D15) is valid in writing to the external address space, in byte strobe mode.
	WR#	Output	Strobe signal which indicates that writing to the external address space is in progress, in 1-write strobe mode.
	BC0# *1, *2	Output	Strobe signal which indicates that the lower-order byte (D0 to D7) is valid in access to the external address space, in 1-write strobe mode.
	BC1# *2	Output	Strobe signal which indicates that the higher-order byte (D8 to D15) is valid in access to the external address space, in 1-write strobe mode.
	CS0#, CS1# CS2#-A/CS2#-B CS3#-A/CS3#-B CS4#-A/CS4#-B/ CS4#-C/CS4#-D CS5#-A/CS5#-B/ CS5#-C/CS5#-D CS6#-A/CS6#-B/ CS6#-C/CS6#-D CS7#-A/CS7#-B/ CS7#-C/CS7#-D	Output	Select signals for areas 0 to 7
	WAIT#	Input	Requests wait cycles in access to the external address space

Classifications	Pin Name	I/O	Description
Interrupt	NMI	Input	Non-maskable interrupt request signal
	IRQ0-A/IRQ0-B IRQ1-A/IRQ1-B IRQ2-A/IRQ2-B IRQ3-A/IRQ3-B IRQ4-A/IRQ4-B IRQ5-A/IRQ5-B IRQ6-A/IRQ6-B IRQ7-A/IRQ7-B IRQ8-A/IRQ8-B IRQ9-A/IRQ9-B IRQ10-A/IRQ10-B IRQ11-A/IRQ11-B IRQ12-A/IRQ12-B IRQ13-A/IRQ13-B IRQ14-A/IRQ14-B IRQ15-A/IRQ15-B	Input	Maskable request signals
16-bit timer pulse unit	TIOCA0, TIOCB0 TIOCC0, TIOCD0	I/O	Signals for TGRA0 to TGRD0. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA1, TIOCB1	I/O	Signals for TGRA1 and TGRB1. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA2, TIOCB2	I/O	Signals for TGRA2 and TGRB2. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA3, TIOCB3 TIOCC3, TIOCD3	I/O	Signals for TGRA3 to TGRD3. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA4, TIOCB4	I/O	Signals for TGRA4 and TGRB4. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA5, TIOCB5	I/O	Signals for TGRA5 and TGRB5. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA6, TIOCB6 TIOCC6, TIOCD6	I/O	Signals for TGRA6 to TGRD6. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA7, TIOCB7	I/O	Signals for TGRA7 and TGRB7. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA8, TIOCB8	I/O	Signals for TGRA8 and TGRB8. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA9, TIOCB9 TIOCC9, TIOCD9	I/O	Signals for TGRA9 to TGRD9. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA10, TIOCB10	I/O	Signals for TGRA10 and TGRB10. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA11, TIOCB11	I/O	Signals for TGRA11 and TGRB11. These pins are used as input capture inputs, output compare outputs, or PWM outputs.

Classifications	Pin Name	I/O	Description
16-bit timer pulse unit	TCLKA-A/TCLKA-B TCLKB-A/TCLKB-B TCLKC-A/TCLKC-B TCLKD-A/TCLKD-B TCLKE, TCLKF TCLKG, TCLKH	Input	Input pins for external clock signals
Programmable pulse generator	PO0 to PO31	Output	Output pins for the pulse signals
8-bit timer	TMO0 to TMO3	Output	Output pins for the compare match signals
	TMCI0 to TMCI3	Input	Input pins for the external clock signals that drive for the counters
	TMRI0 to TMRI3	Input	Input pins for the counter-reset signals
Watchdog timer	WDTOVF#	Output	Output pin for the counter-overflow signal in watchdog-timer mode
Serial communication interface	TxD0, TxD1, TxD2, TxD3, TxD4, TxD5, TxD6	Output	Output pins for data transmission
	RxD0, RxD1, RxD2, RxD3, RxD4, RxD5, RxD6	Input	Input pins for data reception
	SCK0, SCK1, SCK2, SCK3, SCK4, SCK5, SCK6	I/O	Input/output pins for clock signals
I^2C bus interface	SCL0, SCL1	I/O	Input/output pins for RIIC clocks. Bus can be directly driven by the NMOS open drain output.
	SDA0, SDA1	I/O	Input/output pins for RIIC data. Bus can be directly driven by the NMOS open drain output.
A/D converter	AN0 to AN15	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0# to ADTRG3#	Input	Input pins for the external trigger signals that start the A/D conversion
D/A converter	DA0, DA1	Output	Output pins for the analog signals from the D/A converter

Classifications	Pin Name	I/O	Description
Analog power supply	AVCC	Input	Analog power supply pin for the A/D and D/A converters. When the A/D and D/A converters are not in use, connect this pin to the system power supply.
	AVSS	Input	Ground pin for the A/D and D/A converters. Connect this pin to the system power supply (0 V).
	VREFH	Input	Reference power supply pin for the A/D and D/A converters. When the A/D and D/A converters are not in use, connect this pin to the system power supply.
	VREFL	Input	Reference ground pin for the A/D and D/A converters. Make sure to connect this pin to the analog reference power supply (0 V). When the A/D and D/A converters are not in use, connect this pin to the system power supply (0 V). For details, see section 23.6.7, Ranges of Settings for Analog Power Supply and Other Pins.
I/O ports	P00 to P05	I/O	6-bit input/output pins
	P10 to P17	I/O	8-bit input/output pins
	P20 to P27	I/O	8-bit input/output pins
	P30 to P37	I/O	8-bit input/output pins
	P40 to P47	I/O	8-bit input/output pins
	P50 to P57	I/O	8-bit input/output pins. (P53 is an input-only pin.)
	P60 to P67	I/O	8-bit input/output pins
	P70 to P77	I/O	8-bit input/output pins
	P80 to P86	I/O	7-bit input/output pins
	P90 to P97	I/O	8-bit input/output pins
	PA0 to PA7	I/O	8-bit input/output pins
	PB0 to PB7	I/O	8-bit input/output pins
	PC0 to PC7	I/O	8-bit input/output pins
	PD0 to PD7	I/O	8-bit input/output pins
	PE0 to PE7	I/O	8-bit input/output pins
	PF0 to PF6	I/O	7-bit input/output pins
	PG0 to PG7	I/O	8-bit input/output pins
	PH0 to PH7	I/O	8-bit input/output pins

Note 1: The A0 and BC0# pin functions are multiplexed on the same pin: the A0 pin is valid in byte-write mode and the BC0# pin becomes valid in single write-strobe mode. The setting for an eight-bit external bus width is prohibited in single write-strobe mode. For other multiplexed pin functions, refer to section 14, I/O Ports.

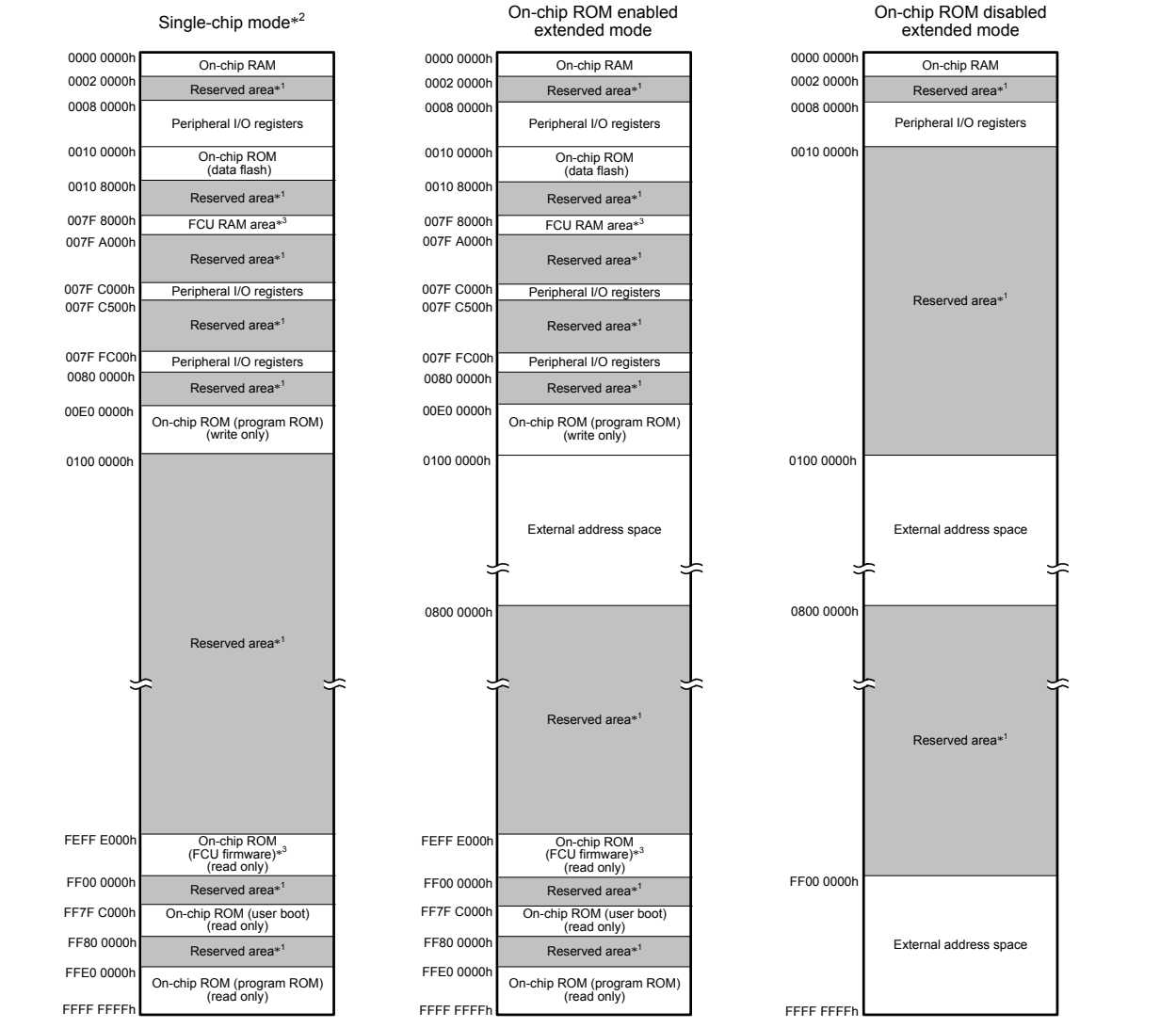
Note 2: The BC0# and BC1# signals are valid in both reading and writing.

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figures 3.1 to 3.4 show the memory maps in the respective operating modes of each product. Accessible areas will differ according to the operating mode and states of control bits.



Notes: 1. A reserved area should not be accessed.
2. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
3. For details on the FCU, see section 26, ROM (Flash Memory for Code Storage) and section 27, Data Flash (Flash Memory for Data Storage) in the User's manual: Hardware.

Figure 3.1 Memory Map of the R5F56108

4. I/O Registers

Table 4.1 List of I/O Registers (Address Order)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16	3 ICLK
0008 0002h	SYSTEM	Mode status register	MDSR	16	16	3 ICLK
0008 0006h	SYSTEM	System control register 0	SYSCR0	16	16	3 ICLK
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32	3 ICLK
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32	3 ICLK
0008 1300h	BSC	Bus error source clear register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus error monitor enable register	BEREN	8	8	2 ICLK
0008 1306h	BSC	Bus error interrupt enable register	BERIE	8	8	2 ICLK
0008 2000h	DMAC0	DMA current transfer source address register	DMCSA	32	32	4 to 5 ICLK
0008 2004h	DMAC0	DMA current transfer destination address register	DMCDA	32	32	4 to 5 ICLK
0008 2008h	DMAC0	DMA current transfer byte count register	DMCBC	32	32	4 to 5 ICLK
0008 200Ch	DMAC0	DMA mode register	DMMOD	32	32	4 to 5 ICLK
0008 2010h	DMAC1	DMA current transfer source address register	DMCSA	32	32	4 to 5 ICLK
0008 2014h	DMAC1	DMA current transfer destination address register	DMCDA	32	32	4 to 5 ICLK
0008 2018h	DMAC1	DMA current transfer byte count register	DMCBC	32	32	4 to 5 ICLK
0008 201Ch	DMAC1	DMA mode register	DMMOD	32	32	4 to 5 ICLK
0008 2020h	DMAC2	DMA current transfer source address register	DMCSA	32	32	4 to 5 ICLK
0008 2024h	DMAC2	DMA current transfer destination address register	DMCDA	32	32	4 to 5 ICLK
0008 2028h	DMAC2	DMA current transfer byte count register	DMCBC	32	32	4 to 5 ICLK
0008 202Ch	DMAC2	DMA mode register	DMMOD	32	32	4 to 5 ICLK
0008 2030h	DMAC3	DMA current transfer source address register	DMCSA	32	32	4 to 5 ICLK
0008 2034h	DMAC3	DMA current transfer destination address register	DMCDA	32	32	4 to 5 ICLK
0008 2038h	DMAC3	DMA current transfer byte count register	DMCBC	32	32	4 to 5 ICLK
0008 203Ch	DMAC3	DMA mode register	DMMOD	32	32	4 to 5 ICLK
0008 2200h	DMAC0	DMA reload transfer source address register	DMRSA	32	32	4 to 5 ICLK *8
0008 2204h	DMAC0	DMA reload transfer destination address register	DMRDA	32	32	4 to 5 ICLK *8
0008 2208h	DMAC0	DMA reload transfer byte count register	DMRBC	32	32	4 to 5 ICLK *8
0008 2210h	DMAC1	DMA reload transfer source address register	DMRSA	32	32	4 to 5 ICLK *8
0008 2214h	DMAC1	DMA reload transfer destination address register	DMRDA	32	32	4 to 5 ICLK *8
0008 2218h	DMAC1	DMA reload transfer byte count register	DMRBC	32	32	4 to 5 ICLK *8
0008 2220h	DMAC2	DMA reload transfer source address register	DMRSA	32	32	4 to 5 ICLK *8
0008 2224h	DMAC2	DMA reload transfer destination address register	DMRDA	32	32	4 to 5 ICLK *8
0008 2228h	DMAC2	DMA reload transfer byte count register	DMRBC	32	32	4 to 5 ICLK *8
0008 2230h	DMAC3	DMA reload transfer source address register	DMRSA	32	32	4 to 5 ICLK *8
0008 2234h	DMAC3	DMA reload transfer destination address register	DMRDA	32	32	4 to 5 ICLK *8
0008 2238h	DMAC3	DMA reload transfer byte count register	DMRBC	32	32	4 to 5 ICLK *8

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 2400h	DMAC0	DMA control register A	DMCRA	32	32	3 ICLK
0008 2404h	DMAC0	DMA control register B	DMCRB	8	8	3 ICLK
0008 2405h	DMAC0	DMA control register C	DMCRC	8	8	3 ICLK
0008 2406h	DMAC0	DMA control register D	DMCRD	8	8	3 ICLK
0008 2407h	DMAC0	DMA control register E	DMCRE	8	8	3 ICLK
0008 2408h	DMAC1	DMA control register A	DMCRA	32	32	3 ICLK
0008 240Ch	DMAC1	DMA control register B	DMCRB	8	8	3 ICLK
0008 240Dh	DMAC1	DMA control register C	DMCRC	8	8	3 ICLK
0008 240Eh	DMAC1	DMA control register D	DMCRD	8	8	3 ICLK
0008 240Fh	DMAC1	DMA control register E	DMCRE	8	8	3 ICLK
0008 2410h	DMAC2	DMA control register A	DMCRA	32	32	3 ICLK
0008 2414h	DMAC2	DMA control register B	DMCRB	8	8	3 ICLK
0008 2415h	DMAC2	DMA control register C	DMCRC	8	8	3 ICLK
0008 2416h	DMAC2	DMA control register D	DMCRD	8	8	3 ICLK
0008 2417h	DMAC2	DMA control register E	DMCRE	8	8	3 ICLK
0008 2418h	DMAC3	DMA control register A	DMCRA	32	32	3 ICLK
0008 241Ch	DMAC3	DMA control register B	DMCRB	8	8	3 ICLK
0008 241Dh	DMAC3	DMA control register C	DMCRC	8	8	3 ICLK
0008 241Eh	DMAC3	DMA control register D	DMCRD	8	8	3 ICLK
0008 241Fh	DMAC3	DMA control register E	DMCRE	8	8	3 ICLK
0008 2502h	DMAC common	DMA start control register	DMSCNT	8	8	3 ICLK
0008 250Bh	DMAC common	DMA interrupt control register	DMICNT	8	8	3 ICLK
0008 2517h	DMAC common	DMA transfer end detect register	DMEDET	8	8	3 ICLK
0008 251Bh	DMAC common	DMA arbitration status register	DMASTS	8	8	3 ICLK
0008 3002h	BSC	CS0 mode register	CS0MOD	16	16	1 to 2 BCLK *7
0008 3004h	BSC	CS0 wait control register 1	CS0WCNT1	32	32	1 to 2 BCLK *7
0008 3008h	BSC	CS0 wait control register 2	CS0WCNT2	32	32	1 to 2 BCLK *7
0008 3012h	BSC	CS1 mode register	CS1MOD	16	16	1 to 2 BCLK *7
0008 3014h	BSC	CS1 wait control register 1	CS1WCNT1	32	32	1 to 2 BCLK *7
0008 3018h	BSC	CS1 wait control register 2	CS1WCNT2	32	32	1 to 2 BCLK *7
0008 3022h	BSC	CS2 mode register	CS2MOD	16	16	1 to 2 BCLK *7
0008 3024h	BSC	CS2 wait control register 1	CS2WCNT1	32	32	1 to 2 BCLK *7
0008 3028h	BSC	CS2 wait control register 2	CS2WCNT2	32	32	1 to 2 BCLK *7
0008 3032h	BSC	CS3 mode register	CS3MOD	16	16	1 to 2 BCLK *7
0008 3034h	BSC	CS3 wait control register 1	CS3WCNT1	32	32	1 to 2 BCLK *7
0008 3038h	BSC	CS3 wait control register 2	CS3WCNT2	32	32	1 to 2 BCLK *7
0008 3042h	BSC	CS4 mode register	CS4MOD	16	16	1 to 2 BCLK *7
0008 3044h	BSC	CS4 wait control register 1	CS4WCNT1	32	32	1 to 2 BCLK *7
0008 3048h	BSC	CS4 wait control register 2	CS4WCNT2	32	32	1 to 2 BCLK *7
0008 3052h	BSC	CS5 mode register	CS5MOD	16	16	1 to 2 BCLK *7
0008 3054h	BSC	CS5 wait control register 1	CS5WCNT1	32	32	1 to 2 BCLK *7
0008 3058h	BSC	CS5 wait control register 2	CS5WCNT2	32	32	1 to 2 BCLK *7
0008 3062h	BSC	CS6 mode register	CS6MOD	16	16	1 to 2 BCLK *7
0008 3064h	BSC	CS6 wait control register 1	CS6WCNT1	32	32	1 to 2 BCLK *7
0008 3068h	BSC	CS6 wait control register 2	CS6WCNT2	32	32	1 to 2 BCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7170h	ICU	Interrupt request destination setting register 112	ISELR112	8	8	2 ICLK
0008 7175h	ICU	Interrupt request destination setting register 117	ISELR117	8	8	2 ICLK
0008 7176h	ICU	Interrupt request destination setting register 118	ISELR118	8	8	2 ICLK
0008 717Ah	ICU	Interrupt request destination setting register 122	ISELR122	8	8	2 ICLK
0008 717Bh	ICU	Interrupt request destination setting register 123	ISELR123	8	8	2 ICLK
0008 717Ch	ICU	Interrupt request destination setting register 124	ISELR124	8	8	2 ICLK
0008 717Dh	ICU	Interrupt request destination setting register 125	ISELR125	8	8	2 ICLK
0008 717Fh	ICU	Interrupt request destination setting register 127	ISELR127	8	8	2 ICLK
0008 7180h	ICU	Interrupt request destination setting register 128	ISELR128	8	8	2 ICLK
0008 7185h	ICU	Interrupt request destination setting register 133	ISELR133	8	8	2 ICLK
0008 7186h	ICU	Interrupt request destination setting register 134	ISELR134	8	8	2 ICLK
0008 718Ah	ICU	Interrupt request destination setting register 138	ISELR138	8	8	2 ICLK
0008 718Bh	ICU	Interrupt request destination setting register 139	ISELR139	8	8	2 ICLK
0008 718Ch	ICU	Interrupt request destination setting register 140	ISELR140	8	8	2 ICLK
0008 718Dh	ICU	Interrupt request destination setting register 141	ISELR141	8	8	2 ICLK
0008 7191h	ICU	Interrupt request destination setting register 145	ISELR145	8	8	2 ICLK
0008 7192h	ICU	Interrupt request destination setting register 146	ISELR146	8	8	2 ICLK
0008 7197h	ICU	Interrupt request destination setting register 151	ISELR151	8	8	2 ICLK
0008 7198h	ICU	Interrupt request destination setting register 152	ISELR152	8	8	2 ICLK
0008 719Ch	ICU	Interrupt request destination setting register 156	ISELR156	8	8	2 ICLK
0008 719Dh	ICU	Interrupt request destination setting register 157	ISELR157	8	8	2 ICLK
0008 719Eh	ICU	Interrupt request destination setting register 158	ISELR158	8	8	2 ICLK
0008 719Fh	ICU	Interrupt request destination setting register 159	ISELR159	8	8	2 ICLK
0008 71A1h	ICU	Interrupt request destination setting register 161	ISELR161	8	8	2 ICLK
0008 71A2h	ICU	Interrupt request destination setting register 162	ISELR162	8	8	2 ICLK
0008 71A7h	ICU	Interrupt request destination setting register 167	ISELR167	8	8	2 ICLK
0008 71A8h	ICU	Interrupt request destination setting register 168	ISELR168	8	8	2 ICLK
0008 71AEh	ICU	Interrupt request destination setting register 174	ISELR174	8	8	2 ICLK
0008 71AFh	ICU	Interrupt request destination setting register 175	ISELR175	8	8	2 ICLK
0008 71B1h	ICU	Interrupt request destination setting register 177	ISELR177	8	8	2 ICLK
0008 71B2h	ICU	Interrupt request destination setting register 178	ISELR178	8	8	2 ICLK
0008 71B4h	ICU	Interrupt request destination setting register 180	ISELR180	8	8	2 ICLK
0008 71B5h	ICU	Interrupt request destination setting register 181	ISELR181	8	8	2 ICLK
0008 71B7h	ICU	Interrupt request destination setting register 183	ISELR183	8	8	2 ICLK
0008 71B8h	ICU	Interrupt request destination setting register 184	ISELR184	8	8	2 ICLK
0008 71C6h	ICU	Interrupt request destination setting register 198	ISELR198	8	8	2 ICLK
0008 71C7h	ICU	Interrupt request destination setting register 199	ISELR199	8	8	2 ICLK
0008 71C8h	ICU	Interrupt request destination setting register 200	ISELR200	8	8	2 ICLK
0008 71C9h	ICU	Interrupt request destination setting register 201	ISELR201	8	8	2 ICLK
0008 71D7h	ICU	Interrupt request destination setting register 215	ISELR215	8	8	2 ICLK
0008 71D8h	ICU	Interrupt request destination setting register 216	ISELR216	8	8	2 ICLK
0008 71DBh	ICU	Interrupt request destination setting register 219	ISELR219	8	8	2 ICLK
0008 71DCh	ICU	Interrupt request destination setting register 220	ISELR220	8	8	2 ICLK
0008 71DFh	ICU	Interrupt request destination setting register 223	ISELR223	8	8	2 ICLK
0008 71E0h	ICU	Interrupt request destination setting register 224	ISELR224	8	8	2 ICLK

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input pull-up resistor current	Ports A to E			$-I_p$	10	—	300	µA	V_{CC} = 3.0 to 3.6 V, V_{in} = 0 V
Input capacitance	All input pins (except port 0, ports 14 to 17)			C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	Port 0, ports 14 to 17				—	—	30		
Supply current*3	In operation	Max.*4		I_{CC}*5	—	—	100	mA	ICLK = 100 MHz PCLK = 50 MHz BCLK = 25 MHz
		Normal*6			—	35	—		
		Increased by BGO operation*7			—	15	—		
	Sleep				—	18	52		
	All-module-clock-stop mode*8				—	14	28		
	Standby mode	Software standby mode			—	0.08	3.0		
		Deep software standby mode	RAM retained		—	15	200	µA	
			RAM power supply halted		—	0.9	26		
Analog power supply current	During A/D conversion (per unit)			AI_{CC}	—	0.8	1.2	mA	
	During D/A conversion (per unit)				—	0.3	1.0	µA	
	Idle (all units)				—	0.3	1.0		
Reference power supply current	During A/D conversion (per unit)				—	0.06	0.1	mA	
	During D/A conversion (per unit)				—	0.4	0.6		
	Idle (all units)				—	0.3	1.0	µA	
RAM standby voltage				V_{RAM}	2.5	—	—	V	
V_{CC} start voltage*9				$V_{CCSTART}$	—	—	0.8	V	
V_{CC} rising gradient*9				SV_{CC}	—	—	20	ms/V	

Notes:
1. This does not include the pins, which are multiplexed as ports 0, and 14 to 17 for 5 V tolerant.
2. This includes the multiplexed pins, but RIIC input pins for ports 14 to 17 are excluded.
3. Supply current values are with all output pins unloaded, all input pins for V_{IH} = V_{CC} and V_{IL}= 0 V, and all input pull-up resistors in the off state.
4. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
5. I_{CC} depends on f (ICLK) as follows. (ICLK : PCLK : BCLK = 8 : 4: 2)

   I_{CC} max. = 0.89 x f + 11 (max.)
   I_{CC} typ. = 0.30 x f + 5 (normal operation)
   I_{CC} max. = 0.41 x f + 11 (sleep mode)
6. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.
7. Incremented if data is written to or erased from the ROM or data flash for data storage during the program execution.
8. The values are for reference.
9. This can be applied when the RES# pin is held low at power-on.

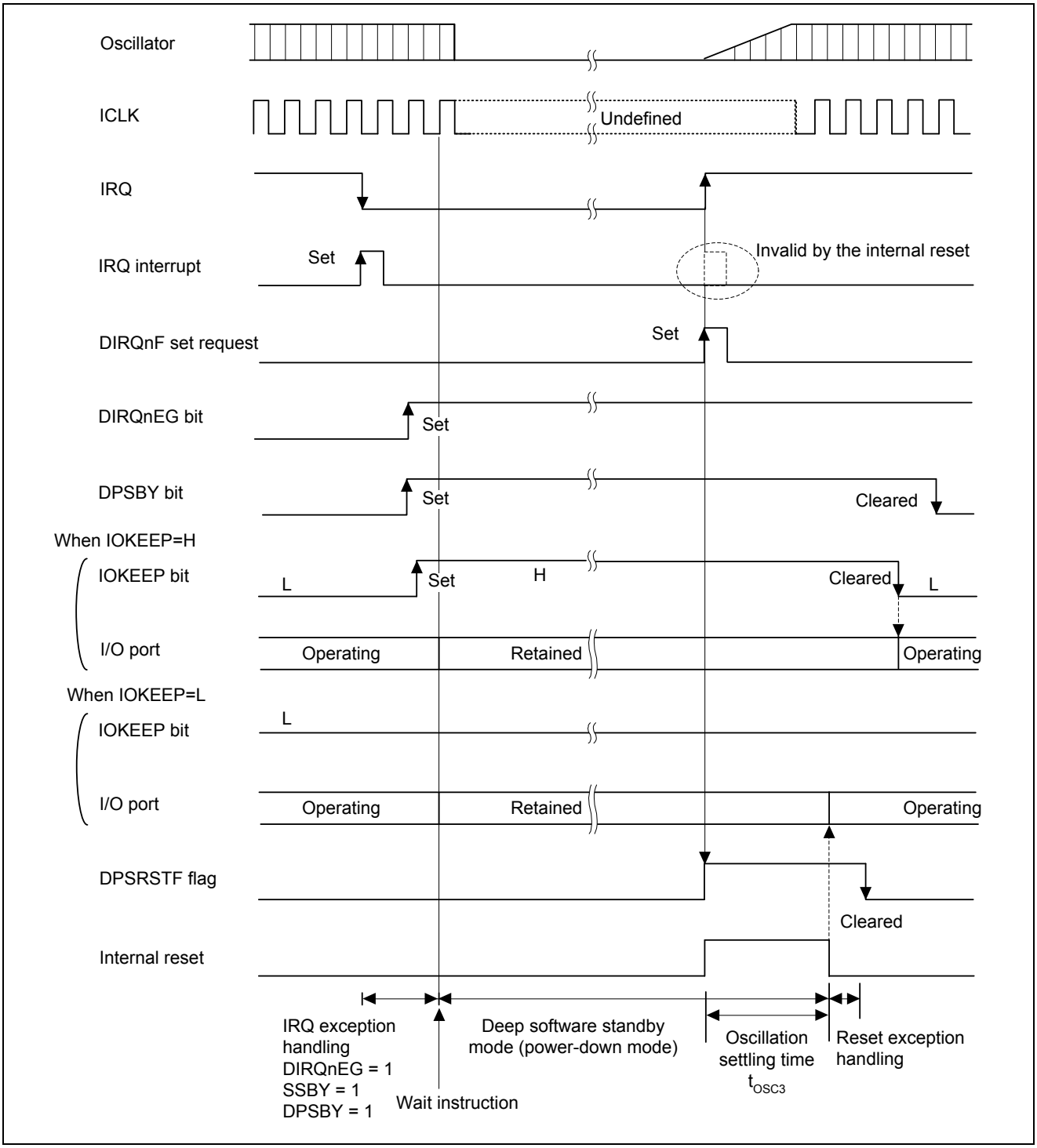


Figure 5.3 Oscillation Settling Timing after Deep Software Standby Mode

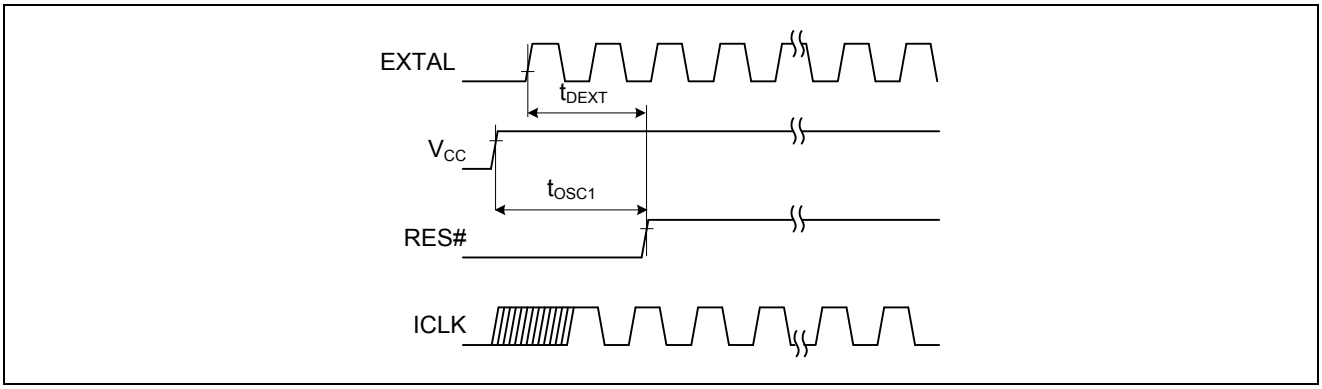


Figure 5.4 Oscillation Settling Timing

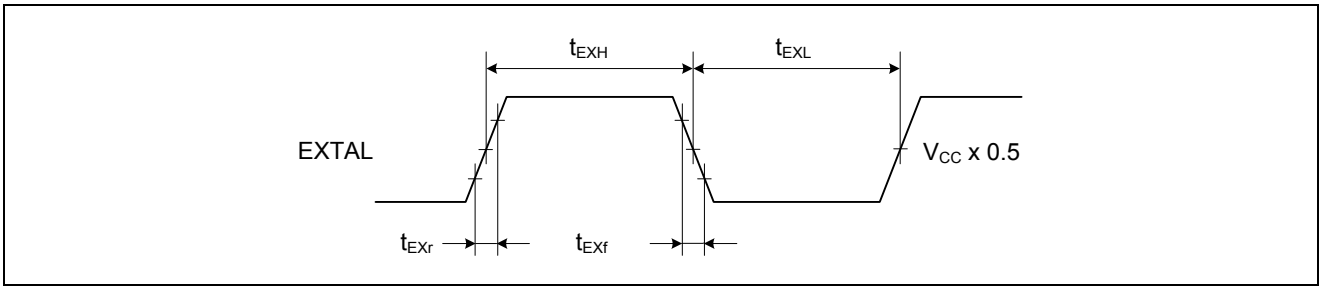


Figure 5.5 External Input Clock Timing

5.3.3 Bus Timing

Table 5.7 Bus Timing

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V, BCLK = 8 to 25 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)
Output load conditions: V_{OH} = V_{CC} x 0.5, V_{OL} = V_{CC} x 0.5, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	30	ns	Figures 5.9 to 5.12
Byte control delay time	t_{BCD}	—	30	ns	
CS# delay time	t_{CSD}	—	30	ns	
RD# delay time	t_{RSD}	—	20	ns	
RD# setup time	t_{RSS}	0.5 × (1/BCLK) - 20	—	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	20	ns	
WR# setup time	t_{WRS}	0.5 × (1/BCLK) - 20	—	ns	
Write data delay time	t_{WDD}	—	35	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	15	—	ns	Figure 5.13
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.8 Timing of On-Chip Peripheral Modules (2)

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V, PCLK = 8 to 50 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item		Symbol	Min. *1*2	Max.	Unit	Test Conditions
RIIC (Standard-mode) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	8(10) x (1/PCLK) + 1300	—	ns	Figure 5.25
	SCL input high pulse width	t_{SCLH}	3(5) x (1/PCLK) + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	5x (1/PCLK) + 1000	—	ns	
	SCL, SDA input rising time	t_{Sr}	—	1000	ns	
	SCL, SDA input falling time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 x (1/PCLK)	ns	
	SDA input bus free time	t_{BUF}	5x (1/PCLK) + 1000	—	ns	
	Start condition input hold time	t_{STAH}	3(5) x (1/PCLK) + 300	—	ns	
	Re-start condition input setup time	t_{STAS}	5x (1/PCLK) + 1000	—	ns	
	Stop condition input setup time	t_{STOS}	3(5) x (1/PCLK) + 300	—	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	8(10) x (1/PCLK) + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(5) x (1/PCLK) + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	5 x (1/PCLK) + 300	—	ns	
	SCL, SDA input rising time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input falling time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 x (1/PCLK)	ns	
	SDA input bus free time	t_{BUF}	5 x (1/PCLK) + 300	—	ns	
	Start condition input hold time	t_{STAH}	3(5) x (1/PCLK) + 300	—	ns	
	Re-start condition input setup time	t_{STAS}	5 x (1/PCLK) + 300	—	ns	
	Stop condition input setup time	t_{STOS}	3(5) x (1/PCLK) + 300	—	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

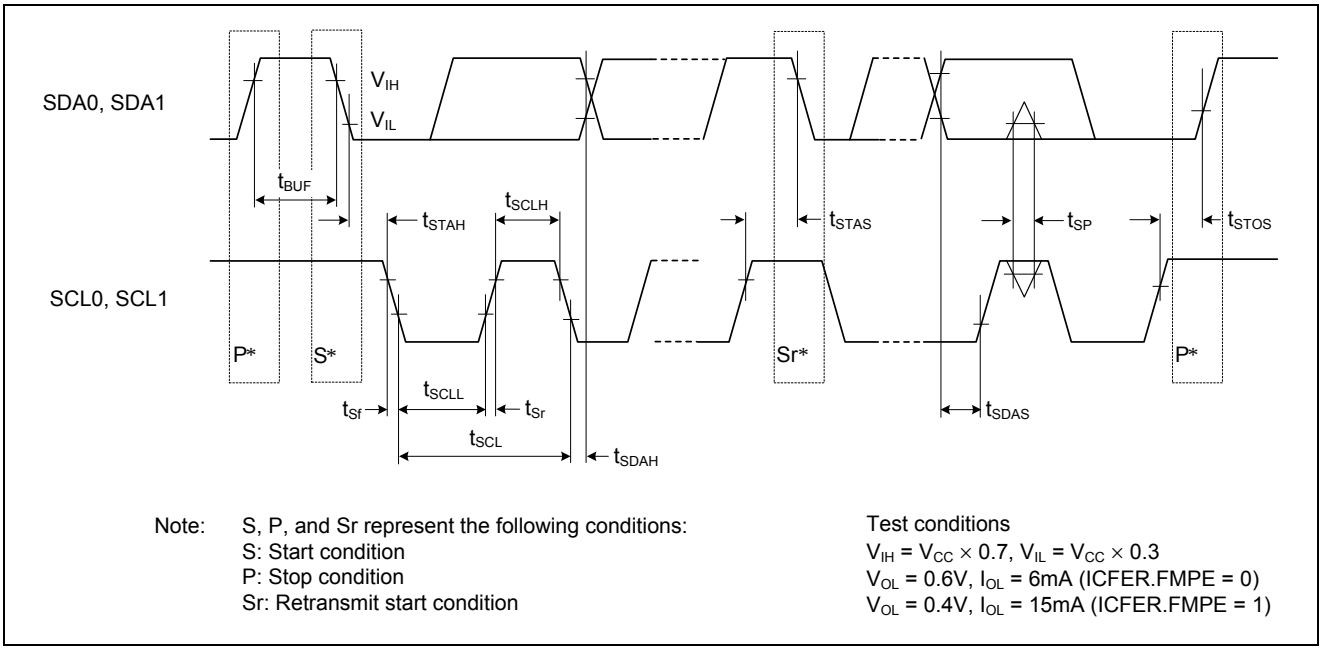


Figure 5.25 I²C Bus Interface Input/Output Timing

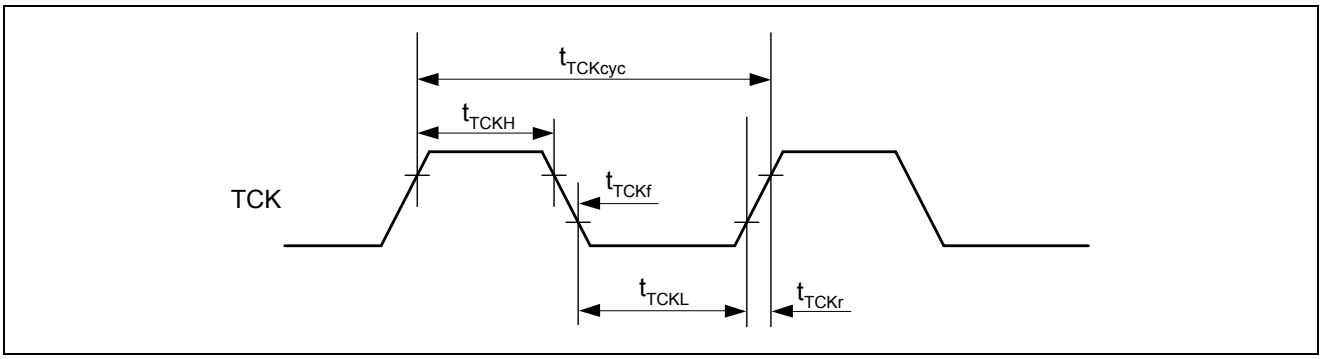


Figure 5.26 Boundary Scan TCK Timing

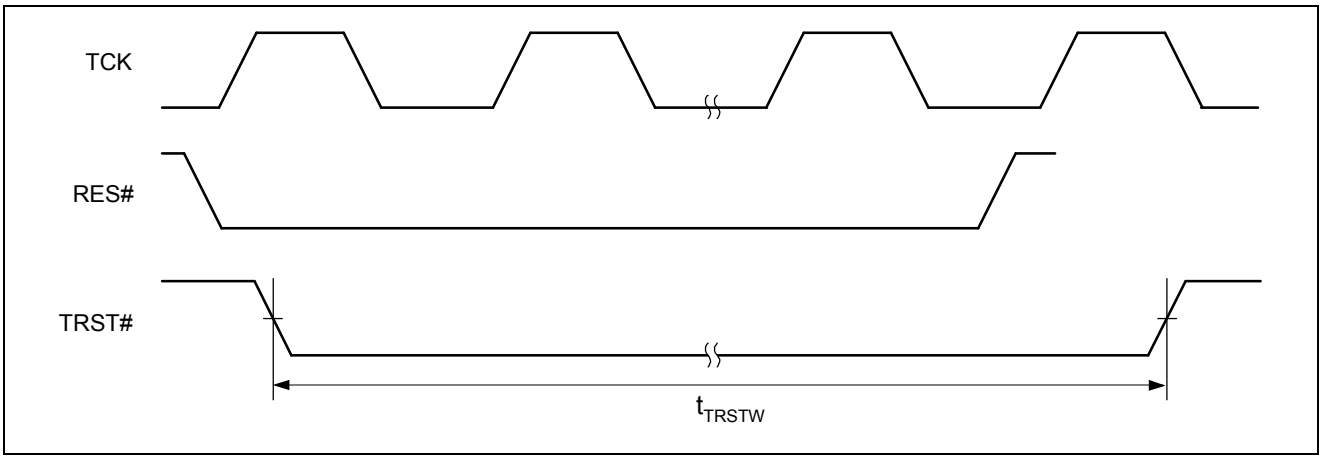


Figure 5.27 Boundary Scan TRST# Timing

5.7 Data Flash (Flash Memory for Data Storage) Characteristics

Table 5.12 Data Flash (Flash Memory for Data Storage) Characteristics

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V
Operating temperature range during programming/erasing:
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time	8 bytes	t_{DP8}	—	0.4	2	ms	PCLK = 50-MHz operation
	128 bytes	t_{DP128}	—	1	5	ms	
Erasure time	8 Kbytes	t_{DE8K}	—	300	900	ms	PCLK = 50-MHz operation
Blank check time	8 bytes	t_{DBC8}	—	—	30	µs	PCLK = 50-MHz operation
	8 Kbytes	t_{DBC8K}	—	—	2.5	ms	
Rewrite/erase cycle*1		N_{DPEC}	30000*2	—	—	Times	
Suspend delay time during writing		t_{DSPD}	—	—	120	µs	Figure 5.29 PCLK = 50-MHz operation
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t_{DSEED}	—	—	1.7	ms	
Data hold time*3		T_{DDRP}	10	—	—	Year	

Notes: 1. Definition of rewrite/erase cycle:
The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 30000), erasing can be performed n times for each block. For instance, when 128-byte writing is performed 64 times for different addresses in 8-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (over writing is prohibited).
2. This indicates the minimum number that guarantees the characteristics after rewriting. (The guaranteed value is in the range from one to the minimum number.)
3. This indicates the characteristic when rewrite is performed within the specification range including the minimum number.

REVISION HISTORY — RX610 Group Datasheet

		Description	
Rev.	**Data**	**Page**	**Summary**
0.50	Mar. 24, 2009	–	First edition issued
1.00	Apr. 22, 2011		1. Overview
		6	Figure 1.2 Block Diagram: Ports F to H added
		7	Figure 1.3 Pin Assignment of the 176-pin LFBGA, added
		10 to 15	Table 1.3 List of Pins and Pin Functions (176-Pin LFBGA), added
			Table 1.5 Pin Functions:
		21, 25	Description on the BSCANP, PF0 to PF6, PG0 to PG7, and PH0 to PH7 pins added
			4. I/O Registers
		34 to 54	Table 4.1 List of I/O Registers (Address Order), changed
			5. Electrical Characteristics
		58	Table 5.3 Permissible Output Currents, changed
		59	Table 5.5 Clock Timing: Oscillation settling time after leaving deep software standby mode (crystal), $t_{OSC3,}$ added
		60	Figure 5.2 Oscillation Settling Timing after Software Standby Mode, changed
		61	Figure 5.3 Oscillation Settling Timing after Deep Software Standby Mode, added
		71	Table 5.8 Timing of On-Chip Peripheral Modules (3), changed
		75	Figure 5.26 Boundary Scan TCK Timing, added
		75	Figure 5.27 Boundary Scan TRST# Timing, added
		76	Figure 5.28 Boundary Scan Input/Output Timing, added
1.20	Feb.20, 2013		1. Overview
		5	Table 1.2 List of Products, product lineup added
		23, 26	Table 1.5 Pin Functions, description on bus control changed, note added
			5. I/O register
		35 to 55	Table 5.1 List of I/O Registers (Address Order), changed