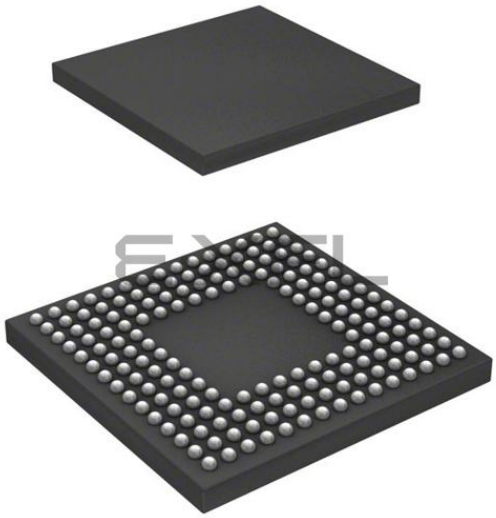
Renesas Electronics America Inc - R5F56104WDBG#U0 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	140
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 2x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56104wdbg-u0

1.2 List of Products

Table 1.2 is the list of products, and figure 1.1 shows how to read the product part no.

Table 1.2 List of Products

Part No.	Package	ROM Capacity	RAM Capacity	Data Flash	Operating Frequency (Max.)
R5F56108VNFP	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56108VDFP	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56108WNBG	PLBG0176GA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56108WDBG	PLBG0176GA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56107VNFP	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56107VDFP	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56107WNBG	PLBG0176GA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56107WDBG	PLBG0176GA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56106VNFP	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz
R5F56106VDFP	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz
R5F56106WNBG	PLBG0176GA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz
R5F56106WDBG	PLBG0176GA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz
R5F56104VNFP	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56104VDFP	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56104WNBG	PLBG0176GA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56104WDBG	PLBG0176GA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
M6		P37			PO15/ TIOCA2/ TIOCB2/ TCLKD-A			
M7		P57		WAIT#				TRDATA3
M8		P83						
M9		P81						TRSYNC
M10		P51		WR1#/BC1#				
M11		PH4						
M12		PC7		A23/ CS4#-D/ CS7#-D		TxD5		
M13	VSS							
M14		PC0		A16				
M15		PB6		A14	PO30/ TIOCA11			
N1		P25			PO5/ TIOCA4/ TMCI1	RxD1		
N2		P24			PO4/ TIOCA4/ TIOCB4/ TMRI1			
N3		P20			PO0/ TIOCA3/ TIOCB3/ TMRI0	TxD0		
N4		P16	IRQ6-B		TCLKC-B	RxD3/SDA0		
N5		P12	IRQ2-B			RxD2		
N6		P36			PO14/ TIOCA2			
N7		P56						TRDATA2
N8	VSS							
N9		P80						
N10		P50		WR0#/WR#				
N11	VSS							
N12		P76	IRQ14-A					
N13		PH2						
N14		PC2		A18				
N15		PC1		A17				
P1		P23			PO3/ TIOCC3/ TIOCD3			

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
108		PE1		D9				
109		PE0		D8				
110		PD7		D7				
111		PD6		D6				
112		PD5		D5				
113		PD4		D4				
114		P64		CS4#-B				
115		P63		CS3#-A/ CS7#-A				
116		P62		CS2#-A/ CS6#-A				
117		P61		CS1#/ CS2#-B/ CS5#-A/ CS6#-B/ CS7#-B				
118		P60		CS0#/ CS4#-A/ CS5#-B				
119		PD3		D3				
120		PD2		D2				
121		PD1		D1				
122		PD0		D0				
123		P97					AN15	
124		P96					AN14	
125		P95					AN13	
126		P94					AN12	
127		P93					AN11	
128		P92					AN10	
129		P91					AN9	
130	VSS							
131		P90					AN8	
132	VCC							
133		P47	IRQ15-B				AN7	
134		P46	IRQ14-B				AN6	
135		P45	IRQ13-B				AN5	
136		P44	IRQ12-B				AN4	
137		P43	IRQ11-B				AN3	
138		P42	IRQ10-B				AN2	
139		P41	IRQ9-B				AN1	
140	VREFL							
141		P40	IRQ8-B				AN0	
142	VREFH							
143	AVCC							
144		P05	IRQ13-A		TMO3	RxD4		TCK

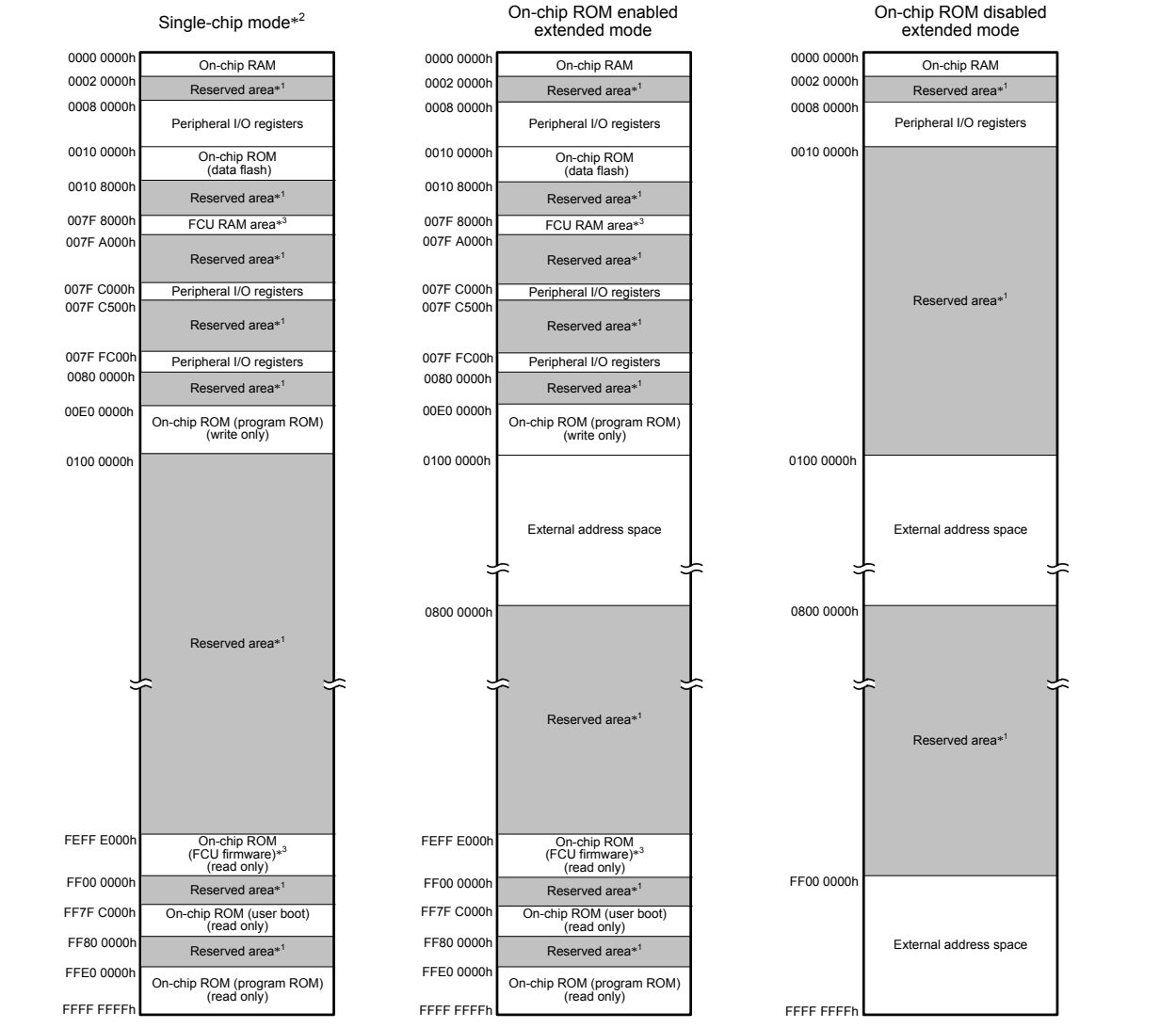
Classifications	Pin Name	I/O	Description
Interrupt	NMI	Input	Non-maskable interrupt request signal
	IRQ0-A/IRQ0-B IRQ1-A/IRQ1-B IRQ2-A/IRQ2-B IRQ3-A/IRQ3-B IRQ4-A/IRQ4-B IRQ5-A/IRQ5-B IRQ6-A/IRQ6-B IRQ7-A/IRQ7-B IRQ8-A/IRQ8-B IRQ9-A/IRQ9-B IRQ10-A/IRQ10-B IRQ11-A/IRQ11-B IRQ12-A/IRQ12-B IRQ13-A/IRQ13-B IRQ14-A/IRQ14-B IRQ15-A/IRQ15-B	Input	Maskable request signals
16-bit timer pulse unit	TIOCA0, TIOCB0 TIOCC0, TIOCD0	I/O	Signals for TGRA0 to TGRD0. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA1, TIOCB1	I/O	Signals for TGRA1 and TGRB1. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA2, TIOCB2	I/O	Signals for TGRA2 and TGRB2. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA3, TIOCB3 TIOCC3, TIOCD3	I/O	Signals for TGRA3 to TGRD3. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA4, TIOCB4	I/O	Signals for TGRA4 and TGRB4. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA5, TIOCB5	I/O	Signals for TGRA5 and TGRB5. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA6, TIOCB6 TIOCC6, TIOCD6	I/O	Signals for TGRA6 to TGRD6. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA7, TIOCB7	I/O	Signals for TGRA7 and TGRB7. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA8, TIOCB8	I/O	Signals for TGRA8 and TGRB8. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA9, TIOCB9 TIOCC9, TIOCD9	I/O	Signals for TGRA9 to TGRD9. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA10, TIOCB10	I/O	Signals for TGRA10 and TGRB10. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA11, TIOCB11	I/O	Signals for TGRA11 and TGRB11. These pins are used as input capture inputs, output compare outputs, or PWM outputs.

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figures 3.1 to 3.4 show the memory maps in the respective operating modes of each product. Accessible areas will differ according to the operating mode and states of control bits.



Notes: 1. A reserved area should not be accessed.
2. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
3. For details on the FCU, see section 26, ROM (Flash Memory for Code Storage) and section 27, Data Flash (Flash Memory for Data Storage) in the User's manual: Hardware.

Figure 3.1 Memory Map of the R5F56108

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 70EAh	ICU	Interrupt request register 234	IR234	8	8	2 ICLK
0008 70EBh	ICU	Interrupt request register 235	IR235	8	8	2 ICLK
0008 70ECh	ICU	Interrupt request register 236	IR236	8	8	2 ICLK
0008 70EDh	ICU	Interrupt request register 237	IR237	8	8	2 ICLK
0008 70EEh	ICU	Interrupt request register 238	IR238	8	8	2 ICLK
0008 70EFh	ICU	Interrupt request register 239	IR239	8	8	2 ICLK
0008 70F0h	ICU	Interrupt request register 240	IR240	8	8	2 ICLK
0008 70F1h	ICU	Interrupt request register 241	IR241	8	8	2 ICLK
0008 70F6h	ICU	Interrupt request register 246	IR246	8	8	2 ICLK
0008 70F7h	ICU	Interrupt request register 247	IR247	8	8	2 ICLK
0008 70F8h	ICU	Interrupt request register 248	IR248	8	8	2 ICLK
0008 70F9h	ICU	Interrupt request register 249	IR249	8	8	2 ICLK
0008 70FAh	ICU	Interrupt request register 250	IR250	8	8	2 ICLK
0008 70FBh	ICU	Interrupt request register 251	IR251	8	8	2 ICLK
0008 70FCh	ICU	Interrupt request register 252	IR252	8	8	2 ICLK
0008 70FDh	ICU	Interrupt request register 253	IR253	8	8	2 ICLK
0008 711Ch	ICU	Interrupt request destination setting register 028	ISELR028	8	8	2 ICLK
0008 711Dh	ICU	Interrupt request destination setting register 029	ISELR029	8	8	2 ICLK
0008 711Eh	ICU	Interrupt request destination setting register 030	ISELR030	8	8	2 ICLK
0008 711Fh	ICU	Interrupt request destination setting register 031	ISELR031	8	8	2 ICLK
0008 7140h	ICU	Interrupt request destination setting register 064	ISELR064	8	8	2 ICLK
0008 7141h	ICU	Interrupt request destination setting register 065	ISELR065	8	8	2 ICLK
0008 7142h	ICU	Interrupt request destination setting register 066	ISELR066	8	8	2 ICLK
0008 7143h	ICU	Interrupt request destination setting register 067	ISELR067	8	8	2 ICLK
0008 7144h	ICU	Interrupt request destination setting register 068	ISELR068	8	8	2 ICLK
0008 7145h	ICU	Interrupt request destination setting register 069	ISELR069	8	8	2 ICLK
0008 7146h	ICU	Interrupt request destination setting register 070	ISELR070	8	8	2 ICLK
0008 7147h	ICU	Interrupt request destination setting register 071	ISELR071	8	8	2 ICLK
0008 7148h	ICU	Interrupt request destination setting register 072	ISELR072	8	8	2 ICLK
0008 7149h	ICU	Interrupt request destination setting register 073	ISELR073	8	8	2 ICLK
0008 714Ah	ICU	Interrupt request destination setting register 074	ISELR074	8	8	2 ICLK
0008 714Bh	ICU	Interrupt request destination setting register 075	ISELR075	8	8	2 ICLK
0008 714Ch	ICU	Interrupt request destination setting register 076	ISELR076	8	8	2 ICLK
0008 714Dh	ICU	Interrupt request destination setting register 077	ISELR077	8	8	2 ICLK
0008 714Eh	ICU	Interrupt request destination setting register 078	ISELR078	8	8	2 ICLK
0008 714Fh	ICU	Interrupt request destination setting register 079	ISELR079	8	8	2 ICLK
0008 7162h	ICU	Interrupt request destination setting register 098	ISELR098	8	8	2 ICLK
0008 7163h	ICU	Interrupt request destination setting register 099	ISELR099	8	8	2 ICLK
0008 7164h	ICU	Interrupt request destination setting register 100	ISELR100	8	8	2 ICLK
0008 7165h	ICU	Interrupt request destination setting register 101	ISELR101	8	8	2 ICLK
0008 7168h	ICU	Interrupt request destination setting register 104	ISELR104	8	8	2 ICLK
0008 7169h	ICU	Interrupt request destination setting register 105	ISELR105	8	8	2 ICLK
0008 716Ah	ICU	Interrupt request destination setting register 106	ISELR106	8	8	2 ICLK
0008 716Bh	ICU	Interrupt request destination setting register 107	ISELR107	8	8	2 ICLK
0008 716Fh	ICU	Interrupt request destination setting register 111	ISELR111	8	8	2 ICLK

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8116h	TPU0	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8118h	TPU0	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 811Ah	TPU0	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 811Ch	TPU0	Timer general register C	TGRC	16	16	2 to 3 PCLK *7
0008 811Eh	TPU0	Timer general register D	TGRD	16	16	2 to 3 PCLK *7
0008 8120h	TPU1	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8121h	TPU1	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8122h	TPU1	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8124h	TPU1	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8125h	TPU1	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8126h	TPU1	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8128h	TPU1	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 812Ah	TPU1	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 8130h	TPU2	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8131h	TPU2	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8132h	TPU2	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8134h	TPU2	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8135h	TPU2	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8136h	TPU2	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8138h	TPU2	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 813Ah	TPU2	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 8140h	TPU3	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8141h	TPU3	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8142h	TPU3	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK *7
0008 8143h	TPU3	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK *7
0008 8144h	TPU3	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8145h	TPU3	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8146h	TPU3	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8148h	TPU3	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 814Ah	TPU3	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 814Ch	TPU3	Timer general register C	TGRC	16	16	2 to 3 PCLK *7
0008 814Eh	TPU3	Timer general register D	TGRD	16	16	2 to 3 PCLK *7
0008 8150h	TPU4	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8151h	TPU4	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8152h	TPU4	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8154h	TPU4	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8155h	TPU4	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8156h	TPU4	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8158h	TPU4	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 815Ah	TPU4	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 8160h	TPU5	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8161h	TPU5	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8162h	TPU5	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8164h	TPU5	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8165h	TPU5	Timer status register	TSR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8166h	TPU5	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8168h	TPU5	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 816Ah	TPU5	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 8170h	TPU (unit 1)	Timer start register	TSTRB	8	8	2 to 3 PCLK *7
0008 8171h	TPU (unit 1)	Timer synchronous register	TSYRB	8	8	2 to 3 PCLK *7
0008 8180h	TPU6	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8181h	TPU6	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8182h	TPU6	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK *7
0008 8183h	TPU6	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK *7
0008 8184h	TPU6	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8185h	TPU6	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8186h	TPU6	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8188h	TPU6	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 818Ah	TPU6	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 818Ch	TPU6	Timer general register C	TGRC	16	16	2 to 3 PCLK *7
0008 818Eh	TPU6	Timer general register D	TGRD	16	16	2 to 3 PCLK *7
0008 8190h	TPU7	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8191h	TPU7	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8192h	TPU7	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8194h	TPU7	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8195h	TPU7	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8196h	TPU7	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8198h	TPU7	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 819Ah	TPU7	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 81A0h	TPU8	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 81A1h	TPU8	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 81A2h	TPU8	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 81A4h	TPU8	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 81A5h	TPU8	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 81A6h	TPU8	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 81A8h	TPU8	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 81AAh	TPU8	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 81B0h	TPU9	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 81B1h	TPU9	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 81B2h	TPU9	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK *7
0008 81B3h	TPU9	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK *7
0008 81B4h	TPU9	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 81B5h	TPU9	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 81B6h	TPU9	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 81B8h	TPU9	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 81BAh	TPU9	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 81BCh	TPU9	Timer general register C	TGRC	16	16	2 to 3 PCLK *7
0008 81BEh	TPU9	Timer general register D	TGRD	16	16	2 to 3 PCLK *7
0008 81C0h	TPU10	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 81C1h	TPU10	Timer mode register	TMDR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 81C2h	TPU10	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 81C4h	TPU10	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 81C5h	TPU10	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 81C6h	TPU10	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 81C8h	TPU10	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 81CAh	TPU10	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 81D0h	TPU11	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 81D1h	TPU11	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 81D2h	TPU11	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 81D4h	TPU11	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 81D5h	TPU11	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 81D6h	TPU11	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 81D8h	TPU11	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 81DAh	TPU11	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 81E6h	PPG0	PPG output control register	PCR	8	8	2 to 3 PCLK *7
0008 81E7h	PPG0	PPG output mode register	PMR	8	8	2 to 3 PCLK *7
0008 81E8h	PPG0	Next data enable register H	NDERH	8	8	2 to 3 PCLK *7
0008 81E9h	PPG0	Next data enable register L	NDERL	8	8	2 to 3 PCLK *7
0008 81EAh	PPG0	Output data register H	PODRH	8	8	2 to 3 PCLK *7
0008 81EBh	PPG0	Output data register L	PODRL	8	8	2 to 3 PCLK *7
0008 81ECh*1	PPG0	Next data register H	NDRH	8	8	2 to 3 PCLK *7
0008 81EDh*2	PPG0	Next data register L	NDRL	8	8	2 to 3 PCLK *7
0008 81EEh*1	PPG0	Next data register H	NDRH	8	8	2 to 3 PCLK *7
0008 81EFh*2	PPG0	Next data register L	NDRL	8	8	2 to 3 PCLK *7
0008 81F0h	PPG1	PPG trigger select register	PTRSLR	8	8	2 to 3 PCLK *7
0008 81F6h	PPG1	PPG output control register	PCR	8	8	2 to 3 PCLK *7
0008 81F7h	PPG1	PPG output mode register	PMR	8	8	2 to 3 PCLK *7
0008 81F8h	PPG1	Next data enable register H	NDERH	8	8	2 to 3 PCLK *7
0008 81F9h	PPG1	Next data enable register L	NDERL	8	8	2 to 3 PCLK *7
0008 81FAh	PPG1	Output data register H	PODRH	8	8	2 to 3 PCLK *7
0008 81FBh	PPG1	Output data register L	PODRL	8	8	2 to 3 PCLK *7
0008 81FCh*3	PPG1	Next data register H	NDRH	8	8	2 to 3 PCLK *7
0008 81FDh*4	PPG1	Next data register L	NDRL	8	8	2 to 3 PCLK *7
0008 81FEh*3	PPG1	Next data register H	NDRH	8	8	2 to 3 PCLK *7
0008 81FFh*4	PPG1	Next data register L	NDRL	8	8	2 to 3 PCLK *7
0008 8200h	TMR0	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8201h	TMR1	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8202h	TMR0	Timer control/status register	TCSR	8	8	2 to 3 PCLK *7
0008 8203h	TMR1	Timer control/status register	TCSR	8	8	2 to 3 PCLK *7
0008 8204h	TMR0	Time constant register A	TCORA	8	8 or 16	2 to 3 PCLK *7
0008 8205h	TMR1	Time constant register A	TCORA	8	8 or 16*5	2 to 3 PCLK *7
0008 8206h	TMR0	Time constant register B	TCORB	8	8 or 16	2 to 3 PCLK *7
0008 8207h	TMR1	Time constant register B	TCORB	8	8 or 16*5	2 to 3 PCLK *7
0008 8208h	TMR0	Timer counter	TCNT	8	8 or 16	2 to 3 PCLK *7
0008 8209h	TMR1	Timer counter	TCNT	8	8 or 16*5	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 830Fh	RIIC0	Slave address register U2	SARU2	8	8	2 to 3 PCLK *7
0008 8310h	RIIC0	I²C bus bit rate low-level register	ICBRL	8	8	2 to 3 PCLK *7
0008 8311h	RIIC0	I²C bus bit rate high-level register	ICBRH	8	8	2 to 3 PCLK *7
0008 8312h	RIIC0	I²C bus transmit data register	ICDRT	8	8	2 to 3 PCLK *7
0008 8313h	RIIC0	I²C bus receive data register	ICDRR	8	8	2 to 3 PCLK *7
0008 8320h	RIIC1	I²C bus control register 1	ICCR1	8	8	2 to 3 PCLK *7
0008 8321h	RIIC1	I²C bus control register 2	ICCR2	8	8	2 to 3 PCLK *7
0008 8322h	RIIC1	I²C bus mode register 1	ICMR1	8	8	2 to 3 PCLK *7
0008 8323h	RIIC1	I²C bus mode register 2	ICMR2	8	8	2 to 3 PCLK *7
0008 8324h	RIIC1	I²C bus mode register 3	ICMR3	8	8	2 to 3 PCLK *7
0008 8325h	RIIC1	I²C bus function enable register	ICFER	8	8	2 to 3 PCLK *7
0008 8326h	RIIC1	I²C bus status enable register	ICSER	8	8	2 to 3 PCLK *7
0008 8327h	RIIC1	I²C bus interrupt enable register	ICIER	8	8	2 to 3 PCLK *7
0008 8328h	RIIC1	I²C bus status register 1	ICSR1	8	8	2 to 3 PCLK *7
0008 8329h	RIIC1	I²C bus status register 2	ICSR2	8	8	2 to 3 PCLK *7
0008 832Ah	RIIC1	Slave address register L0	SARL0	8	8	2 to 3 PCLK *7
0008 832Ah	RIIC1	Internal control for timeout L	TMOCNTL	16	16	2 to 3 PCLK *7
0008 832Bh	RIIC1	Slave address register U0	SARU0	8	8	2 to 3 PCLK *7
0008 832Bh	RIIC1	Internal control for timeout U	TMOCNTU	16	16	2 to 3 PCLK *7
0008 832Ch	RIIC1	Slave address register L1	SARL1	8	8	2 to 3 PCLK *7
0008 832Dh	RIIC1	Slave address register U1	SARU1	8	8	2 to 3 PCLK *7
0008 832Eh	RIIC1	Slave address register L2	SARL2	8	8	2 to 3 PCLK *7
0008 832Fh	RIIC1	Slave address register U2	SARU2	8	8	2 to 3 PCLK *7
0008 8330h	RIIC1	I²C bus bit rate low-level register	ICBRL	8	8	2 to 3 PCLK *7
0008 8331h	RIIC1	I²C bus bit rate high-level register	ICBRH	8	8	2 to 3 PCLK *7
0008 8332h	RIIC1	I²C bus transmit data register	ICDRT	8	8	2 to 3 PCLK *7
0008 8333h	RIIC1	I²C bus receive data register	ICDRR	8	8	2 to 3 PCLK *7
0008 C000h	P0	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C001h	P1	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C002h	P2	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C003h	P3	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C004h	P4	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C005h	P5	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C006h	P6	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C007h	P7	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C008h	P8	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C009h	P9	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Ah	PA	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Bh	PB	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Ch	PC	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Dh	PD	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Eh	PE	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Fh	PF	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C010h	PG	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C011h	PH	Data direction register	DDR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C020h	P0	Data register	DR	8	8	2 to 3 PCLK *7
0008 C021h	P1	Data register	DR	8	8	2 to 3 PCLK *7
0008 C022h	P2	Data register	DR	8	8	2 to 3 PCLK *7
0008 C023h	P3	Data register	DR	8	8	2 to 3 PCLK *7
0008 C024h	P4	Data register	DR	8	8	2 to 3 PCLK *7
0008 C025h	P5	Data register	DR	8	8	2 to 3 PCLK *7
0008 C026h	P6	Data register	DR	8	8	2 to 3 PCLK *7
0008 C027h	P7	Data register	DR	8	8	2 to 3 PCLK *7
0008 C028h	P8	Data register	DR	8	8	2 to 3 PCLK *7
0008 C029h	P9	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Ah	PA	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Bh	PB	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Ch	PC	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Dh	PD	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Eh	PE	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Fh	PF	Data register	DR	8	8	2 to 3 PCLK *7
0008 C030h	PG	Data register	DR	8	8	2 to 3 PCLK *7
0008 C031h	PH	Data register	DR	8	8	2 to 3 PCLK *7
0008 C040h	P0	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C041h	P1	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C042h	P2	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C043h	P3	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C044h	P4	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C045h	P5	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C046h	P6	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C047h	P7	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C048h	P8	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C049h	P9	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Ah	PA	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Bh	PB	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Ch	PC	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Dh	PD	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Eh	PE	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Fh	PF	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C050h	PG	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C051h	PH	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C060h	P0	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C061h	P1	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C062h	P2	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C063h	P3	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C064h	P4	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C065h	P5	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C066h	P6	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C067h	P7	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C068h	P8	Input buffer control register	ICR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C069h	P9	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C06Ah	PA	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C06Bh	PB	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C06Ch	PC	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C06Dh	PD	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C06Eh	PE	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C06Fh	PF	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C070h	PG	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C071h	PH	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C082h	P2	Open drain control register	ODR	8	8	2 to 3 PCLK *7
0008 C08Ch	PC	Open drain control register	ODR	8	8	2 to 3 PCLK *7
0008 C0CAh	PA	Pull-Up resistor control register	PCR	8	8	2 to 3 PCLK *7
0008 C0CBh	PB	Pull-Up resistor control register	PCR	8	8	2 to 3 PCLK *7
0008 C0CCh	PC	Pull-Up resistor control register	PCR	8	8	2 to 3 PCLK *7
0008 C0CDh	PD	Pull-Up resistor control register	PCR	8	8	2 to 3 PCLK *7
0008 C0CEh	PE	Pull-Up resistor control register	PCR	8	8	2 to 3 PCLK *7
0008 C100h	I/O PORT	Port function control register 0	PFCR0	8	8	2 to 3 PCLK *7
0008 C101h	I/O PORT	Port function control register 1	PFCR1	8	8	2 to 3 PCLK *7
0008 C102h	I/O PORT	Port function control register 2	PFCR2	8	8	2 to 3 PCLK *7
0008 C103h	I/O PORT	Port function control register 3	PFCR3	8	8	2 to 3 PCLK *7
0008 C104h	I/O PORT	Port function control register 4	PFCR4	8	8	2 to 3 PCLK *7
0008 C105h	I/O PORT	Port function control register 5	PFCR5	8	8	2 to 3 PCLK *7
0008 C106h	I/O PORT	Port function control register 6	PFCR6	8	8	2 to 3 PCLK *7
0008 C107h	I/O PORT	Port function control register 7	PFCR7	8	8	2 to 3 PCLK *7
0008 C108h	I/O PORT	Port function control register 8	PFCR8	8	8	2 to 3 PCLK *7
0008 C109h	I/O PORT	Port function control register 9	PFCR9	8	8	2 to 3 PCLK *7
0008 C280h	SYSTEM	Deep standby control register	DPSBYCR	8	8	4 to 5 PCLK *7
0008 C281h	SYSTEM	Deep standby wait control register	DPSWCR	8	8	4 to 5 PCLK *7
0008 C282h	SYSTEM	Deep standby interrupt enable register	DPSIER	8	8	4 to 5 PCLK *7
0008 C283h	SYSTEM	Deep standby interrupt flag register	DPSIFR	8	8	4 to 5 PCLK *7
0008 C284h	SYSTEM	Deep standby interrupt edge register	DPSIEGR	8	8	4 to 5 PCLK *7
0008 C285h	SYSTEM	Reset status register	RSTSR	8	8	4 to 5 PCLK *7
0008 C289h	FLASH	Flash write erase protection register	FWEPROR	8	8	4 to 5 PCLK *7
0008 C290h	SYSTEM	Deep standby backup register 0	DPSBKR0	8	8	4 to 5 PCLK *7
0008 C291h	SYSTEM	Deep standby backup register 1	DPSBKR1	8	8	4 to 5 PCLK *7
0008 C292h	SYSTEM	Deep standby backup register 2	DPSBKR2	8	8	4 to 5 PCLK *7
0008 C293h	SYSTEM	Deep standby backup register 3	DPSBKR3	8	8	4 to 5 PCLK *7
0008 C294h	SYSTEM	Deep standby backup register 4	DPSBKR4	8	8	4 to 5 PCLK *7
0008 C295h	SYSTEM	Deep standby backup register 5	DPSBKR5	8	8	4 to 5 PCLK *7
0008 C296h	SYSTEM	Deep standby backup register 6	DPSBKR6	8	8	4 to 5 PCLK *7
0008 C297h	SYSTEM	Deep standby backup register 7	DPSBKR7	8	8	4 to 5 PCLK *7
0008 C298h	SYSTEM	Deep standby backup register 8	DPSBKR8	8	8	4 to 5 PCLK *7
0008 C299h	SYSTEM	Deep standby backup register 9	DPSBKR9	8	8	4 to 5 PCLK *7
0008 C29Ah	SYSTEM	Deep standby backup register 10	DPSBKR10	8	8	4 to 5 PCLK *7
0008 C29Bh	SYSTEM	Deep standby backup register 11	DPSBKR11	8	8	4 to 5 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C29Ch	SYSTEM	Deep standby backup register 12	DPSBKR12	8	8	4 to 5 PCLK *7
0008 C29Dh	SYSTEM	Deep standby backup register 13	DPSBKR13	8	8	4 to 5 PCLK *7
0008 C29Eh	SYSTEM	Deep standby backup register 14	DPSBKR14	8	8	4 to 5 PCLK *7
0008 C29Fh	SYSTEM	Deep standby backup register 15	DPSBKR15	8	8	4 to 5 PCLK *7
0008 C2A0h	SYSTEM	Deep standby backup register 16	DPSBKR16	8	8	4 to 5 PCLK *7
0008 C2A1h	SYSTEM	Deep standby backup register 17	DPSBKR17	8	8	4 to 5 PCLK *7
0008 C2A2h	SYSTEM	Deep standby backup register 18	DPSBKR18	8	8	4 to 5 PCLK *7
0008 C2A3h	SYSTEM	Deep standby backup register 19	DPSBKR19	8	8	4 to 5 PCLK *7
0008 C2A4h	SYSTEM	Deep standby backup register 20	DPSBKR20	8	8	4 to 5 PCLK *7
0008 C2A5h	SYSTEM	Deep standby backup register 21	DPSBKR21	8	8	4 to 5 PCLK *7
0008 C2A6h	SYSTEM	Deep standby backup register 22	DPSBKR22	8	8	4 to 5 PCLK *7
0008 C2A7h	SYSTEM	Deep standby backup register 23	DPSBKR23	8	8	4 to 5 PCLK *7
0008 C2A8h	SYSTEM	Deep standby backup register 24	DPSBKR24	8	8	4 to 5 PCLK *7
0008 C2A9h	SYSTEM	Deep standby backup register 25	DPSBKR25	8	8	4 to 5 PCLK *7
0008 C2AAh	SYSTEM	Deep standby backup register 26	DPSBKR26	8	8	4 to 5 PCLK *7
0008 C2ABh	SYSTEM	Deep standby backup register 27	DPSBKR27	8	8	4 to 5 PCLK *7
0008 C2ACh	SYSTEM	Deep standby backup register 28	DPSBKR28	8	8	4 to 5 PCLK *7
0008 C2ADh	SYSTEM	Deep standby backup register 29	DPSBKR29	8	8	4 to 5 PCLK *7
0008 C2AEh	SYSTEM	Deep standby backup register 30	DPSBKR30	8	8	4 to 5 PCLK *7
0008 C2AFh	SYSTEM	Deep standby backup register 31	DPSBKR31	8	8	4 to 5 PCLK *7
0008 C300h	ICU	IRQ detection enable registrar 0	IRQER0	8	8	2 to 3 PCLK *7
0008 C301h	ICU	IRQ detection enable registrar 1	IRQER1	8	8	2 to 3 PCLK *7
0008 C302h	ICU	IRQ detection enable registrar 2	IRQER2	8	8	2 to 3 PCLK *7
0008 C303h	ICU	IRQ detection enable registrar 3	IRQER3	8	8	2 to 3 PCLK *7
0008 C304h	ICU	IRQ detection enable registrar 4	IRQER4	8	8	2 to 3 PCLK *7
0008 C305h	ICU	IRQ detection enable registrar 5	IRQER5	8	8	2 to 3 PCLK *7
0008 C306h	ICU	IRQ detection enable registrar 6	IRQER6	8	8	2 to 3 PCLK *7
0008 C307h	ICU	IRQ detection enable registrar 7	IRQER7	8	8	2 to 3 PCLK *7
0008 C308h	ICU	IRQ detection enable registrar 8	IRQER8	8	8	2 to 3 PCLK *7
0008 C309h	ICU	IRQ detection enable registrar 9	IRQER9	8	8	2 to 3 PCLK *7
0008 C30Ah	ICU	IRQ detection enable registrar 10	IRQER10	8	8	2 to 3 PCLK *7
0008 C30Bh	ICU	IRQ detection enable registrar 11	IRQER11	8	8	2 to 3 PCLK *7
0008 C30Ch	ICU	IRQ detection enable registrar 12	IRQER12	8	8	2 to 3 PCLK *7
0008 C30Dh	ICU	IRQ detection enable registrar 13	IRQER13	8	8	2 to 3 PCLK *7
0008 C30Eh	ICU	IRQ detection enable registrar 14	IRQER14	8	8	2 to 3 PCLK *7
0008 C30Fh	ICU	IRQ detection enable registrar 15	IRQER15	8	8	2 to 3 PCLK *7
0008 C320h	ICU	IRQ control register 0	IRQCR0	8	8	2 to 3 PCLK *7
0008 C321h	ICU	IRQ control register 1	IRQCR1	8	8	2 to 3 PCLK *7
0008 C322h	ICU	IRQ control register 2	IRQCR2	8	8	2 to 3 PCLK *7
0008 C323h	ICU	IRQ control register 3	IRQCR3	8	8	2 to 3 PCLK *7
0008 C324h	ICU	IRQ control register 4	IRQCR4	8	8	2 to 3 PCLK *7
0008 C325h	ICU	IRQ control register 5	IRQCR5	8	8	2 to 3 PCLK *7
0008 C326h	ICU	IRQ control register 6	IRQCR6	8	8	2 to 3 PCLK *7
0008 C327h	ICU	IRQ control register 7	IRQCR7	8	8	2 to 3 PCLK *7
0008 C328h	ICU	IRQ control register 8	IRQCR8	8	8	2 to 3 PCLK *7

5.3.2 Control Signal Timing

Table 5.6 Control Signal Timing

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V
ICLK = 8 to 100 MHz, BCLK = 8 to 25 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item	Symbol	Min.	Max.	Unit	Test Conditions
RES# pulse width (except for ROM, data flash programming/erasure)	t_{RESW}*1	20	—	t_{cyc}	Figure 5.6
		1.5	—	μs	
Internal reset time (during ROM, data flash programming/erasure)	t_{RESW2} *2	35	—	μs	
NMI pulse width	t_{NMIW}	200	—	ns	Figure 5.7
IRQ pulse width	t_{IRQW}	200	—	ns	Figure 5.8

Notes: 1. Both the time and the number of cycles should satisfy the specifications.
2. This is to specify the FCU reset and the WDT reset.

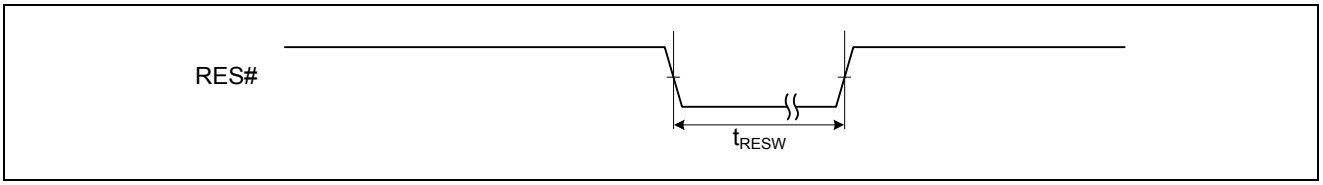


Figure 5.6 Reset Input Timing

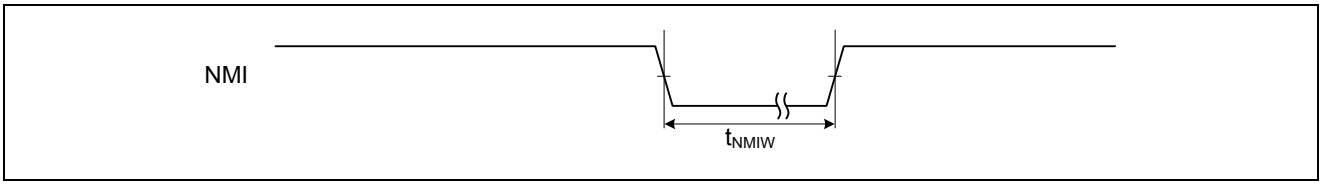


Figure 5.7 NMI Interrupt Input Timing

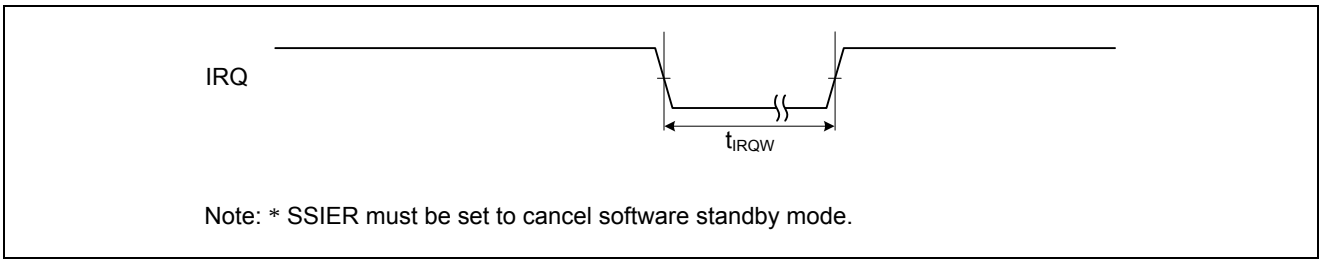


Figure 5.8 IRQ Interrupt Input Timing

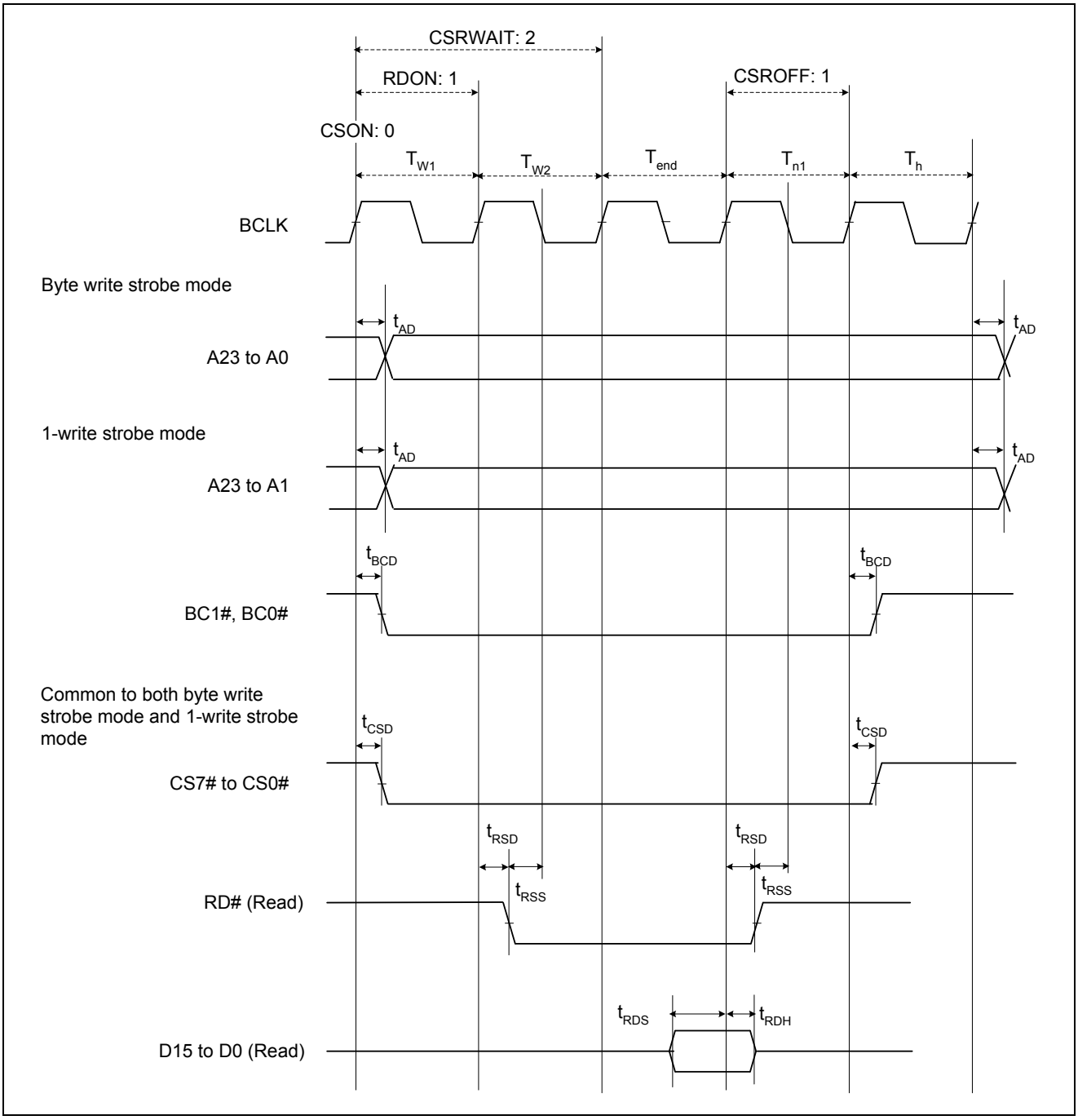


Figure 5.9 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

5.3.4 Timing of On-Chip Peripheral Modules

Table 5.8 Timing of On-Chip Peripheral Modules (1)

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V, PCLK = 8 to 50 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)
Output load conditions: V_{OH} = V_{CC} x 0.5, V_{OL} = V_{CC} x 0.5, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item			Symbol	Min.	Max.	Unit	Test Conditions
I/O ports	Output data delay time		t_{PWD}	—	40	ns	Figure 5.14
	Input data setup time		t_{PRS}	25	—	ns	
	Input data hold time		t_{PRH}	25	—	ns	
TPU	Timer output delay time		t_{TOCD}	—	40	ns	Figure 5.15
	Timer input setup time		t_{TICS}	25	—	ns	
	Timer clock input setup time		t_{TCKS}	25	—	ns	Figure 5.16
	Timer clock pulse width	Single-edge setting	t_{TCKWH}	1.5 x (1/PCLK)	—	t_{cyc}	
		Both-edge setting	t_{TCKWL}	2.5 x (1/PCLK)	—	t_{cyc}	
PPG	Pulse output delay time		t_{POD}	—	40	ns	Figure 5.17
8-bit timer	Timer output delay time		t_{TMOD}	—	40	ns	Figure 5.18
	Timer reset input setup time		t_{TMRS}	25	—	ns	Figure 5.19
	Timer clock input setup time		t_{TMCS}	25	—	ns	Figure 5.20
	Timer clock pulse width	Single-edge setting	t_{TMCWH}	1.5 x (1/PCLK)	—	t_{cyc}	
		Both-edge setting	t_{TMCWL}	2.5 x (1/PCLK)	—	t_{cyc}	
WDT	Overflow output delay time		t_{WOVD}	—	40	ns	Figure 5.21
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4 x (1/PCLK)	—	t_{cyc}	Figure 5.22
		Clock synchronous		6 x (1/PCLK)	—		
	Input clock pulse width		t_{SCKW}	0.4 x t_{Scyc}	0.6 x t_{Scyc}	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	20	ns	
	Input clock fall time		t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	4 x (1/PCLK)	—	t_{cyc}	
		Clock synchronous		6 x (1/PCLK)	—		
	Output clock pulse width		t_{SCKW}	0.4 x t_{Scyc}	0.6 x t_{Scyc}	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	20	ns	
	Output clock fall time		t_{SCKf}	—	20	ns	
	Transmit data delay time		t_{TXD}	—	40	ns	Figure 5.23
	Receive data setup time (clock synchronous)		t_{RXS}	40	—	ns	
	Receive data hold time (clock synchronous)		t_{RXH}	40	—	ns	
A/D converter	Trigger input setup time		t_{TRGS}	25	—	ns	Figure 5.24

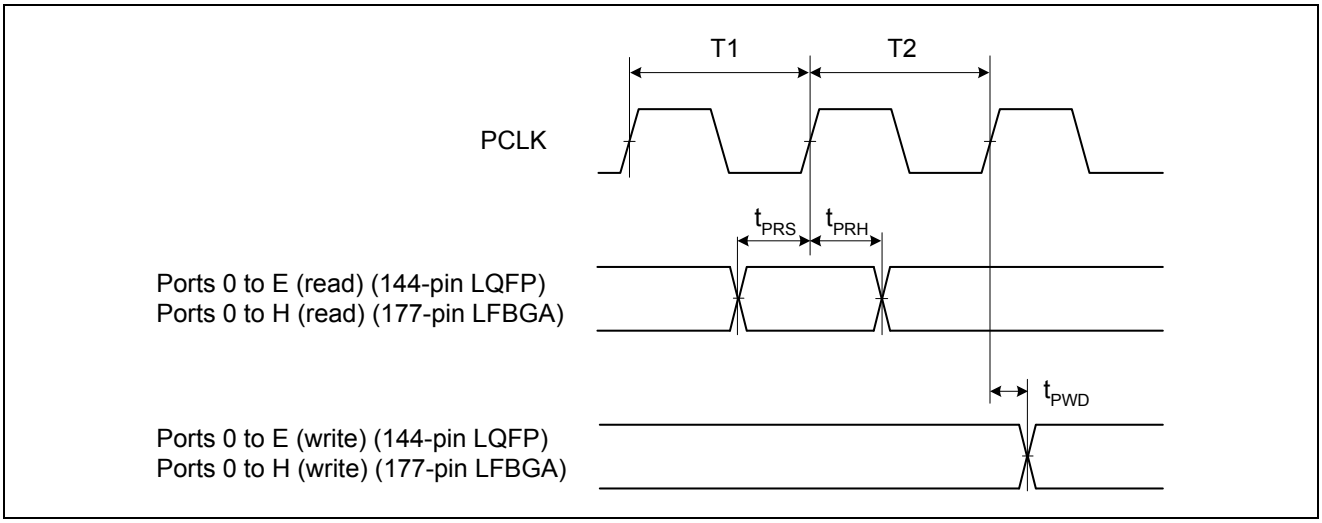


Figure 5.14 I/O Port Input/Output Timing

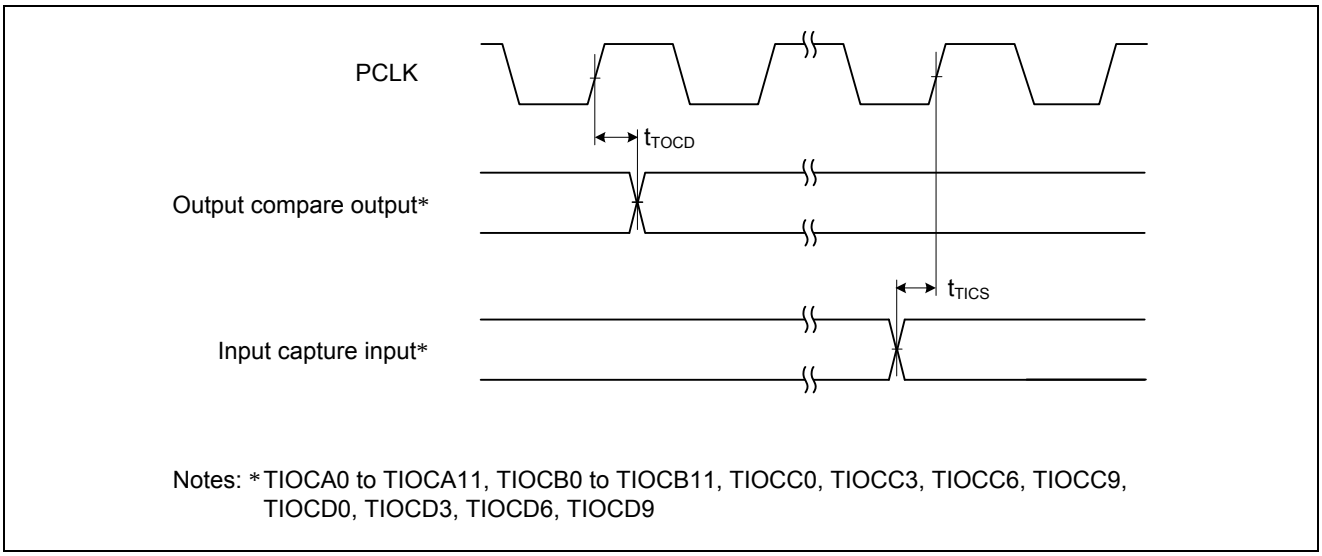


Figure 5.15 TPU Input/Output Timing

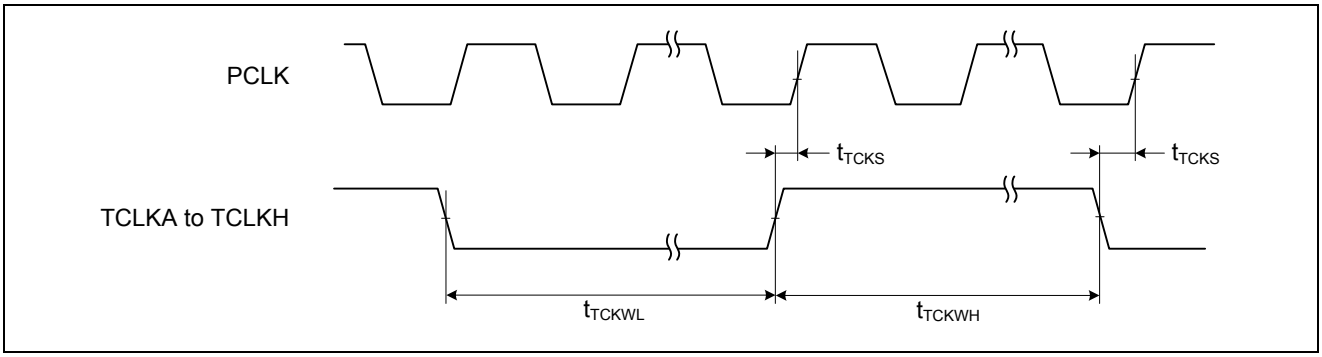


Figure 5.16 TPU Clock Input Timing

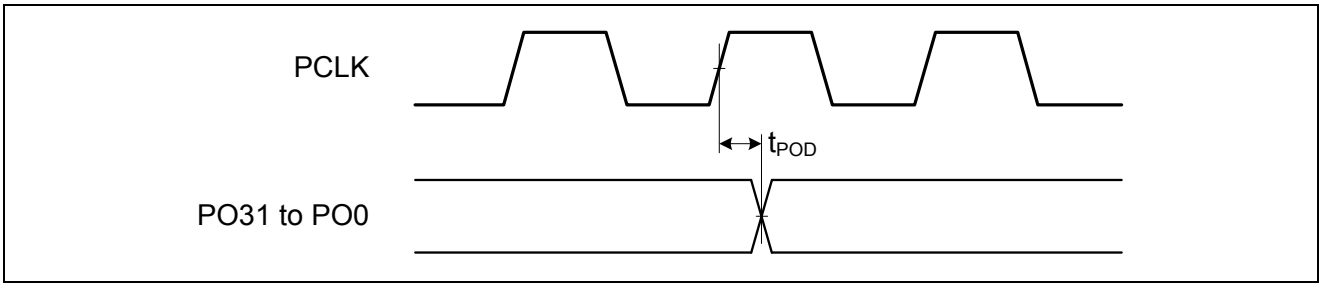


Figure 5.17 PPG Output Timing

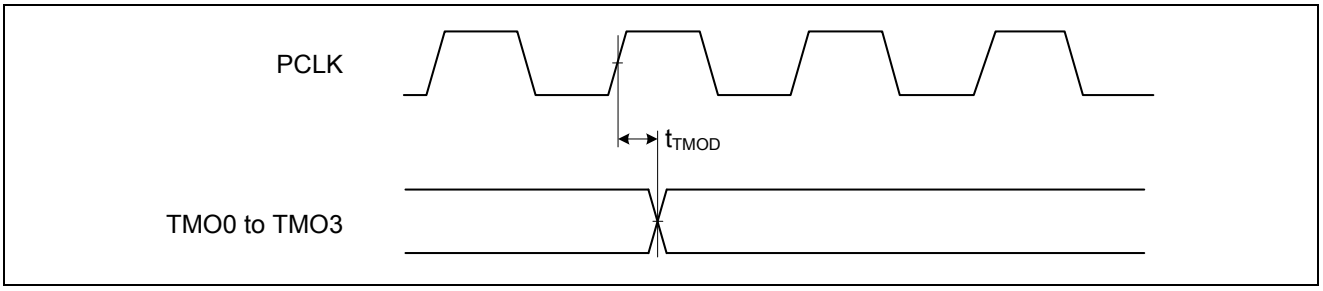


Figure 5.18 8-Bit Timer Output Timing

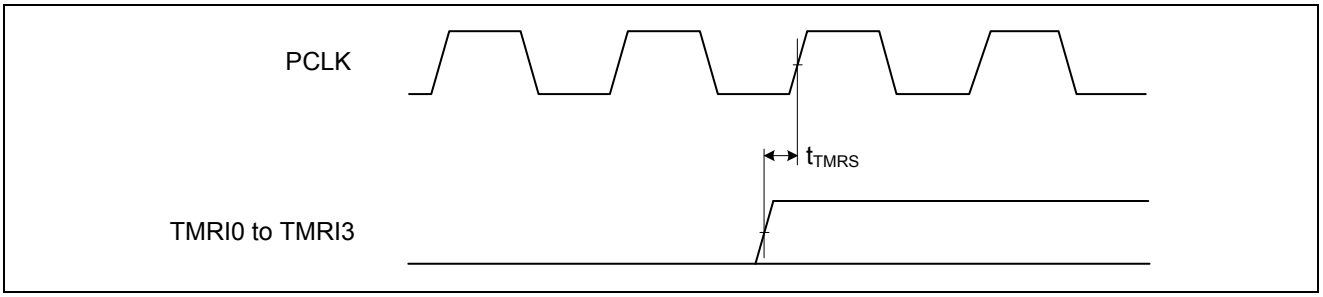


Figure 5.19 8-Bit Timer Reset Input Timing

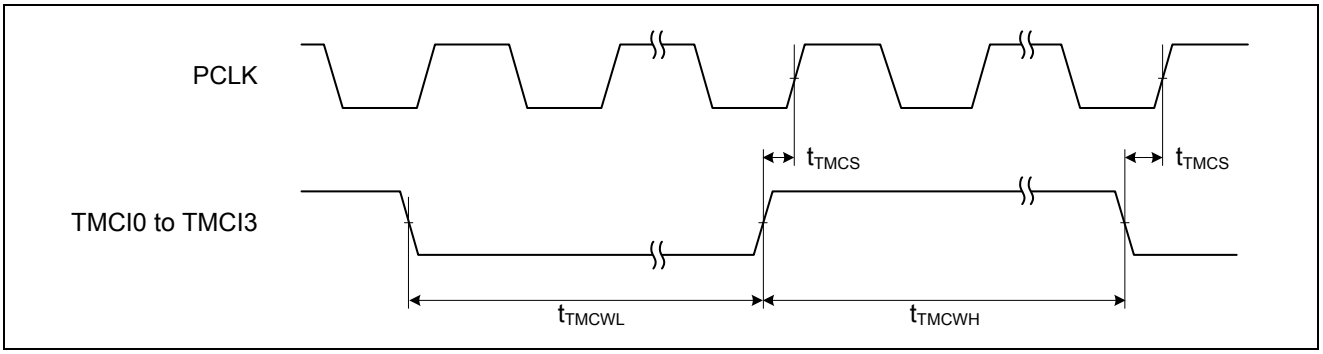


Figure 5.20 8-Bit Timer Clock Input Timing

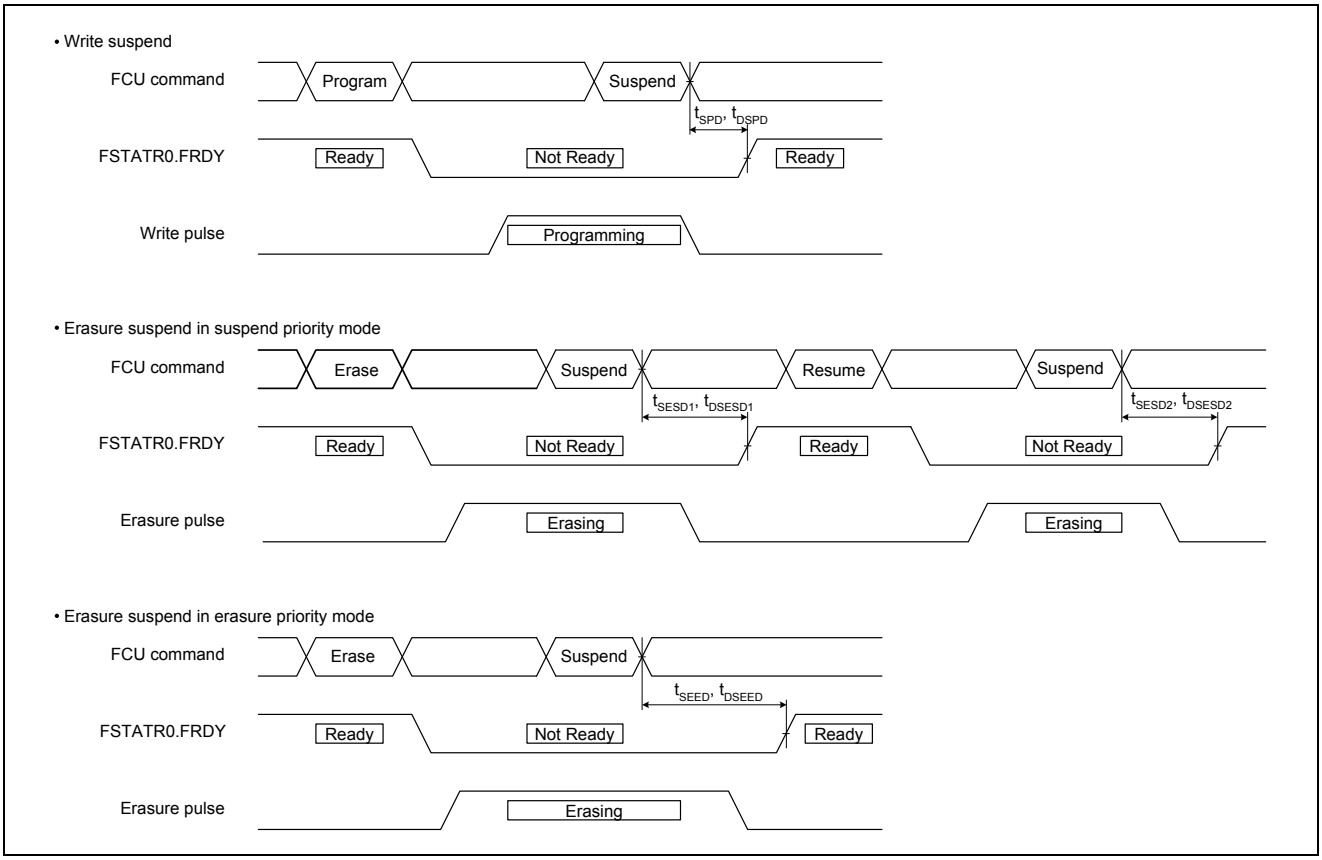


Figure 5.29 ROM, Data Flash Write/Erase Suspend Timing

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.