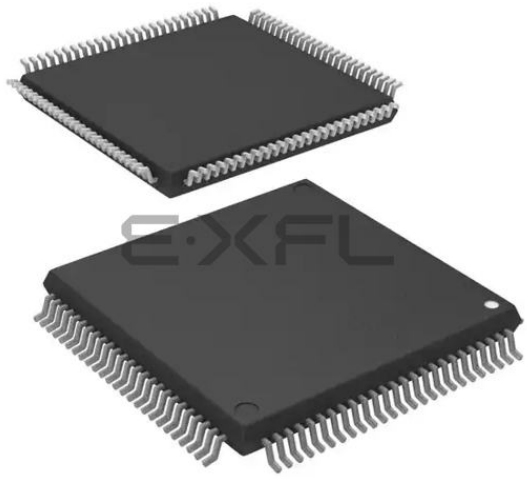

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	117
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 2x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56106vnfp-v0

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
F13		PA2		A2	PO18/ TIOCC6/ TCLKE			
F14		PA0		A0/BC0#	PO16/ TIOCA6			
F15		PA1		A1	PO17/ TIOCA6/ TIOCB6			
G1	RES#							
G2	XTAL							
G3		P85						
G4		P86						
G12		PA7		A7	PO23/ TIOCA8/ TIOCB8/ TCLKH			
G13		PA6		A6	PO22/ TIOCA8			
G14		PA4		A4	PO20/ TIOCA7			
G15		PA5		A5	PO21/ TIOCA7/ TIOCB7/ TCLKG			
H1	VCC							
H2			NMI					
H3	EXTAL							
H4	VSS							
H12		PB0		A8	PO24/ TIOCA9			
H13	VSS							
H14		PH0						
H15		PH1						
J1		PF5						
J2		PF4						
J3		PF6						
J4		P34	IRQ4-A		PO12/ TIOCA1			
J12		P72						
J13		P71		CS4#-C/ CS5#-C/ CS6#-C/ CS7#-C				
J14	VCC							

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
M6		P37			PO15/ TIOCA2/ TIOCB2/ TCLKD-A			
M7		P57		WAIT#				TRDATA3
M8		P83						
M9		P81						TRSYNC
M10		P51		WR1#/BC1#				
M11		PH4						
M12		PC7		A23/ CS4#-D/ CS7#-D		TxD5		
M13	VSS							
M14		PC0		A16				
M15		PB6		A14	PO30/ TIOCA11			
N1		P25			PO5/ TIOCA4/ TMCI1	RxD1		
N2		P24			PO4/ TIOCA4/ TIOCB4/ TMRI1			
N3		P20			PO0/ TIOCA3/ TIOCB3/ TMRI0	TxD0		
N4		P16	IRQ6-B		TCLKC-B	RxD3/SDA0		
N5		P12	IRQ2-B			RxD2		
N6		P36			PO14/ TIOCA2			
N7		P56						TRDATA2
N8	VSS							
N9		P80						
N10		P50		WR0#/WR#				
N11	VSS							
N12		P76	IRQ14-A					
N13		PH2						
N14		PC2		A18				
N15		PC1		A17				
P1		P23			PO3/ TIOCC3/ TIOCD3			

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
P2		P22			PO2/ TIOCC3/ TMO0	SCK0		
P3	PLLVCC							
P4		P15	IRQ5-B		TCLKB-B	SCK3/SCL1		
P5		P11	IRQ1-B			SCK2		
P6		P84						
P7		P54						TRDATA0
P8	VCC							
P9		P52		RD#				
P10		PH6						
P11	VCC							
P12		P77						
P13		PC6		A22/ CS6#-D		RxD5		
P14		PC4		A20				
P15	VCC							
R1		P21			PO1/ TIOCA3/ TMCI0	RxD0		
R2		P17	IRQ7-B		TCLKD-B	TxD3/SCL0	ADTRG1#	
R3	PLLVSS							
R4		P13	IRQ3-B			TxD2	ADTRG0#	
R5		P10	IRQ0-B					
R6		P35			PO13/ TIOCA1/ TIOCB1/ TCLKC-A			
R7		P55						TRDATA1
R8		P82						TRCLK
R9	BCLK	P53						
R10		PH7						
R11		PH5						
R12		PH3						
R13		P75						
R14		PC5		A21/ CS5#-D		SCK5		
R15		PC3		A19				

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
55		P54						TRDATA0
56		P83						
57	VSS							
58		P82						TRCLK
59	VCC							
60		P81						TRSYNC#
61		P80						
62	BCLK	P53						
63		P52		RD#				
64		P51		WR1#/BC1#				
65		P50		WR0#/WR#				
66		P77						
67		P76	IRQ14-A					
68		P75						
69		PC7		A23/ CS4#-D/ CS7#-D		TxD5		
70		PC6		A22/ CS6#-D		RxD5		
71		PC5		A21/ CS5#-D		SCK5		
72		PC4		A20				
73		PC3		A19				
74	VCC							
75		PC2		A18				
76	VSS							
77		PC1		A17				
78		PC0		A16				
79		PB7		A15	PO31/ TIOCA11/ TIOCB11			
80		PB6		A14	PO30/ TIOCA11			
81		PB5		A13	PO29/ TIOCA10/ TIOCB10			
82		PB4		A12	PO28/ TIOCA10			
83		PB3		A11	PO27/ TIOCC9/ TIOCD9			
84		PB2		A10	PO26/ TIOCC9			

1.5 Pin Functions

Table 1.5 lists the pin functions.

Table 1.5 Pin Functions

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	Input	Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	PLLVCC	Input	Power supply pin for the PLL circuit. Connect it to the system power supply.
	PLLVSS	Input	Ground pin for the PLL circuit
Clock	XTAL	Input	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the system clock for external devices.
Operating mode control	MD0, MD1, MDE	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	Input pin to enable on-chip emulator signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
	BSCANP	Input	Input pin to enable boundary-scan signal. When this pin is driven high, the boundary scan is enabled. When the boundary scan is not used, this pin should be driven low.
On-chip emulator	TRST#	Input	On-chip emulator pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid.
	TRDATA0 to TRDATA3	Output	These pins output the trace information.
Address bus	A0 to A23*1	Output	Output pins for the address
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus

Classifications	Pin Name	I/O	Description
16-bit timer pulse unit	TCLKA-A/TCLKA-B TCLKB-A/TCLKB-B TCLKC-A/TCLKC-B TCLKD-A/TCLKD-B TCLKE, TCLKF TCLKG, TCLKH	Input	Input pins for external clock signals
Programmable pulse generator	PO0 to PO31	Output	Output pins for the pulse signals
8-bit timer	TMO0 to TMO3	Output	Output pins for the compare match signals
	TMCI0 to TMCI3	Input	Input pins for the external clock signals that drive for the counters
	TMRI0 to TMRI3	Input	Input pins for the counter-reset signals
Watchdog timer	WDTOVF#	Output	Output pin for the counter-overflow signal in watchdog-timer mode
Serial communication interface	TxD0, TxD1, TxD2, TxD3, TxD4, TxD5, TxD6	Output	Output pins for data transmission
	RxD0, RxD1, RxD2, RxD3, RxD4, RxD5, RxD6	Input	Input pins for data reception
	SCK0, SCK1, SCK2, SCK3, SCK4, SCK5, SCK6	I/O	Input/output pins for clock signals
I^2C bus interface	SCL0, SCL1	I/O	Input/output pins for RIIC clocks. Bus can be directly driven by the NMOS open drain output.
	SDA0, SDA1	I/O	Input/output pins for RIIC data. Bus can be directly driven by the NMOS open drain output.
A/D converter	AN0 to AN15	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0# to ADTRG3#	Input	Input pins for the external trigger signals that start the A/D conversion
D/A converter	DA0, DA1	Output	Output pins for the analog signals from the D/A converter

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers.

R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).

Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.

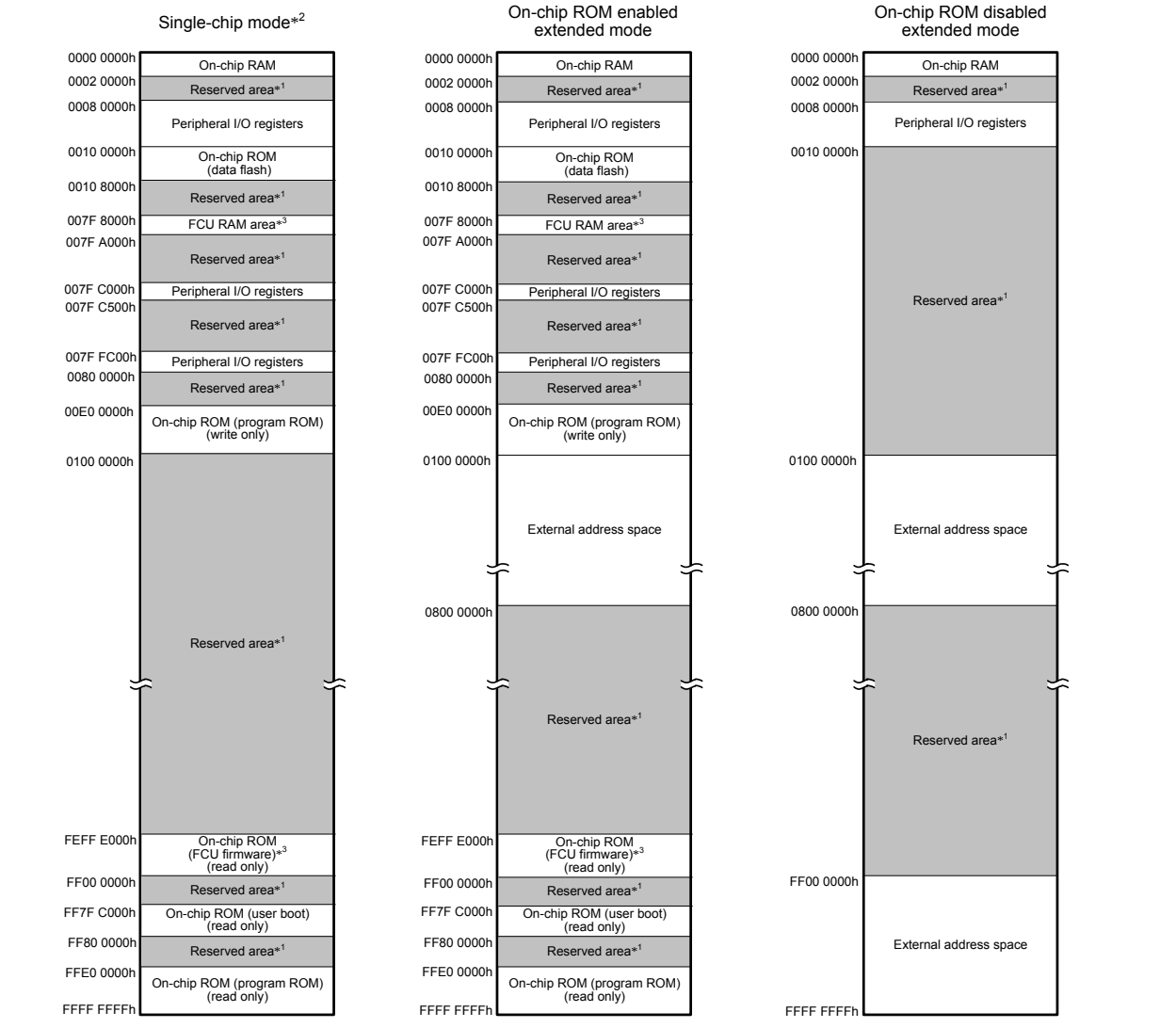
The FINTV specifies a branch destination address when a fast interrupt has been generated.

3. Address Space

3.1 Address Space

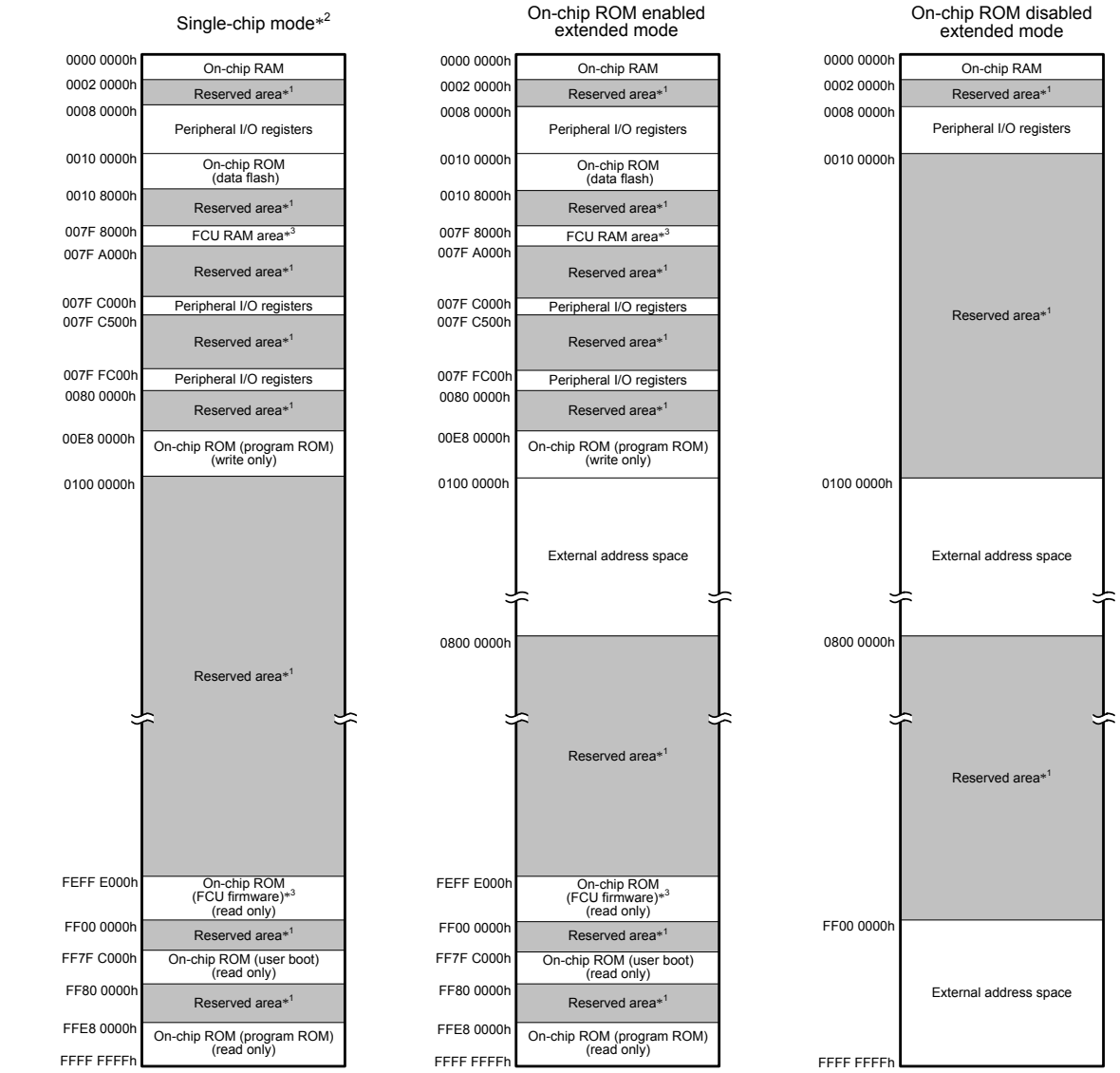
This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figures 3.1 to 3.4 show the memory maps in the respective operating modes of each product. Accessible areas will differ according to the operating mode and states of control bits.



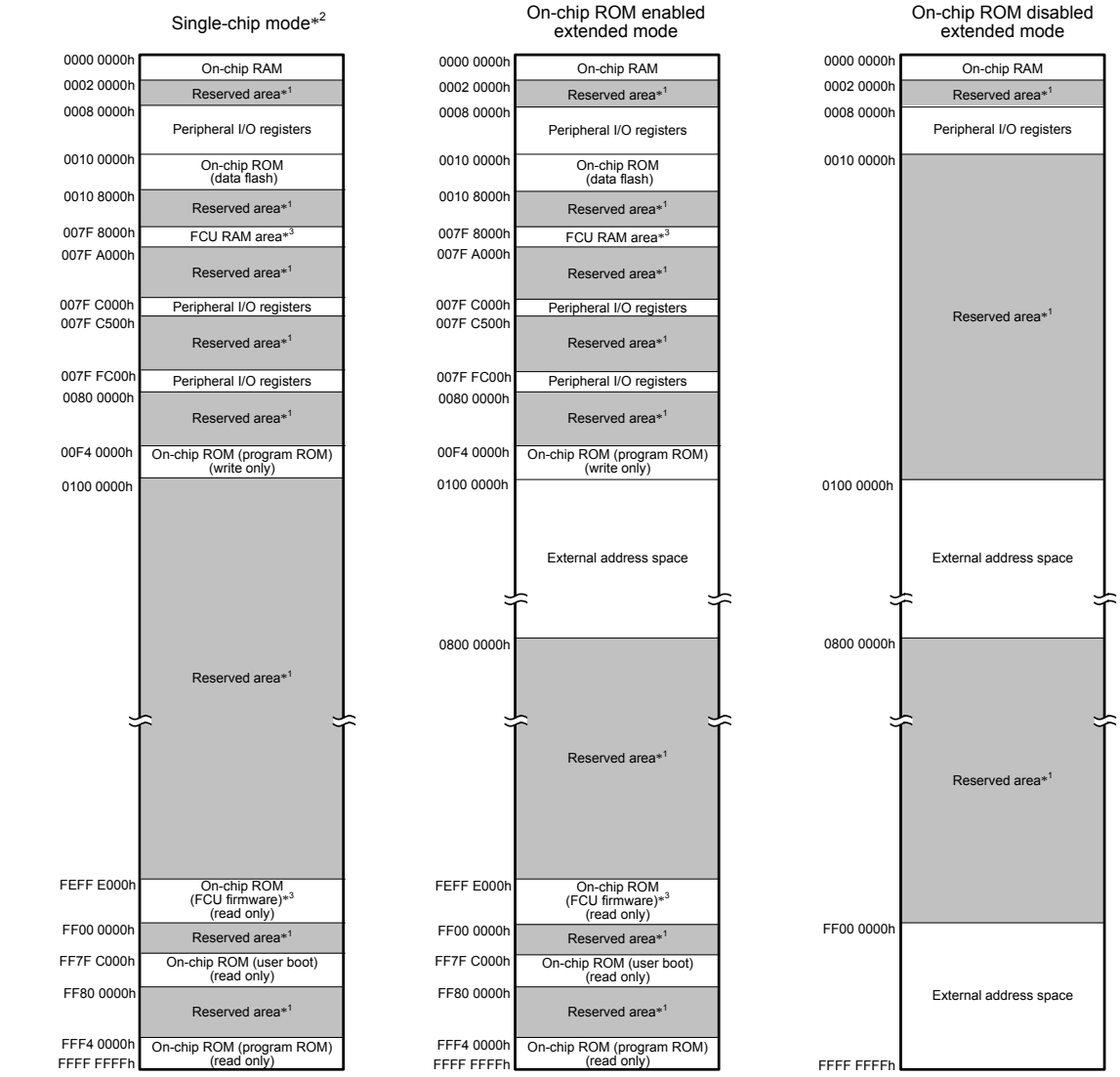
Notes: 1. A reserved area should not be accessed.
2. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
3. For details on the FCU, see section 26, ROM (Flash Memory for Code Storage) and section 27, Data Flash (Flash Memory for Data Storage) in the User's manual: Hardware.

Figure 3.1 Memory Map of the R5F56108



Notes: 1. A reserved area should not be accessed.
2. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
3. For details on the FCU, see section 26, ROM (Flash Memory for Code Storage) and section 27, Data Flash (Flash Memory for Data Storage) in the User's manual: Hardware.

Figure 3.2 Memory Map of the R5F56107



Notes: 1. A reserved area should not be accessed.
2. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
3. For details on the FCU, see section 26, ROM (Flash Memory for Code Storage) and section 27, Data Flash (Flash Memory for Data Storage) in the User's manual: Hardware.

Figure 3.4 Memory Map of the R5F56104

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 70A0h	ICU	Interrupt request register 160	IR160	8	8	2 ICLK
0008 70A1h	ICU	Interrupt request register 161	IR161	8	8	2 ICLK
0008 70A2h	ICU	Interrupt request register 162	IR162	8	8	2 ICLK
0008 70A5h	ICU	Interrupt request register 165	IR165	8	8	2 ICLK
0008 70A6h	ICU	Interrupt request register 166	IR166	8	8	2 ICLK
0008 70A7h	ICU	Interrupt request register 167	IR167	8	8	2 ICLK
0008 70A8h	ICU	Interrupt request register 168	IR168	8	8	2 ICLK
0008 70AAh	ICU	Interrupt request register 170	IR170	8	8	2 ICLK
0008 70ABh	ICU	Interrupt request register 171	IR171	8	8	2 ICLK
0008 70AEh	ICU	Interrupt request register 174	IR174	8	8	2 ICLK
0008 70AFh	ICU	Interrupt request register 175	IR175	8	8	2 ICLK
0008 70B0h	ICU	Interrupt request register 176	IR176	8	8	2 ICLK
0008 70B1h	ICU	Interrupt request register 177	IR177	8	8	2 ICLK
0008 70B2h	ICU	Interrupt request register 178	IR178	8	8	2 ICLK
0008 70B3h	ICU	Interrupt request register 179	IR179	8	8	2 ICLK
0008 70B4h	ICU	Interrupt request register 180	IR180	8	8	2 ICLK
0008 70B5h	ICU	Interrupt request register 181	IR181	8	8	2 ICLK
0008 70B6h	ICU	Interrupt request register 182	IR182	8	8	2 ICLK
0008 70B7h	ICU	Interrupt request register 183	IR183	8	8	2 ICLK
0008 70B8h	ICU	Interrupt request register 184	IR184	8	8	2 ICLK
0008 70B9h	ICU	Interrupt request register 185	IR185	8	8	2 ICLK
0008 70C6h	ICU	Interrupt request register 198	IR198	8	8	2 ICLK
0008 70C7h	ICU	Interrupt request register 199	IR199	8	8	2 ICLK
0008 70C8h	ICU	Interrupt request register 200	IR200	8	8	2 ICLK
0008 70C9h	ICU	Interrupt request register 201	IR201	8	8	2 ICLK
0008 70D6h	ICU	Interrupt request register 214	IR214	8	8	2 ICLK
0008 70D7h	ICU	Interrupt request register 215	IR215	8	8	2 ICLK
0008 70D8h	ICU	Interrupt request register 216	IR216	8	8	2 ICLK
0008 70D9h	ICU	Interrupt request register 217	IR217	8	8	2 ICLK
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8	2 ICLK
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8	2 ICLK
0008 70DCh	ICU	Interrupt request register 220	IR220	8	8	2 ICLK
0008 70DDh	ICU	Interrupt request register 221	IR221	8	8	2 ICLK
0008 70DEh	ICU	Interrupt request register 222	IR222	8	8	2 ICLK
0008 70DFh	ICU	Interrupt request register 223	IR223	8	8	2 ICLK
0008 70E0h	ICU	Interrupt request register 224	IR224	8	8	2 ICLK
0008 70E1h	ICU	Interrupt request register 225	IR225	8	8	2 ICLK
0008 70E2h	ICU	Interrupt request register 226	IR226	8	8	2 ICLK
0008 70E3h	ICU	Interrupt request register 227	IR227	8	8	2 ICLK
0008 70E4h	ICU	Interrupt request register 228	IR228	8	8	2 ICLK
0008 70E5h	ICU	Interrupt request register 229	IR229	8	8	2 ICLK
0008 70E6h	ICU	Interrupt request register 230	IR230	8	8	2 ICLK
0008 70E7h	ICU	Interrupt request register 231	IR231	8	8	2 ICLK
0008 70E8h	ICU	Interrupt request register 232	IR232	8	8	2 ICLK
0008 70E9h	ICU	Interrupt request register 233	IR233	8	8	2 ICLK

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7321h	ICU	Interrupt priority register 21	IPR21	8	8	2 ICLK
0008 7322h	ICU	Interrupt priority register 22	IPR22	8	8	2 ICLK
0008 7323h	ICU	Interrupt priority register 23	IPR23	8	8	2 ICLK
0008 7324h	ICU	Interrupt priority register 24	IPR24	8	8	2 ICLK
0008 7325h	ICU	Interrupt priority register 25	IPR25	8	8	2 ICLK
0008 7326h	ICU	Interrupt priority register 26	IPR26	8	8	2 ICLK
0008 7327h	ICU	Interrupt priority register 27	IPR27	8	8	2 ICLK
0008 7328h	ICU	Interrupt priority register 28	IPR28	8	8	2 ICLK
0008 7329h	ICU	Interrupt priority register 29	IPR29	8	8	2 ICLK
0008 732Ah	ICU	Interrupt priority register 2A	IPR2A	8	8	2 ICLK
0008 732Bh	ICU	Interrupt priority register 2B	IPR2B	8	8	2 ICLK
0008 732Ch	ICU	Interrupt priority register 2C	IPR2C	8	8	2 ICLK
0008 732Dh	ICU	Interrupt priority register 2D	IPR2D	8	8	2 ICLK
0008 732Eh	ICU	Interrupt priority register 2E	IPR2E	8	8	2 ICLK
0008 732Fh	ICU	Interrupt priority register 2F	IPR2F	8	8	2 ICLK
0008 7340h	ICU	Interrupt priority register 40	IPR40	8	8	2 ICLK
0008 7344h	ICU	Interrupt priority register 44	IPR44	8	8	2 ICLK
0008 7345h	ICU	Interrupt priority register 45	IPR45	8	8	2 ICLK
0008 7346h	ICU	Interrupt priority register 46	IPR46	8	8	2 ICLK
0008 7347h	ICU	Interrupt priority register 47	IPR47	8	8	2 ICLK
0008 734Ch	ICU	Interrupt priority register 4C	IPR4C	8	8	2 ICLK
0008 734Dh	ICU	Interrupt priority register 4D	IPR4D	8	8	2 ICLK
0008 734Eh	ICU	Interrupt priority register 4E	IPR4E	8	8	2 ICLK
0008 734Fh	ICU	Interrupt priority register 4F	IPR4F	8	8	2 ICLK
0008 7350h	ICU	Interrupt priority register 50	IPR50	8	8	2 ICLK
0008 7351h	ICU	Interrupt priority register 51	IPR51	8	8	2 ICLK
0008 7352h	ICU	Interrupt priority register 52	IPR52	8	8	2 ICLK
0008 7353h	ICU	Interrupt priority register 53	IPR53	8	8	2 ICLK
0008 7354h	ICU	Interrupt priority register 54	IPR54	8	8	2 ICLK
0008 7355h	ICU	Interrupt priority register 55	IPR55	8	8	2 ICLK
0008 7356h	ICU	Interrupt priority register 56	IPR56	8	8	2 ICLK
0008 7357h	ICU	Interrupt priority register 57	IPR57	8	8	2 ICLK
0008 7358h	ICU	Interrupt priority register 58	IPR58	8	8	2 ICLK
0008 7359h	ICU	Interrupt priority register 59	IPR59	8	8	2 ICLK
0008 735Ah	ICU	Interrupt priority register 5A	IPR5A	8	8	2 ICLK
0008 735Bh	ICU	Interrupt priority register 5B	IPR5B	8	8	2 ICLK
0008 735Ch	ICU	Interrupt priority register 5C	IPR5C	8	8	2 ICLK
0008 735Dh	ICU	Interrupt priority register 5D	IPR5D	8	8	2 ICLK
0008 735Eh	ICU	Interrupt priority register 5E	IPR5E	8	8	2 ICLK
0008 735Fh	ICU	Interrupt priority register 5F	IPR5F	8	8	2 ICLK
0008 7360h	ICU	Interrupt priority register 60	IPR60	8	8	2 ICLK
0008 7361h	ICU	Interrupt priority register 61	IPR61	8	8	2 ICLK
0008 7362h	ICU	Interrupt priority register 62	IPR62	8	8	2 ICLK
0008 7363h	ICU	Interrupt priority register 63	IPR63	8	8	2 ICLK
0008 7368h	ICU	Interrupt priority register 68	IPR68	8	8	2 ICLK

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 81C2h	TPU10	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 81C4h	TPU10	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 81C5h	TPU10	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 81C6h	TPU10	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 81C8h	TPU10	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 81CAh	TPU10	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 81D0h	TPU11	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 81D1h	TPU11	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 81D2h	TPU11	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 81D4h	TPU11	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 81D5h	TPU11	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 81D6h	TPU11	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 81D8h	TPU11	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 81DAh	TPU11	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 81E6h	PPG0	PPG output control register	PCR	8	8	2 to 3 PCLK *7
0008 81E7h	PPG0	PPG output mode register	PMR	8	8	2 to 3 PCLK *7
0008 81E8h	PPG0	Next data enable register H	NDERH	8	8	2 to 3 PCLK *7
0008 81E9h	PPG0	Next data enable register L	NDERL	8	8	2 to 3 PCLK *7
0008 81EAh	PPG0	Output data register H	PODRH	8	8	2 to 3 PCLK *7
0008 81EBh	PPG0	Output data register L	PODRL	8	8	2 to 3 PCLK *7
0008 81ECh*1	PPG0	Next data register H	NDRH	8	8	2 to 3 PCLK *7
0008 81EDh*2	PPG0	Next data register L	NDRL	8	8	2 to 3 PCLK *7
0008 81EEh*1	PPG0	Next data register H	NDRH	8	8	2 to 3 PCLK *7
0008 81EFh*2	PPG0	Next data register L	NDRL	8	8	2 to 3 PCLK *7
0008 81F0h	PPG1	PPG trigger select register	PTRSLR	8	8	2 to 3 PCLK *7
0008 81F6h	PPG1	PPG output control register	PCR	8	8	2 to 3 PCLK *7
0008 81F7h	PPG1	PPG output mode register	PMR	8	8	2 to 3 PCLK *7
0008 81F8h	PPG1	Next data enable register H	NDERH	8	8	2 to 3 PCLK *7
0008 81F9h	PPG1	Next data enable register L	NDERL	8	8	2 to 3 PCLK *7
0008 81FAh	PPG1	Output data register H	PODRH	8	8	2 to 3 PCLK *7
0008 81FBh	PPG1	Output data register L	PODRL	8	8	2 to 3 PCLK *7
0008 81FCh*3	PPG1	Next data register H	NDRH	8	8	2 to 3 PCLK *7
0008 81FDh*4	PPG1	Next data register L	NDRL	8	8	2 to 3 PCLK *7
0008 81FEh*3	PPG1	Next data register H	NDRH	8	8	2 to 3 PCLK *7
0008 81FFh*4	PPG1	Next data register L	NDRL	8	8	2 to 3 PCLK *7
0008 8200h	TMR0	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8201h	TMR1	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8202h	TMR0	Timer control/status register	TCSR	8	8	2 to 3 PCLK *7
0008 8203h	TMR1	Timer control/status register	TCSR	8	8	2 to 3 PCLK *7
0008 8204h	TMR0	Time constant register A	TCORA	8	8 or 16	2 to 3 PCLK *7
0008 8205h	TMR1	Time constant register A	TCORA	8	8 or 16*5	2 to 3 PCLK *7
0008 8206h	TMR0	Time constant register B	TCORB	8	8 or 16	2 to 3 PCLK *7
0008 8207h	TMR1	Time constant register B	TCORB	8	8 or 16*5	2 to 3 PCLK *7
0008 8208h	TMR0	Timer counter	TCNT	8	8 or 16	2 to 3 PCLK *7
0008 8209h	TMR1	Timer counter	TCNT	8	8 or 16*5	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 825Fh	SCI3	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8260h	SCI4	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8261h	SCI4	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 8262h	SCI4	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 8263h	SCI4	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 8264h	SCI4	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 8265h	SCI4	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 8266h	SCI4	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7
0008 8267h	SCI4	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8268h	SCI5	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8269h	SCI5	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 826Ah	SCI5	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 826Bh	SCI5	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 826Ch	SCI5	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 826Dh	SCI5	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 826Eh	SCI5	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7
0008 826Fh	SCI5	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8270h	SCI6	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8271h	SCI6	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 8272h	SCI6	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 8273h	SCI6	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 8274h	SCI6	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 8275h	SCI6	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 8276h	SCI6	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7
0008 8277h	SCI6	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8280h	CRC	CRC control register	CRCCR	8	8	2 to 3 PCLK *7
0008 8281h	CRC	CRC data input register	CRCDIR	8	8	2 to 3 PCLK *7
0008 8282h	CRC	CRC data output register	CRCDOR	16	16	2 to 3 PCLK *7
0008 8300h	RIIC0	I^2C bus control register 1	ICCR1	8	8	2 to 3 PCLK *7
0008 8301h	RIIC0	I^2C bus control register 2	ICCR2	8	8	2 to 3 PCLK *7
0008 8302h	RIIC0	I^2C bus mode register 1	ICMR1	8	8	2 to 3 PCLK *7
0008 8303h	RIIC0	I^2C bus mode register 2	ICMR2	8	8	2 to 3 PCLK *7
0008 8304h	RIIC0	I^2C bus mode register 3	ICMR3	8	8	2 to 3 PCLK *7
0008 8305h	RIIC0	I^2C bus function enable register	ICFER	8	8	2 to 3 PCLK *7
0008 8306h	RIIC0	I^2C bus status enable register	ICSER	8	8	2 to 3 PCLK *7
0008 8307h	RIIC0	I^2C bus interrupt enable register	ICIER	8	8	2 to 3 PCLK *7
0008 8308h	RIIC0	I^2C bus status register 1	ICSR1	8	8	2 to 3 PCLK *7
0008 8309h	RIIC0	I^2C bus status register 2	ICSR2	8	8	2 to 3 PCLK *7
0008 830Ah	RIIC0	Slave address register L0	SARL0	8	8	2 to 3 PCLK *7
0008 830Ah	RIIC0	Internal control for timeout L	TMOCNTL	16	16	2 to 3 PCLK *7
0008 830Bh	RIIC0	Slave address register U0	SARU0	8	8	2 to 3 PCLK *7
0008 830Bh	RIIC0	Internal control for timeout U	TMOCNTU	16	16	2 to 3 PCLK *7
0008 830Ch	RIIC0	Slave address register L1	SARL1	8	8	2 to 3 PCLK *7
0008 830Dh	RIIC0	Slave address register U1	SARU1	8	8	2 to 3 PCLK *7
0008 830Eh	RIIC0	Slave address register L2	SARL2	8	8	2 to 3 PCLK *7

5.3.2 Control Signal Timing

Table 5.6 Control Signal Timing

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V
ICLK = 8 to 100 MHz, BCLK = 8 to 25 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item	Symbol	Min.	Max.	Unit	Test Conditions
RES# pulse width (except for ROM, data flash programming/erasure)	t_{RESW}*1	20	—	t_{cyc}	Figure 5.6
		1.5	—	μs	
Internal reset time (during ROM, data flash programming/erasure)	t_{RESW2} *2	35	—	μs	
NMI pulse width	t_{NMIW}	200	—	ns	Figure 5.7
IRQ pulse width	t_{IRQW}	200	—	ns	Figure 5.8

Notes: 1. Both the time and the number of cycles should satisfy the specifications.
2. This is to specify the FCU reset and the WDT reset.

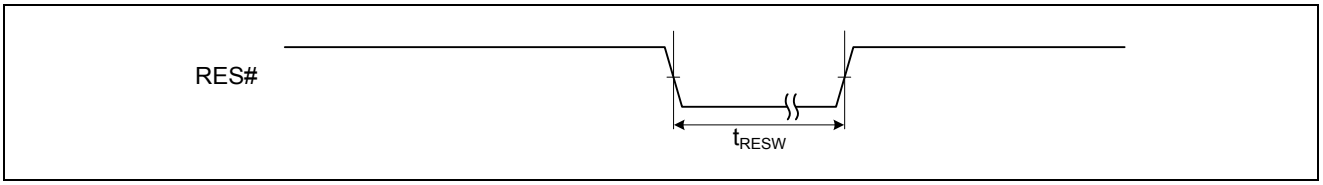


Figure 5.6 Reset Input Timing

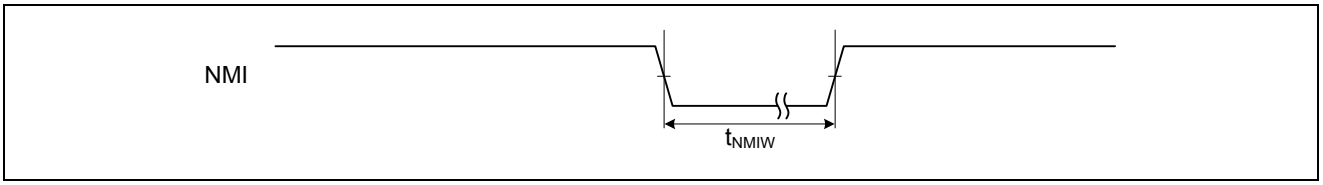


Figure 5.7 NMI Interrupt Input Timing

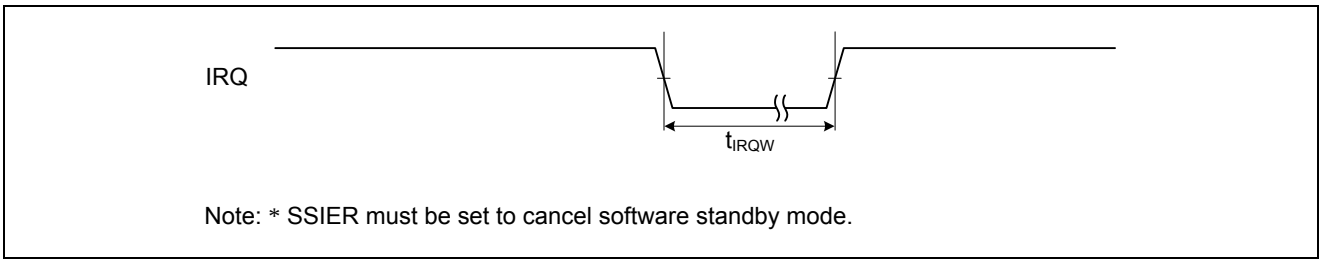


Figure 5.8 IRQ Interrupt Input Timing

Table 5.8 Timing of On-Chip Peripheral Modules (2)

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V, PCLK = 8 to 50 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item		Symbol	Min. *1*2	Max.	Unit	Test Conditions
RIIC (Standard-mode) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	8(10) x (1/PCLK) + 1300	—	ns	Figure 5.25
	SCL input high pulse width	t_{SCLH}	3(5) x (1/PCLK) + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	5x (1/PCLK) + 1000	—	ns	
	SCL, SDA input rising time	t_{Sr}	—	1000	ns	
	SCL, SDA input falling time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 x (1/PCLK)	ns	
	SDA input bus free time	t_{BUF}	5x (1/PCLK) + 1000	—	ns	
	Start condition input hold time	t_{STAH}	3(5) x (1/PCLK) + 300	—	ns	
	Re-start condition input setup time	t_{STAS}	5x (1/PCLK) + 1000	—	ns	
	Stop condition input setup time	t_{STOS}	3(5) x (1/PCLK) + 300	—	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	8(10) x (1/PCLK) + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(5) x (1/PCLK) + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	5 x (1/PCLK) + 300	—	ns	
	SCL, SDA input rising time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input falling time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 x (1/PCLK)	ns	
	SDA input bus free time	t_{BUF}	5 x (1/PCLK) + 300	—	ns	
	Start condition input hold time	t_{STAH}	3(5) x (1/PCLK) + 300	—	ns	
	Re-start condition input setup time	t_{STAS}	5 x (1/PCLK) + 300	—	ns	
	Stop condition input setup time	t_{STOS}	3(5) x (1/PCLK) + 300	—	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

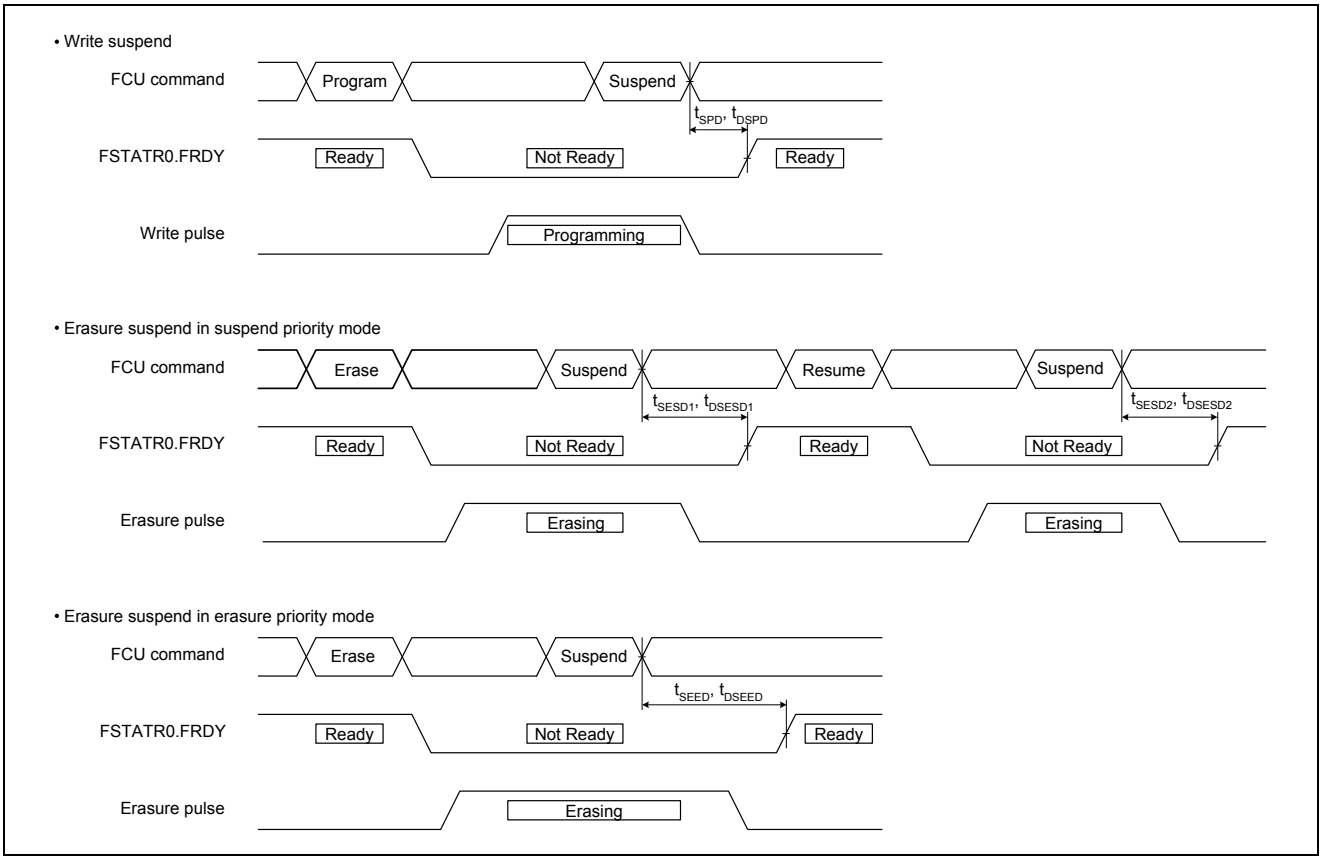
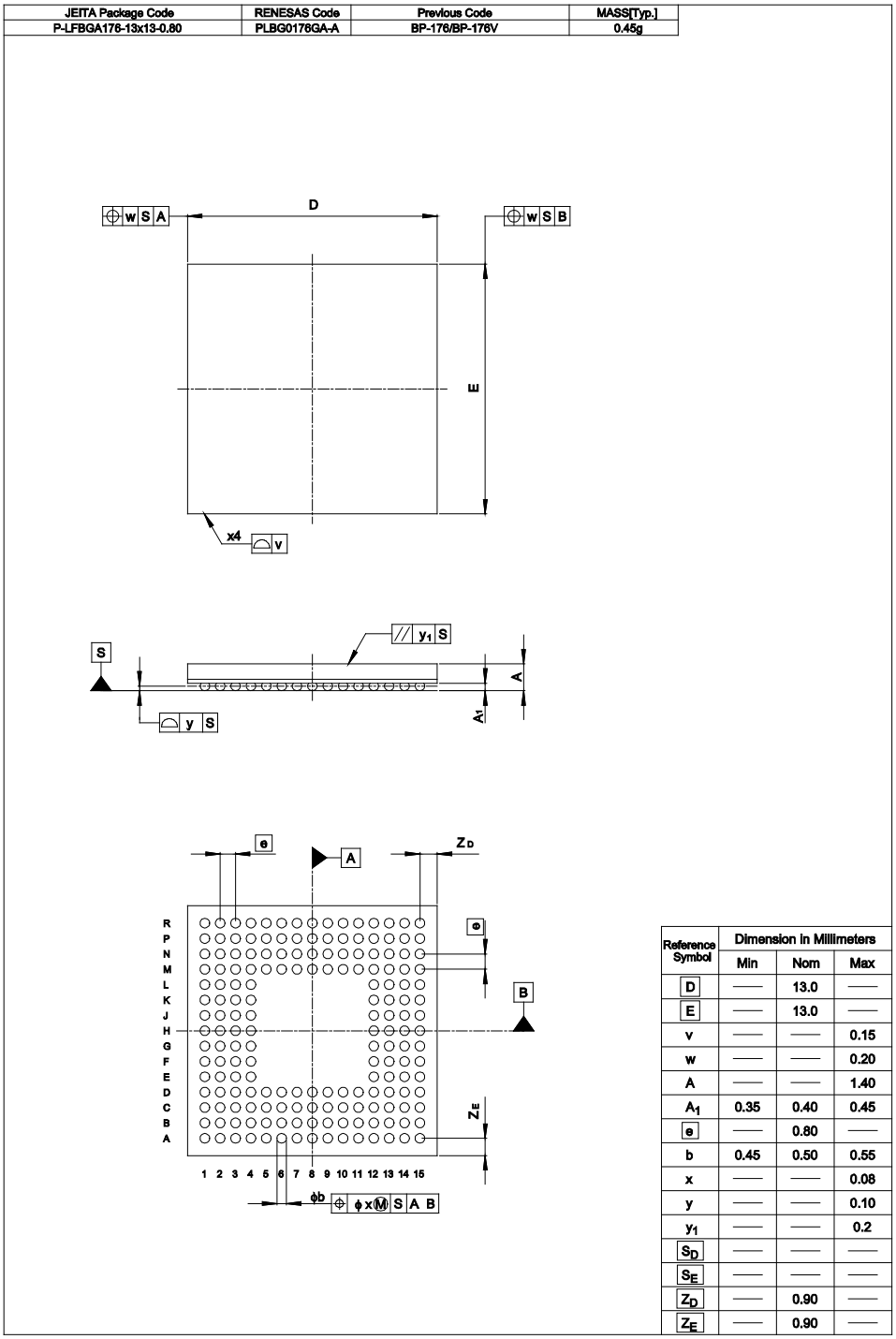


Figure 5.29 ROM, Data Flash Write/Erase Suspend Timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in "Packages" on Renesas Technology Corp. website.

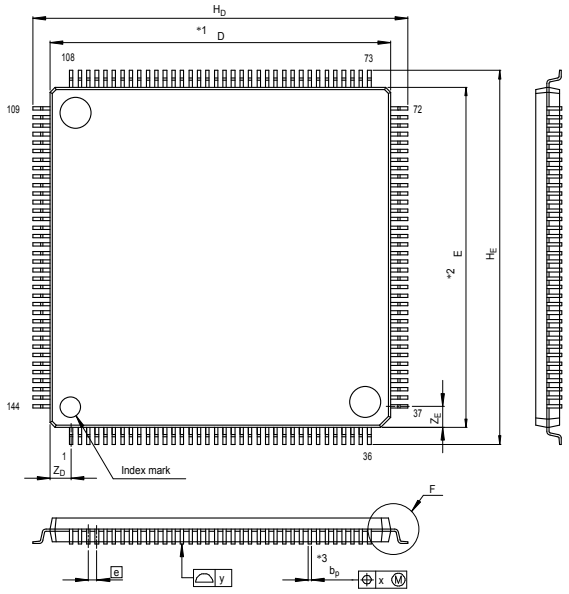
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA176-13x13-0.80	PLBG0176GA-A	BP-176/BP-176V	0.45g

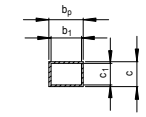


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	13.0	—
E	—	13.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.90	—
Z_E	—	0.90	—

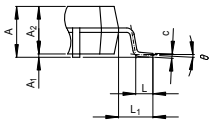
176-pin LFBGA (PLBG0176GA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

144-pin LQFP (PLQP0144KA-A)

REVISION HISTORY — RX610 Group Datasheet

		Description	
Rev.	**Data**	**Page**	**Summary**
0.50	Mar. 24, 2009	–	First edition issued
1.00	Apr. 22, 2011		1. Overview
		6	Figure 1.2 Block Diagram: Ports F to H added
		7	Figure 1.3 Pin Assignment of the 176-pin LFBGA, added
		10 to 15	Table 1.3 List of Pins and Pin Functions (176-Pin LFBGA), added
			Table 1.5 Pin Functions:
		21, 25	Description on the BSCANP, PF0 to PF6, PG0 to PG7, and PH0 to PH7 pins added
			4. I/O Registers
		34 to 54	Table 4.1 List of I/O Registers (Address Order), changed
			5. Electrical Characteristics
		58	Table 5.3 Permissible Output Currents, changed
		59	Table 5.5 Clock Timing: Oscillation settling time after leaving deep software standby mode (crystal), $t_{OSC3,}$ added
		60	Figure 5.2 Oscillation Settling Timing after Software Standby Mode, changed
		61	Figure 5.3 Oscillation Settling Timing after Deep Software Standby Mode, added
		71	Table 5.8 Timing of On-Chip Peripheral Modules (3), changed
		75	Figure 5.26 Boundary Scan TCK Timing, added
		75	Figure 5.27 Boundary Scan TRST# Timing, added
		76	Figure 5.28 Boundary Scan Input/Output Timing, added
1.20	Feb.20, 2013		1. Overview
		5	Table 1.2 List of Products, product lineup added
		23, 26	Table 1.5 Pin Functions, description on bus control changed, note added
			5. I/O register
		35 to 55	Table 5.1 List of I/O Registers (Address Order), changed