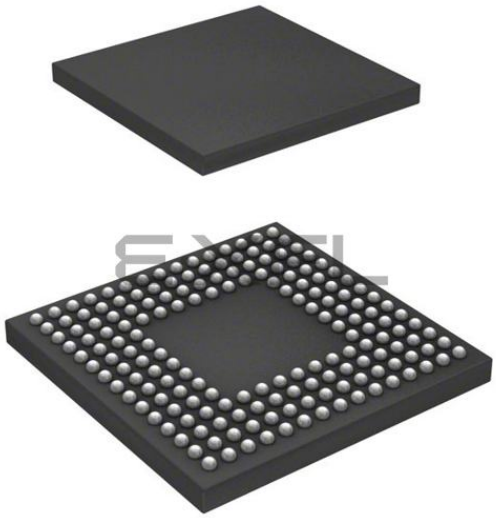
Renesas Electronics America Inc - R5F56106WDBG#U0 Datasheet



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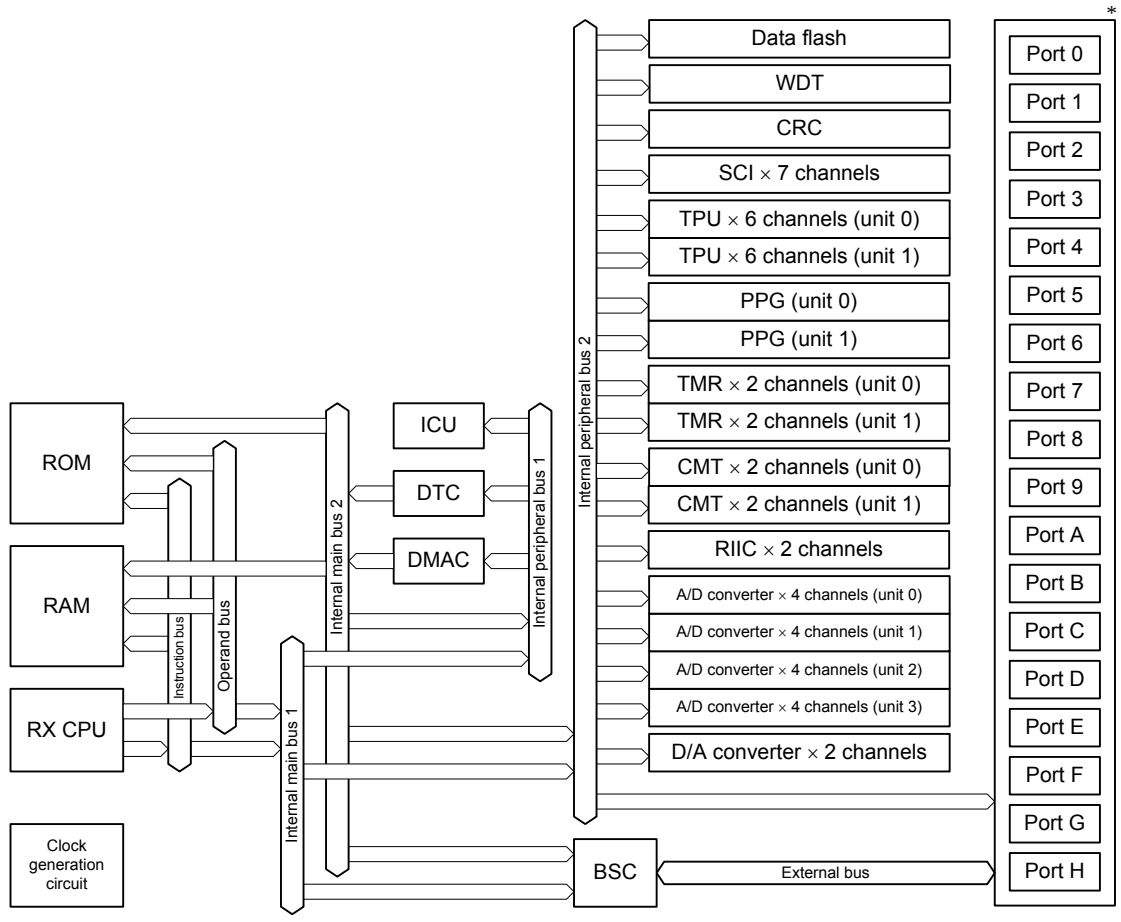
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	140
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 2x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56106wdbg-u0

Watchdog timer		• 8 bits x 1 channel • Select from among 8 counter-input clocks • Switchable between watchdog timer mode and interval timer mode
Communication function	Serial communication interface	• 7 channels • Serial communication mode: Asynchronous, clock synchronous, and smart card interface • On-chip baud rate generator allows any bit rate to be selected • Choice of LSB-first or MSB-first transfer • Enables average transfer rate clock input from TMR (SCI5, SCI6)
	I^2C bus interface	• 2 channels • Communication format I^2C bus format/SMBus format Master/slave selectable (For multi-master operation) • Maximum transfer rate: 1 Mbps
A/D converter		• 4 units (1 unit x 4 channels) • 10-bit resolution • Conversion time: 1.0 μs per channel (at 50-MHz (PCLK) operation) • Two kinds of operating modes Single mode and scan mode (single scan mode or continuous scan mode) • Sample-and-hold function • Three types of A/D conversion start Conversion can be started by software, a conversion start trigger by the timer (TPU or TMR), or an external trigger signal.
D/A converter		• 2 channels • 10-bit resolution • Output voltage: 0 V to VREFH
CRC calculator		• CRC code generation for arbitrary data lengths in 8-bit units • One of three generating polynomials selectable $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$ • CRC code generation for LSB-first or MSB-first communication selectable
Operating frequency		8 to 100 MHz
Power supply voltage		V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6V, VREFH = 3.0 to AV_{CC}
Supply current		50 mA (typ.) (regular specifications)
Operating temperature		−20 to +85°C (regular specifications), −40 to +85°C (wide-range specifications)
Package		176-pin LFBGA (PLBG0176GA-A) 144-pin LQFP (PLQP0144KA-A)

1.3 Block Diagram

Figure 1.2 shows a block diagram of the RX610 Group.



[Legend]

ICU:	Interrupt control unit	SCI:	Serial communications interfaces
DTC:	Data transfer controller	TPU:	16-bit timer pulse unit
DMAC:	DMA controller	PPG:	Programmable pulse generator
BSC:	Bus controller	TMR:	8-bit timer
WDT:	Watchdog timer	CMT:	Compare match timer
CRC:	CRC (Cyclic Redundancy Check) calculator	RIIC:	I^2C bus interface

Note: * Ports F and H are not included in the 144-pin LQFP package.

Figure 1.2 Block Diagram

Table 1.3 List of Pins and Pin Functions (176-Pin LFBGA)

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
A1		P04	IRQ12-A		TMCI3	TxD4		TDI
A2	AVCC							
A3	VREFL							
A4		P43	IRQ11-B				AN3	
A5		P46	IRQ14-B				AN6	
A6		P90					AN8	
A7		P93					AN11	
A8		P97					AN15	
A9		PG2						
A10		PD1		D1				
A11		P60		CS0#/ CS4#-A/ CS5#-B				
A12		P63		CS3#-A/ CS7#-A				
A13		PD4		D4				
A14		PD6		D6				
A15		PE0		D8				
B1		P67					DA1	
B2		P05	IRQ13-A		TMO3	RxD4		TCK
B3	VREFH							
B4		P42	IRQ10-B				AN2	
B5		P45	IRQ13-B				AN5	
B6	VCC							
B7		P92					AN10	
B8		P96					AN14	
B9		PG1						
B10		PD0		D0				
B11		P61		CS1#/ CS2#-B/ CS5#-A/ CS6#-B/ CS7#-B				
B12	VCC							
B13		PD5		D5				
B14		PE1		D9				
B15		PE2		D10				
C1		P02	IRQ10-A		TMO2	SCK6		TRST#
C2		P66					DA0	
C3		P03	IRQ11-A		TMRI3	SCK4		TMS
C4		P41	IRQ9-B				AN1	
C5		P47	IRQ15-B				AN7	

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
J15		P70		CS3#-B			ADTRG2#	
K1		P31	IRQ1-A		PO9/ TIOCA0/ TIOCB0			
K2		P30	IRQ0-A		PO8/ TIOCA0			
K3		P32	IRQ2-A		PO10/ TIOCC0/ TCLKA-A			
K4		P33	IRQ3-A		PO11/ TIOCC0/ TIOCD0/ TCLKB-A			
K12		PB2		A10	PO26/ TIOCC9			
K13		PB1		A9	PO25/ TIOCA9/ TIOCB9			
K14		P73						
K15		P74					ADTRG3#	
L1		PF2						
L2		PF1						
L3		PF3						
L4		PF0						
L12		PB7		A15	PO31/ TIOCA11/ TIOCB11			
L13		PB5		A13	PO29/ TIOCA10/ TIOCB10			
L14		PB4		A12	PO28/ TIOCA10			
L15		PB3		A11	PO27/ TIOCC9/ TIOCD9			
M1		P27			PO7/ TIOCA5/ TIOCB5	SCK1		
M2		P26			PO6/ TIOCA5/ TMO1	TxD1		
M3	VCC							
M4	VSS							
M5		P14	IRQ4-B		TCLKA-B	SDA1		

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
85		PB1		A9	PO25/ TIOCA9/ TIOCB9			
86		P74					ADTRG3#	
87		P73						
88		P72						
89		P71		CS4#-C/ CS5#-C/ CS6#-C/ CS7#-C				
90		P70		CS3#-B			ADTRG2#	
91	VCC							
92		PB0		A8	PO24/ TIOCA9			
93	VSS							
94		PA7		A7	PO23/ TIOCA8/ TIOCB8/ TCLKH			
95		PA6		A6	PO22/ TIOCA8			
96		PA5		A5	PO21/ TIOCA7/ TIOCB7/ TCLKG			
97		PA4		A4	PO20/ TIOCA7			
98		PA3		A3	PO19/ TIOCC6/ TIOCD6/ TCLKF			
99		PA2		A2	PO18/ TIOCC6/ TCLKE			
100		PA1		A1	PO17/ TIOCA6/ TIOCB6			
101		PA0		A0/BC0#	PO16/ TIOCA6			
102		PE7	IRQ7-A	D15				
103		PE6	IRQ6-A	D14				
104		PE5	IRQ5-A	D13				
105		PE4		D12				
106		PE3		D11				
107		PE2		D10				

1.5 Pin Functions

Table 1.5 lists the pin functions.

Table 1.5 Pin Functions

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	Input	Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	PLLVCC	Input	Power supply pin for the PLL circuit. Connect it to the system power supply.
	PLLVSS	Input	Ground pin for the PLL circuit
Clock	XTAL	Input	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the system clock for external devices.
Operating mode control	MD0, MD1, MDE	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	Input pin to enable on-chip emulator signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
	BSCANP	Input	Input pin to enable boundary-scan signal. When this pin is driven high, the boundary scan is enabled. When the boundary scan is not used, this pin should be driven low.
On-chip emulator	TRST#	Input	On-chip emulator pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid.
	TRDATA0 to TRDATA3	Output	These pins output the trace information.
Address bus	A0 to A23*1	Output	Output pins for the address
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus

Classifications	Pin Name	I/O	Description
16-bit timer pulse unit	TCLKA-A/TCLKA-B TCLKB-A/TCLKB-B TCLKC-A/TCLKC-B TCLKD-A/TCLKD-B TCLKE, TCLKF TCLKG, TCLKH	Input	Input pins for external clock signals
Programmable pulse generator	PO0 to PO31	Output	Output pins for the pulse signals
8-bit timer	TMO0 to TMO3	Output	Output pins for the compare match signals
	TMCI0 to TMCI3	Input	Input pins for the external clock signals that drive for the counters
	TMRI0 to TMRI3	Input	Input pins for the counter-reset signals
Watchdog timer	WDTOVF#	Output	Output pin for the counter-overflow signal in watchdog-timer mode
Serial communication interface	TxD0, TxD1, TxD2, TxD3, TxD4, TxD5, TxD6	Output	Output pins for data transmission
	RxD0, RxD1, RxD2, RxD3, RxD4, RxD5, RxD6	Input	Input pins for data reception
	SCK0, SCK1, SCK2, SCK3, SCK4, SCK5, SCK6	I/O	Input/output pins for clock signals
I^2C bus interface	SCL0, SCL1	I/O	Input/output pins for RIIC clocks. Bus can be directly driven by the NMOS open drain output.
	SDA0, SDA1	I/O	Input/output pins for RIIC data. Bus can be directly driven by the NMOS open drain output.
A/D converter	AN0 to AN15	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0# to ADTRG3#	Input	Input pins for the external trigger signals that start the A/D conversion
D/A converter	DA0, DA1	Output	Output pins for the analog signals from the D/A converter

4. I/O Registers

Table 4.1 List of I/O Registers (Address Order)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16	3 ICLK
0008 0002h	SYSTEM	Mode status register	MDSR	16	16	3 ICLK
0008 0006h	SYSTEM	System control register 0	SYSCR0	16	16	3 ICLK
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32	3 ICLK
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32	3 ICLK
0008 1300h	BSC	Bus error source clear register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus error monitor enable register	BEREN	8	8	2 ICLK
0008 1306h	BSC	Bus error interrupt enable register	BERIE	8	8	2 ICLK
0008 2000h	DMAC0	DMA current transfer source address register	DMCSA	32	32	4 to 5 ICLK
0008 2004h	DMAC0	DMA current transfer destination address register	DMCDA	32	32	4 to 5 ICLK
0008 2008h	DMAC0	DMA current transfer byte count register	DMCBC	32	32	4 to 5 ICLK
0008 200Ch	DMAC0	DMA mode register	DMMOD	32	32	4 to 5 ICLK
0008 2010h	DMAC1	DMA current transfer source address register	DMCSA	32	32	4 to 5 ICLK
0008 2014h	DMAC1	DMA current transfer destination address register	DMCDA	32	32	4 to 5 ICLK
0008 2018h	DMAC1	DMA current transfer byte count register	DMCBC	32	32	4 to 5 ICLK
0008 201Ch	DMAC1	DMA mode register	DMMOD	32	32	4 to 5 ICLK
0008 2020h	DMAC2	DMA current transfer source address register	DMCSA	32	32	4 to 5 ICLK
0008 2024h	DMAC2	DMA current transfer destination address register	DMCDA	32	32	4 to 5 ICLK
0008 2028h	DMAC2	DMA current transfer byte count register	DMCBC	32	32	4 to 5 ICLK
0008 202Ch	DMAC2	DMA mode register	DMMOD	32	32	4 to 5 ICLK
0008 2030h	DMAC3	DMA current transfer source address register	DMCSA	32	32	4 to 5 ICLK
0008 2034h	DMAC3	DMA current transfer destination address register	DMCDA	32	32	4 to 5 ICLK
0008 2038h	DMAC3	DMA current transfer byte count register	DMCBC	32	32	4 to 5 ICLK
0008 203Ch	DMAC3	DMA mode register	DMMOD	32	32	4 to 5 ICLK
0008 2200h	DMAC0	DMA reload transfer source address register	DMRSA	32	32	4 to 5 ICLK *8
0008 2204h	DMAC0	DMA reload transfer destination address register	DMRDA	32	32	4 to 5 ICLK *8
0008 2208h	DMAC0	DMA reload transfer byte count register	DMRBC	32	32	4 to 5 ICLK *8
0008 2210h	DMAC1	DMA reload transfer source address register	DMRSA	32	32	4 to 5 ICLK *8
0008 2214h	DMAC1	DMA reload transfer destination address register	DMRDA	32	32	4 to 5 ICLK *8
0008 2218h	DMAC1	DMA reload transfer byte count register	DMRBC	32	32	4 to 5 ICLK *8
0008 2220h	DMAC2	DMA reload transfer source address register	DMRSA	32	32	4 to 5 ICLK *8
0008 2224h	DMAC2	DMA reload transfer destination address register	DMRDA	32	32	4 to 5 ICLK *8
0008 2228h	DMAC2	DMA reload transfer byte count register	DMRBC	32	32	4 to 5 ICLK *8
0008 2230h	DMAC3	DMA reload transfer source address register	DMRSA	32	32	4 to 5 ICLK *8
0008 2234h	DMAC3	DMA reload transfer destination address register	DMRDA	32	32	4 to 5 ICLK *8
0008 2238h	DMAC3	DMA reload transfer byte count register	DMRBC	32	32	4 to 5 ICLK *8

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 71E3h	ICU	Interrupt request destination setting register 227	ISELR227	8	8	2 ICLK
0008 71E4h	ICU	Interrupt request destination setting register 228	ISELR228	8	8	2 ICLK
0008 71E7h	ICU	Interrupt request destination setting register 231	ISELR231	8	8	2 ICLK
0008 71E8h	ICU	Interrupt request destination setting register 232	ISELR232	8	8	2 ICLK
0008 71EBh	ICU	Interrupt request destination setting register 235	ISELR235	8	8	2 ICLK
0008 71ECh	ICU	Interrupt request destination setting register 236	ISELR236	8	8	2 ICLK
0008 71EFh	ICU	Interrupt request destination setting register 239	ISELR239	8	8	2 ICLK
0008 71F0h	ICU	Interrupt request destination setting register 240	ISELR240	8	8	2 ICLK
0008 71F7h	ICU	Interrupt request destination setting register 247	ISELR247	8	8	2 ICLK
0008 71F8h	ICU	Interrupt request destination setting register 248	ISELR248	8	8	2 ICLK
0008 71FBh	ICU	Interrupt request destination setting register 251	ISELR251	8	8	2 ICLK
0008 71FCh	ICU	Interrupt request destination setting register 252	ISELR252	8	8	2 ICLK
0008 71FDh	ICU	Interrupt request destination setting register 253	ISELR253	8	8	2ICLK
0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8	2 ICLK
0008 7203h	ICU	Interrupt request enable register 03	IER03	8	8	2 ICLK
0008 7208h	ICU	Interrupt request enable register 08	IER08	8	8	2 ICLK
0008 7209h	ICU	Interrupt request enable register 09	IER09	8	8	2 ICLK
0008 720Ch	ICU	Interrupt request enable register 0C	IER0C	8	8	2 ICLK
0008 720Dh	ICU	Interrupt request enable register 0D	IER0D	8	8	2 ICLK
0008 720Eh	ICU	Interrupt request enable register 0E	IER0E	8	8	2 ICLK
0008 720Fh	ICU	Interrupt request enable register 0F	IER0F	8	8	2 ICLK
0008 7210h	ICU	Interrupt request enable register 10	IER10	8	8	2 ICLK
0008 7211h	ICU	Interrupt request enable register 11	IER11	8	8	2 ICLK
0008 7212h	ICU	Interrupt request enable register 12	IER12	8	8	2 ICLK
0008 7213h	ICU	Interrupt request enable register 13	IER13	8	8	2 ICLK
0008 7214h	ICU	Interrupt request enable register 14	IER14	8	8	2 ICLK
0008 7215h	ICU	Interrupt request enable register 15	IER15	8	8	2 ICLK
0008 7216h	ICU	Interrupt request enable register 16	IER16	8	8	2 ICLK
0008 7217h	ICU	Interrupt request enable register 17	IER17	8	8	2 ICLK
0008 7218h	ICU	Interrupt request enable register 18	IER18	8	8	2 ICLK
0008 7219h	ICU	Interrupt request enable register 19	IER19	8	8	2 ICLK
0008 721Ah	ICU	Interrupt request enable register 1A	IER1A	8	8	2 ICLK
0008 721Bh	ICU	Interrupt request enable register 1B	IER1B	8	8	2 ICLK
0008 721Ch	ICU	Interrupt request enable register 1C	IER1C	8	8	2 ICLK
0008 721Dh	ICU	Interrupt request enable register 1D	IER1D	8	8	2 ICLK
0008 721Eh	ICU	Interrupt request enable register 1E	IER1E	8	8	2 ICLK
0008 721Fh	ICU	Interrupt request enable register 1F	IER1F	8	8	2 ICLK
0008 7300h	ICU	Interrupt priority register 00	IPR00	8	8	2 ICLK
0008 7301h	ICU	Interrupt priority register 01	IPR01	8	8	2 ICLK
0008 7302h	ICU	Interrupt priority register 02	IPR02	8	8	2 ICLK
0008 7304h	ICU	Interrupt priority register 04	IPR04	8	8	2 ICLK
0008 7305h	ICU	Interrupt priority register 05	IPR05	8	8	2 ICLK
0008 7306h	ICU	Interrupt priority register 06	IPR06	8	8	2 ICLK
0008 7307h	ICU	Interrupt priority register 07	IPR07	8	8	2 ICLK
0008 7320h	ICU	Interrupt priority register 20	IPR20	8	8	2 ICLK

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8116h	TPU0	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8118h	TPU0	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 811Ah	TPU0	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 811Ch	TPU0	Timer general register C	TGRC	16	16	2 to 3 PCLK *7
0008 811Eh	TPU0	Timer general register D	TGRD	16	16	2 to 3 PCLK *7
0008 8120h	TPU1	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8121h	TPU1	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8122h	TPU1	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8124h	TPU1	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8125h	TPU1	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8126h	TPU1	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8128h	TPU1	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 812Ah	TPU1	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 8130h	TPU2	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8131h	TPU2	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8132h	TPU2	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8134h	TPU2	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8135h	TPU2	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8136h	TPU2	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8138h	TPU2	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 813Ah	TPU2	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 8140h	TPU3	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8141h	TPU3	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8142h	TPU3	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK *7
0008 8143h	TPU3	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK *7
0008 8144h	TPU3	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8145h	TPU3	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8146h	TPU3	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8148h	TPU3	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 814Ah	TPU3	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 814Ch	TPU3	Timer general register C	TGRC	16	16	2 to 3 PCLK *7
0008 814Eh	TPU3	Timer general register D	TGRD	16	16	2 to 3 PCLK *7
0008 8150h	TPU4	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8151h	TPU4	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8152h	TPU4	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8154h	TPU4	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8155h	TPU4	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8156h	TPU4	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8158h	TPU4	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 815Ah	TPU4	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 8160h	TPU5	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8161h	TPU5	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8162h	TPU5	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8164h	TPU5	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8165h	TPU5	Timer status register	TSR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 820Ah	TMR0	Timer counter control register	TCCR	8	8 or 16	2 to 3 PCLK *7
0008 820Bh	TMR1	Timer counter control register	TCCR	8	8 or 16	2 to 3 PCLK *7
0008 8210h	TMR2	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8211h	TMR3	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8212h	TMR2	Timer control/status register	TCSR	8	8	2 to 3 PCLK *7
0008 8213h	TMR3	Timer control/status register	TCSR	8	8	2 to 3 PCLK *7
0008 8214h	TMR2	Time constant register A	TCORA	8	8 or 16	2 to 3 PCLK *7
0008 8215h	TMR3	Time constant register A	TCORA	8	8 or 16*5	2 to 3 PCLK *7
0008 8216h	TMR2	Time constant register B	TCORB	8	8 or 16	2 to 3 PCLK *7
0008 8217h	TMR3	Time constant register B	TCORB	8	8 or 16*5	2 to 3 PCLK *7
0008 8218h	TMR2	Timer counter	TCNT	8	8 or 16	2 to 3 PCLK *7
0008 8219h	TMR3	Timer counter	TCNT	8	8 or 16*5	2 to 3 PCLK *7
0008 821Ah	TMR2	Timer counter control register	TCCR	8	8 or 16	2 to 3 PCLK *7
0008 821Bh	TMR3	Timer counter control register	TCCR	8	8 or 16	2 to 3 PCLK *7
0008 8240h	SCI0	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8241h	SCI0	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 8242h	SCI0	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 8243h	SCI0	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 8244h	SCI0	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 8245h	SCI0	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 8246h	SCI0	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7
0008 8247h	SCI0	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8248h	SCI1	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8249h	SCI1	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 824Ah	SCI1	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 824Bh	SCI1	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 824Ch	SCI1	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 824Dh	SCI1	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 824Eh	SCI1	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7
0008 824Fh	SCI1	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8250h	SCI2	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8251h	SCI2	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 8252h	SCI2	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 8253h	SCI2	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 8254h	SCI2	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 8255h	SCI2	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 8256h	SCI2	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7
0008 8257h	SCI2	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8258h	SCI3	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8259h	SCI3	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 825Ah	SCI3	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 825Bh	SCI3	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 825Ch	SCI3	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 825Dh	SCI3	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 825Eh	SCI3	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C329h	ICU	IRQ control register 9	IRQCR9	8	8	2 to 3 PCLK *7
0008 C32Ah	ICU	IRQ control register 10	IRQCR10	8	8	2 to 3 PCLK *7
0008 C32Bh	ICU	IRQ control register 11	IRQCR11	8	8	2 to 3 PCLK *7
0008 C32Ch	ICU	IRQ control register 12	IRQCR12	8	8	2 to 3 PCLK *7
0008 C32Dh	ICU	IRQ control register 13	IRQCR13	8	8	2 to 3 PCLK *7
0008 C32Eh	ICU	IRQ control register 14	IRQCR14	8	8	2 to 3 PCLK *7
0008 C32Fh	ICU	IRQ control register 15	IRQCR15	8	8	2 to 3 PCLK *7
0008 C340h	ICU	Software standby release IRQ enable register	SSIER	16	16	2 to 3 PCLK *7
0008 C350h	ICU	Non-maskable interrupt enable register	NMIER	8	8	2 to 3 PCLK *7
0008 C351h	ICU	NMI pin interrupt control register	NMICR	8	8	2 to 3 PCLK *7
0008 C352h	ICU	Non-maskable interrupt status register	NMISR	8	8	2 to 3 PCLK *7
0008 C353h	ICU	Non-maskable interrupt clear register	NMICLR	8	8	2 to 3 PCLK *7
007F C402h	FLASH	Flash mode register	FMODR	8	8	2 to 3 PCLK *7
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2 to 3 PCLK *7
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2 to 3 PCLK *7
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2 to 3 PCLK *7
007F C440h	FLASH	Data flash read enable register	DFLRE	16	16	2 to 3 PCLK *7
007F C450h	FLASH	Data flash programming/erasure enable register	DFLWE	16	16	2 to 3 PCLK *7
007F C454h	FLASH	FCU RAM enable register	FCURAME	16	16	2 to 3 PCLK *7
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2 to 3 PCLK *7
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2 to 3 PCLK *7
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2 to 3 PCLK *7
007F FFB4h	FLASH	Flash protection register	FPROTR	16	16	2 to 3 PCLK *7
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2 to 3 PCLK *7
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2 to 3 PCLK *7
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2 to 3 PCLK *7
007F FFCAh	FLASH	Data flash blank check control register	DFLBCCNT	16	16	2 to 3 PCLK *7
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2 to 3 PCLK *7
007F FFCEh	FLASH	Data flash blank check status register	DFLBCSTAT	16	16	2 to 3 PCLK *7
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2 to 3 PCLK *7

Notes:
1. When the same output trigger is specified for pulse output groups 2 and 3 by the PPG0.PCR setting, the PPG0.NDRH address is 000881ECh. When different output triggers are specified, the PPG0.NDRH addresses for pulse output groups 2 and 3 are 000881EEh and 000881ECh, respectively.
2. When the same output trigger is specified for pulse output groups 0 and 1 by the PPG0.PCR setting, the PPG0.NDRL address is 000881EDh. When different output triggers are specified, the PPG0.NDRL addresses for pulse output groups 0 and 1 are 000881EFh and 000881EDh, respectively.
3. When the same output trigger is specified for pulse output groups 6 and 7 by the PPG1.PCR setting, the PPG1.NDRH address is 000881FCh. When different output triggers are specified, the PPG1.NDRH addresses for pulse output groups 6 and 7 are 000881FEh and 000881FCh, respectively.
4. When the same output trigger is specified for pulse output groups 4 and 5 by the PPG1.PCR setting, the PPG1.NDRL address is 000881FDh. When different output triggers are specified, the PPG1.NDRL addresses for pulse output groups 4 and 5 are 000881FFh and 000881FDh, respectively.
5. 16-bit access to odd addresses is prohibited. When 16-bit access is required, access is at the address corresponding to TMR0 or TMR2.
6. For certain bits, functions differ according to whether the mode is serial communications or smart card interface.
7. The number of access cycles varies depending on the number of divided cycles for clock synchronization (0 to one PCLK).
8. The number of access cycles may be 5 ICLK if the register is accessed during the DMAC operation.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}, $PLLV_{CC}$	-0.3 to +4.6	V
Input voltage (except for ports 0, 14 to 17)	V_{in}	-0.3 to V_{CC} +0.3	V
Input voltage (ports 0, 14 to 17*1)	V_{in}	-0.3 to +6.5	V
Reference power supply voltage	V_{REFH}	-0.3 to V_{CC} +0.3	V
Analog power supply voltage	AV_{CC}*2	-0.3 to +4.6	V
Analog input voltage	V_{AN}	-0.3 to V_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: -20 to +85	°C
		Wide-range specifications: -40 to +85	
Storage temperature	T_{stg}	-55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Notes: 1. Ports 0, and 14 to 17 are 5 V tolerant.

2. Connect AV_{CC} to V_{CC}. When neither the A/D converter nor the D/A converter is in use, do not leave the AV_{SS}, V_{REFH}, and V_{REFL} pins open. Connect the AV_{CC} and V_{REFH} pins to V_{CC}, and the AV_{SS} and V_{REFL} pins to V_{SS}, respectively.

5.2 DC Characteristics

Table 5.2 DC Characteristics

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin*1 TPU input pin*1 TMR input pin*1 SCI input pin*1 ADTRG# input pin*1 RES#, NMI	V_{IH}	V_{CC} x 0.8	—	V_{CC} + 0.3	V	
		V_{IL}	-0.3	—	V_{CC} x 0.2		
		ΔV_T	V_{CC} x 0.06	—	—		
	RIIC input pin	V_{IH}	V_{CC} x 0.7	—	5.8		
		V_{IL}	-0.3	—	V_{CC} x 0.3		
		ΔV_T	V_{CC} x 0.05	—	—		
	Ports 0, 14 to 17*2	V_{IH}	V_{CC} x 0.8	—	5.8		
		V_{IL}	-0.3	—	V_{CC} x 0.2		
	Ports 10 to 13, ports 2 to E (144-pin LQFP) ports 2 to H (176-pin LFBGA) Other input pins	V_{IH}	V_{CC} x 0.8	—	V_{CC} + 0.3		
		V_{IL}	-0.3	—	V_{CC} x 0.2		
Input high voltage (except Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	V_{CC} x 0.9	—	V_{CC} + 0.3	V	
	EXTAL		V_{CC} x 0.8	—	V_{CC} + 0.3		
	D0 to D15		V_{CC} x 0.7	—	V_{CC} + 0.3		
Input low voltage (except Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	-0.3	—	V_{CC} x 0.1	V	
	EXTAL		-0.3	—	V_{CC} x 0.2		
	D0 to D15		-0.3	—	V_{CC} x 0.3		
Output high voltage	All output pins	V_{OH}	V_{CC}-0.5	—	—	V	I_{OH} = -1 mA
Output low voltage	All output pins (except for RIIC pins)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	RIIC pins		—	—	0.4		I_{OL} = 3.0 mA
			—	—	0.6		I_{OL} = 6.0 mA
	RIIC pins (only P14 and P15 in channel 1)		—	—	0.4		I_{OL} = 15 mA (ICFER.FMPE = 1)
			—	0.4	—		I_{OL} = 20 mA (ICFER.FMPE = 1)
Input leakage current	RES#, MD pin, EMLE, NMI	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, V_{CC}
Three-state leakage current (off state)	Ports 10 to 13, ports 2 to E (144-pin LQFP) ports 2 to H (176-pin LFBGA)	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, V_{CC}
	Port 0, ports 14 to 17		—	—	5.0		

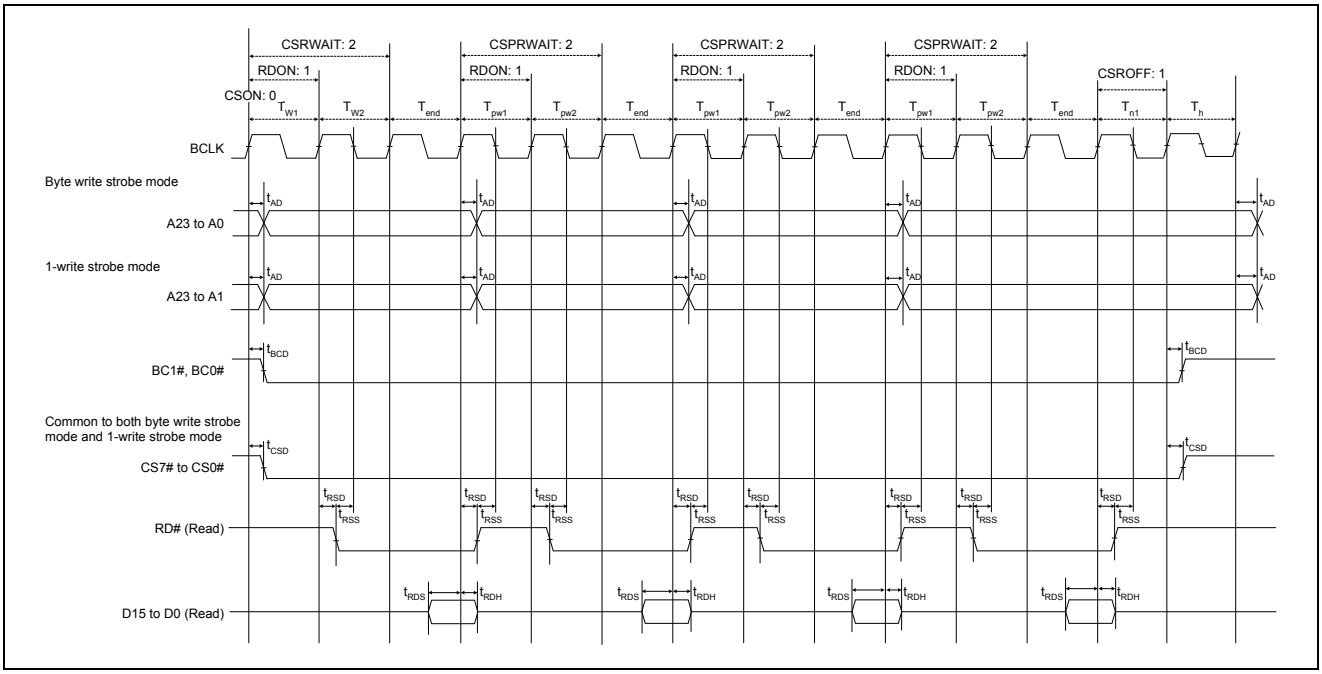


Figure 5.11 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)

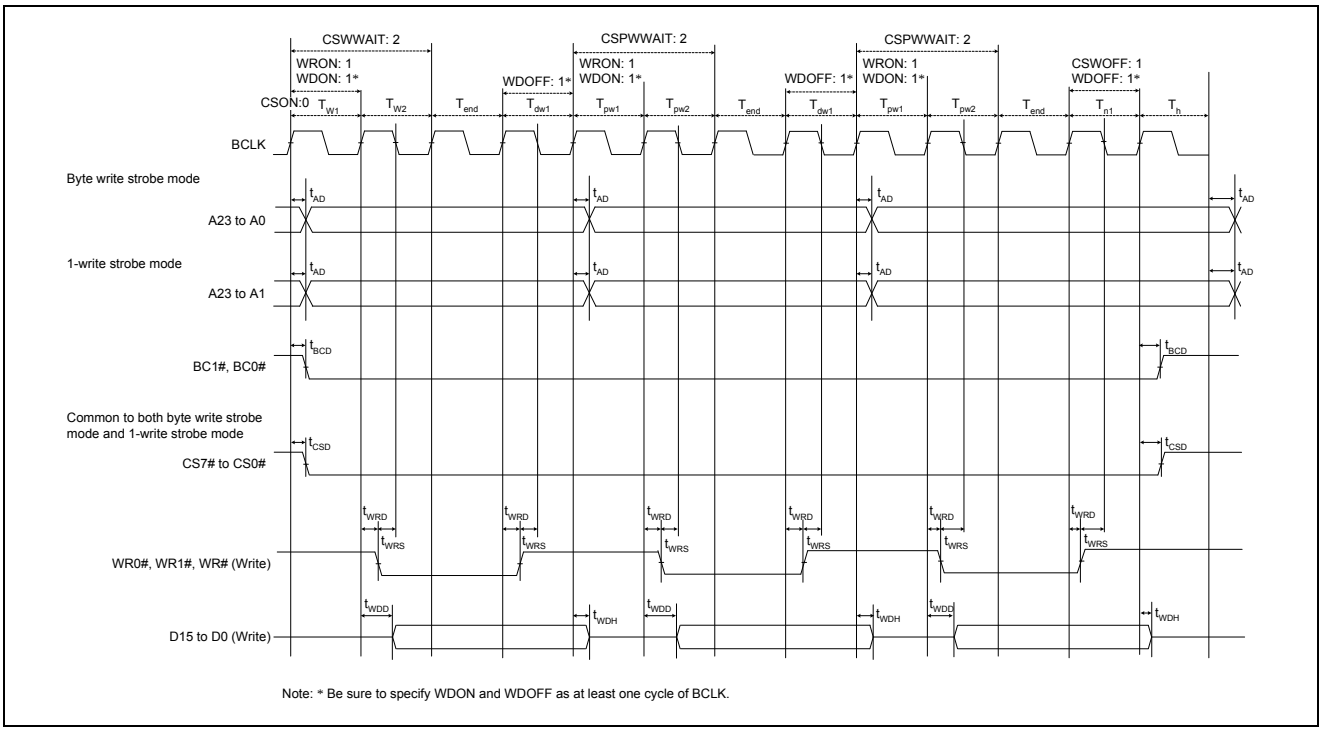


Figure 5.12 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

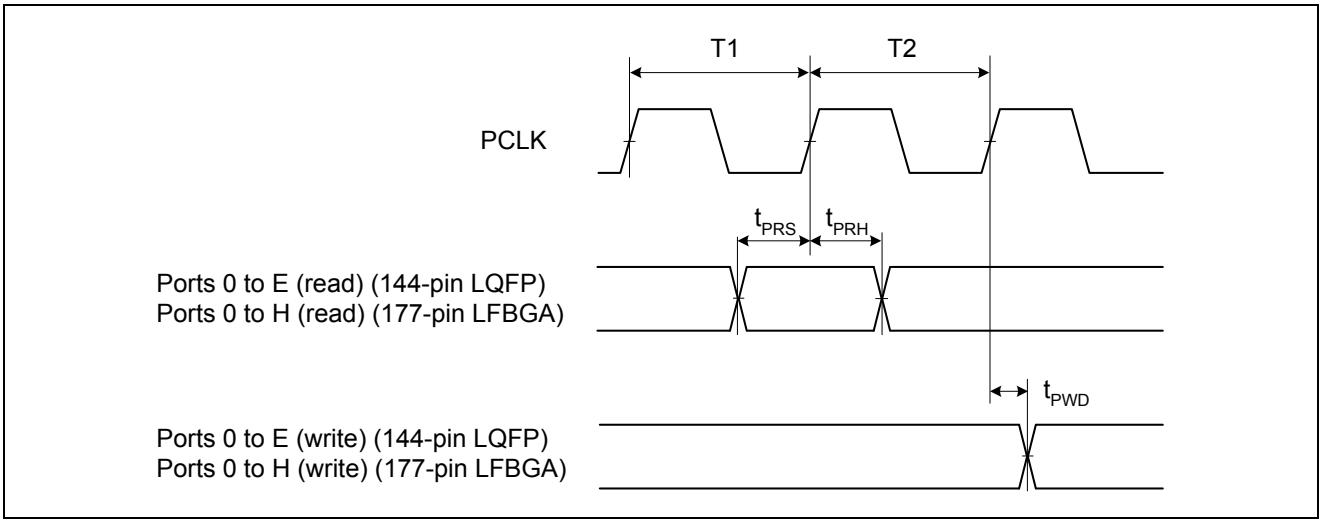


Figure 5.14 I/O Port Input/Output Timing

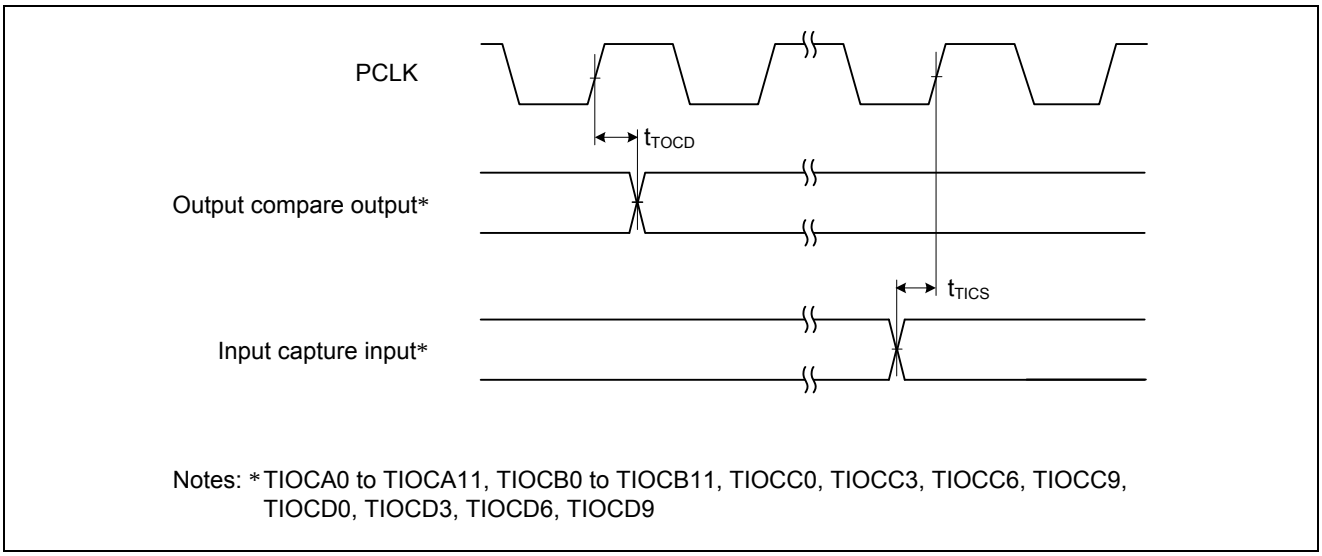


Figure 5.15 TPU Input/Output Timing

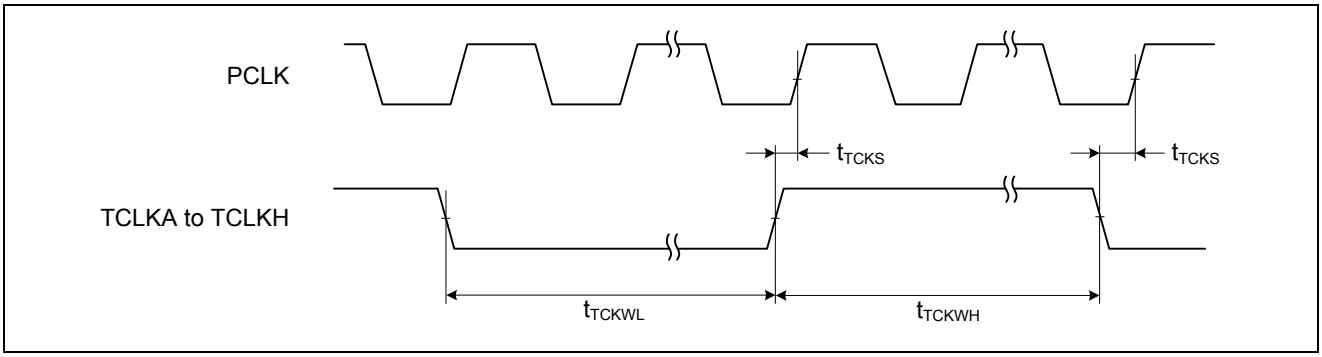


Figure 5.16 TPU Clock Input Timing

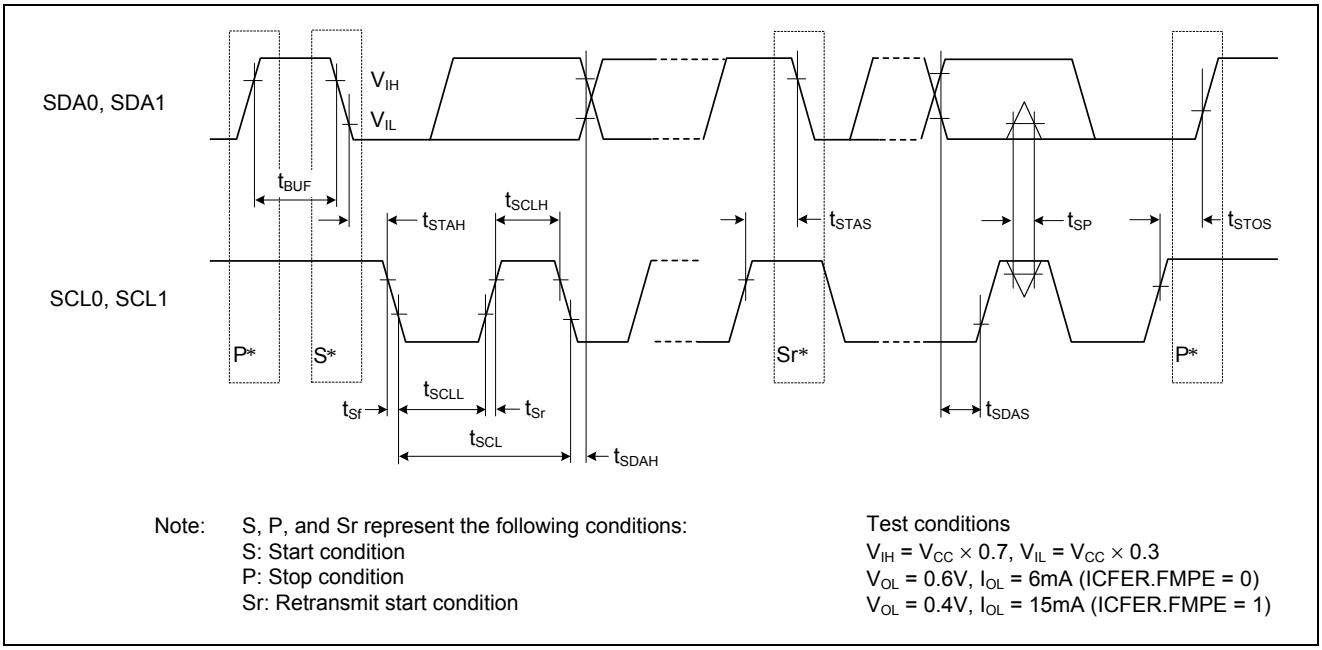


Figure 5.25 I²C Bus Interface Input/Output Timing

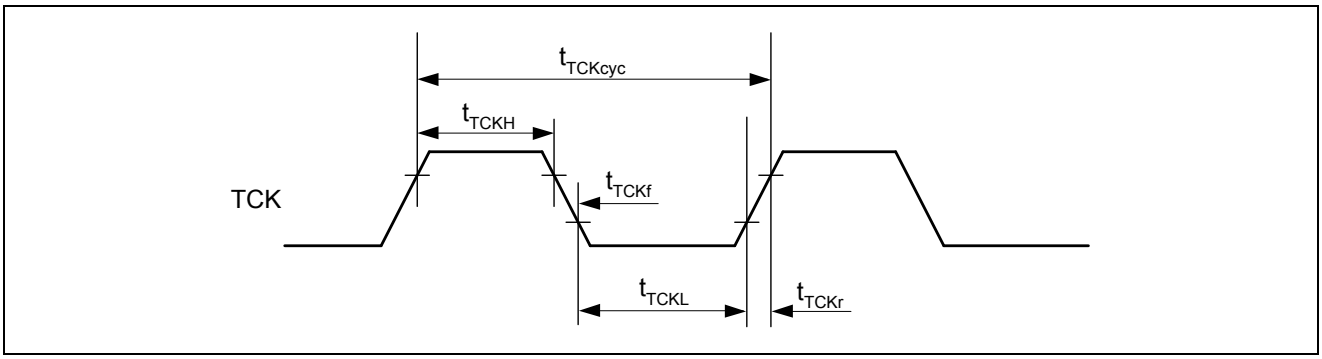


Figure 5.26 Boundary Scan TCK Timing

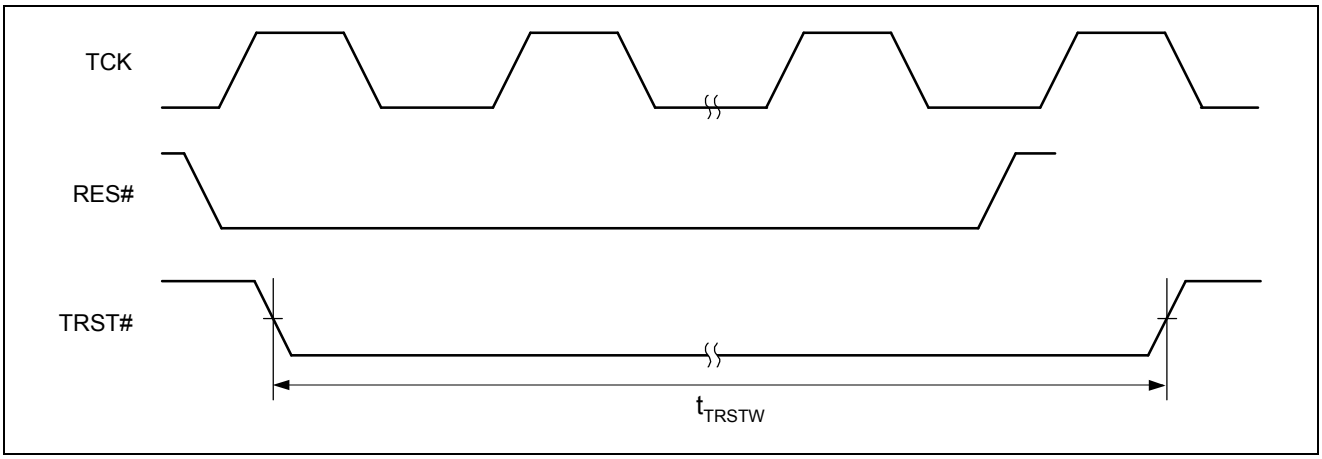


Figure 5.27 Boundary Scan TRST# Timing

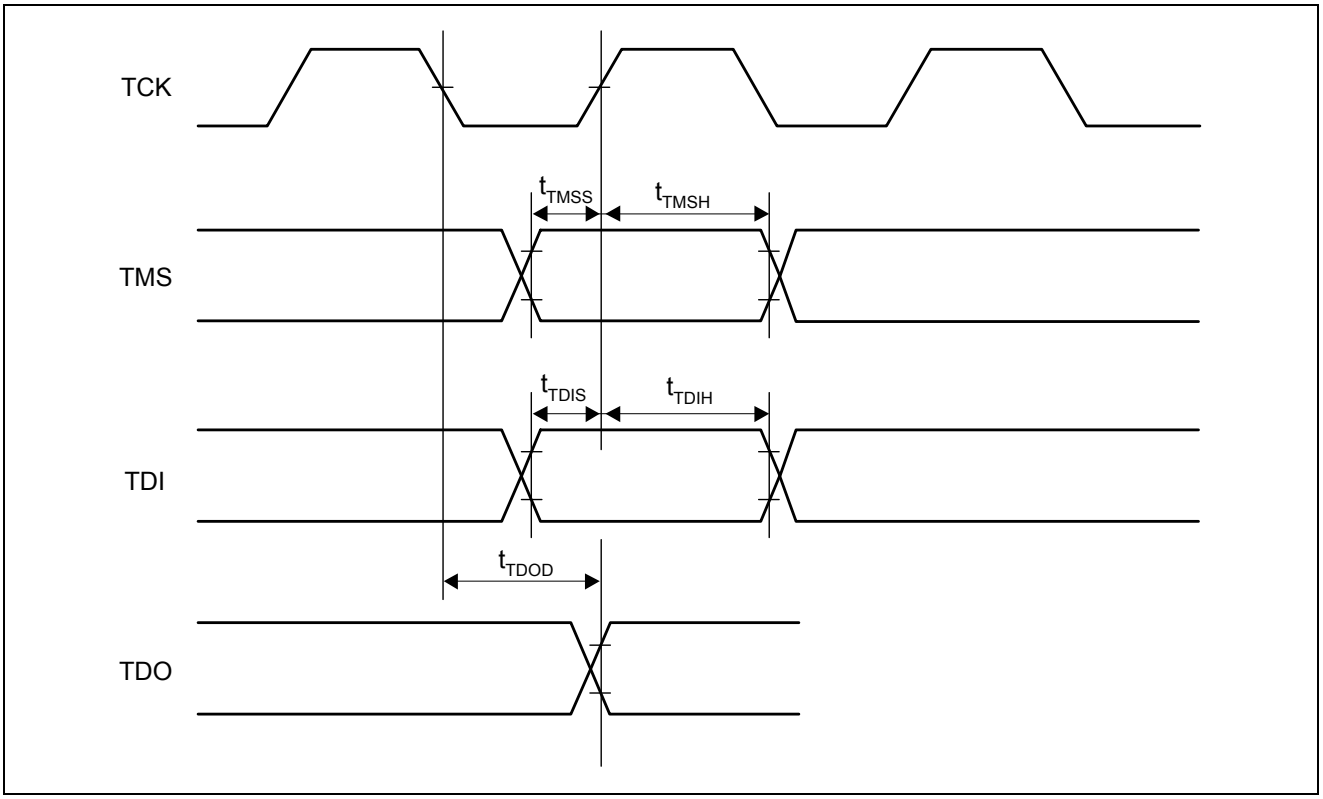


Figure 5.28 Boundary Scan Input/Output Timing

5.4 A/D Conversion Characteristics

Table 5.9 A/D Conversion Characteristics

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V, PCLK = 8 to 50 MHz, ADCLK = 4 to 50 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			10	10	10	Bit	
Conversion time*1 (ADCLK = 50-MHz operation)	With 0.1-µF external capacitor	When the capacitor is charged enough*2	0.8 (0.3)*3	—	—	µs	Sampling 15 states
	Without external capacitor	Permissible signal source impedance (max.) = 1.0 kΩ	1.0 (0.5)*3	—	—		Sampling 25 states
		Permissible signal source impedance (max.) = 5.0 kΩ	2.6 (2.1)*3	—	—		Sampling 105 states
Analog input capacitance			—	—	6.0	pF	
INL integral nonlinearity error (INL)			—	±1.5	±3.0	LSB	
Offset error			—	±1.5	±3.0	LSB	
Full-scale error			—	±1.5	±3.0	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	±1.5	±3.0	LSB	
DNL differential nonlinearity error (DNL)			—	±0.5	±1.0	LSB	

Notes: 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
2. The scanning is not supported.
3. The value in parentheses indicates the sampling time.

5.5 D/A Conversion Characteristics

Table 5.10 D/A Conversion Characteristics

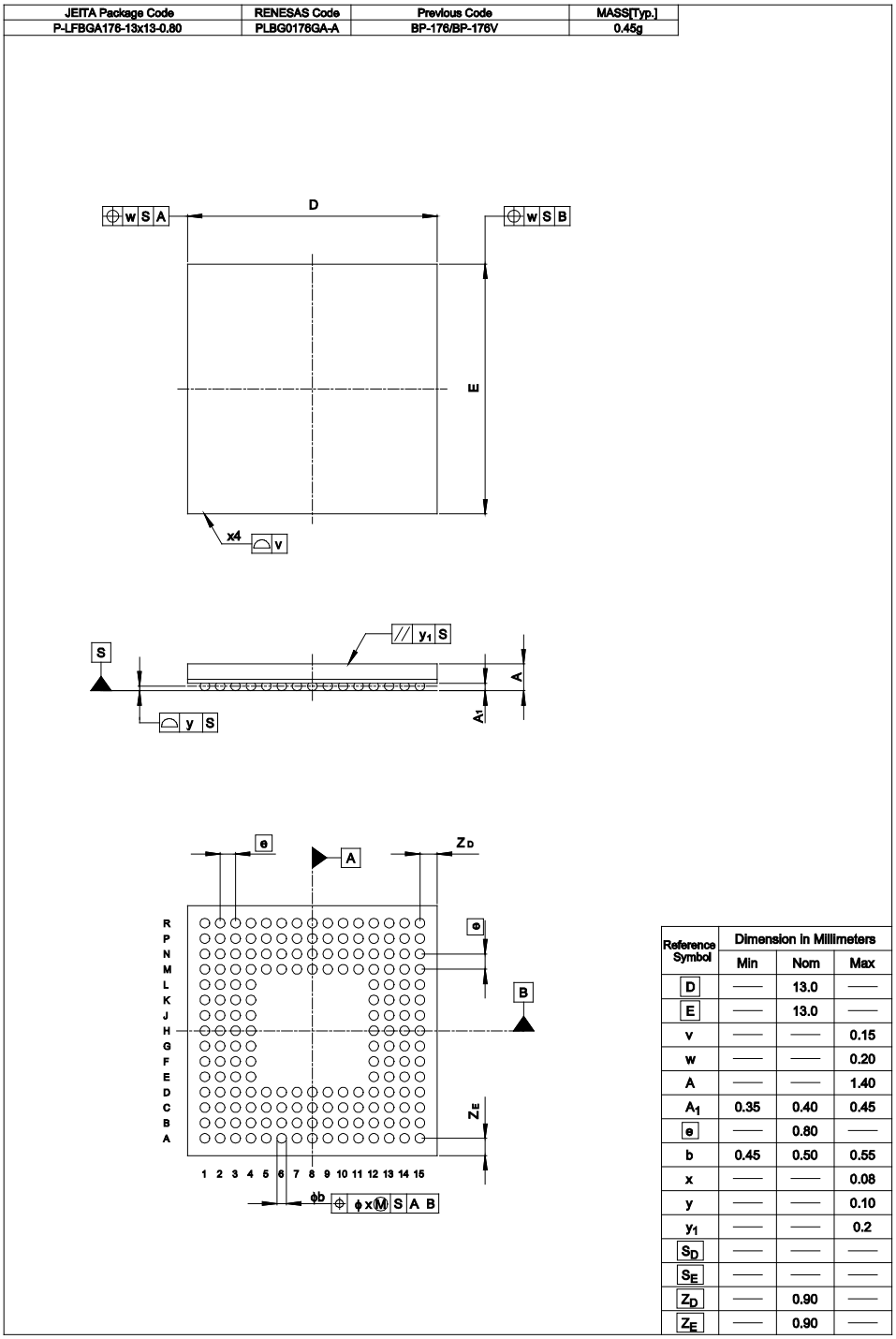
Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V, PCLK = 8 to 50 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time	—	—	3	µs	20-pF capacitive load
Absolute accuracy	—	±2.0	±4.0	LSB	2-MΩ resistive load
	—	—	±3.0	LSB	4-MΩ resistive load
	—	—	±2.0	LSB	10-MΩ resistive load
RO output resistance	—	3.6	—	kΩ	

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in "Packages" on Renesas Technology Corp. website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA176-13x13-0.80	PLBG0176GA-A	BP-176/BP-176V	0.45g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	13.0	—
E	—	13.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.90	—
Z_E	—	0.90	—

176-pin LFBGA (PLBG0176GA-A)