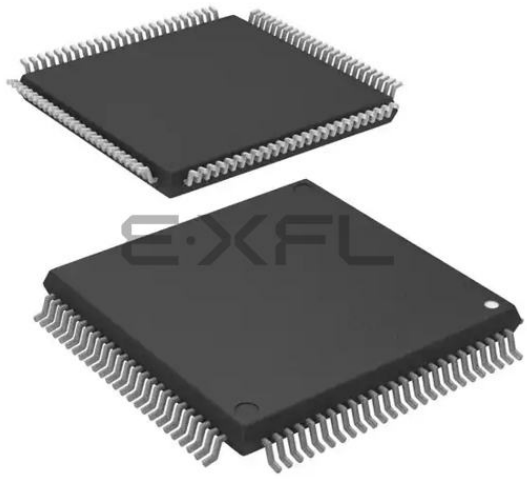
Renesas Electronics America Inc - R5F56107VDFP#V0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	117
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 2x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56107vdfp-v0

1.1.2 Outline of Specifications

Table 1.1 lists the specifications of the RX610 Group in outline.

Table 1.1 Outline of Specifications

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 100 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction in one state (in one system clock cycle) • Address space: 4-Gbyte linear address • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Nine 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point operation instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 x 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions conforming to the IEEE754 standard
Memory	Flash	• Flash capacity: 2 Mbytes (max.) • Three types of on-board programming modes SCI boot mode, user program mode, and user boot mode
	RAM	RAM capacity: 128 Kbytes
	Data flash	Data flash capacity: 32 Kbytes
MCU operating modes		Single-chip mode, on-chip ROM enabled extended mode, and on-chip ROM disabled extended mode
Clock	Clock generation circuit	• One main clock oscillation circuit • Includes a PLL circuit and frequency divider, so the operating frequency is selectable • System clock, peripheral module clock, and external bus clock are independently specifiable. The CPU, DMAC, DTC, ROM, and RAM run in synchronization with the system clock (ICLK): 8 to 100 MHz Peripheral modules run in synchronization with the peripheral module clock (PCLK): 8 to 50 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): 8 to 25 MHz
Power down	Power-down function	• Module stop function • Four power-down modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode

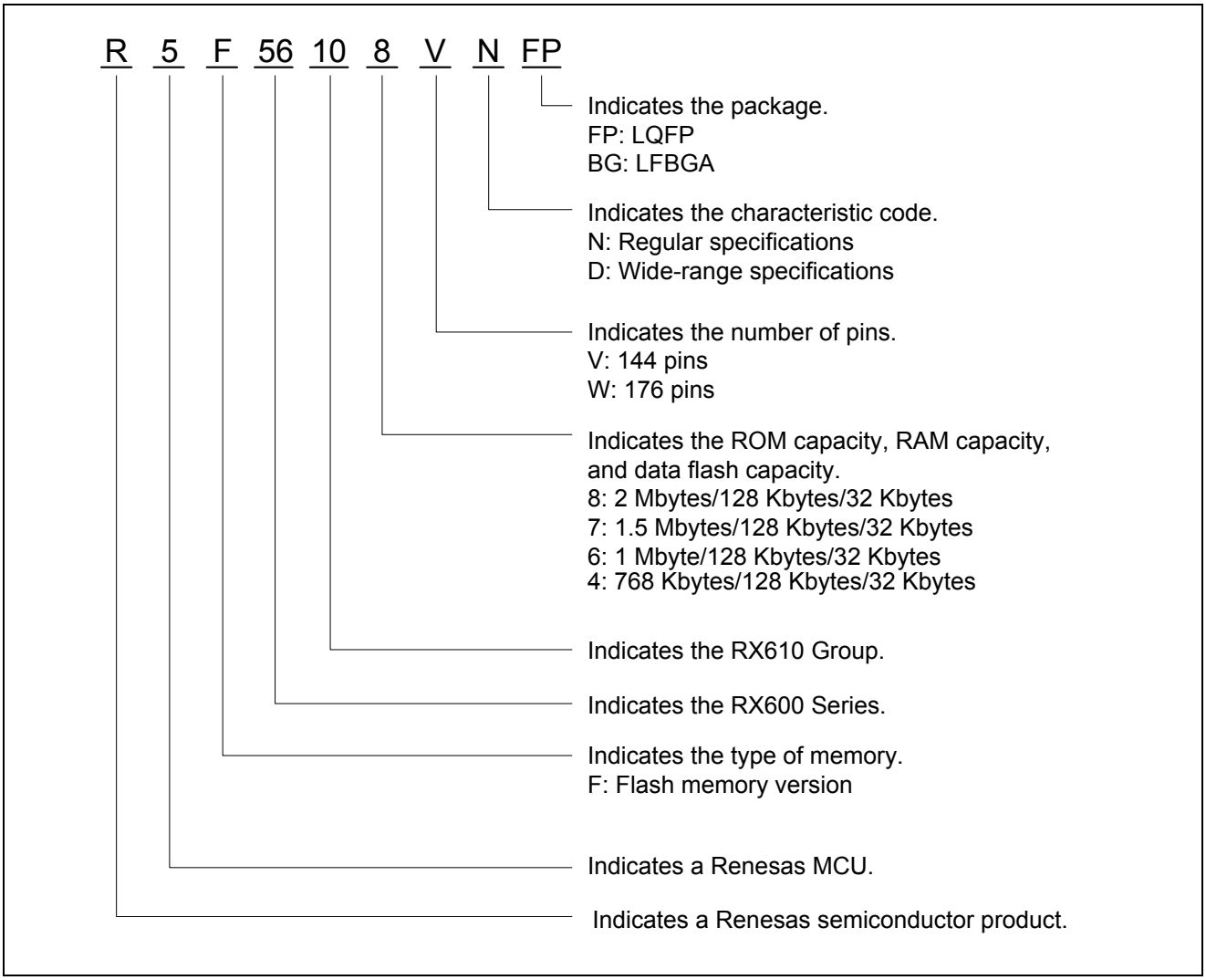
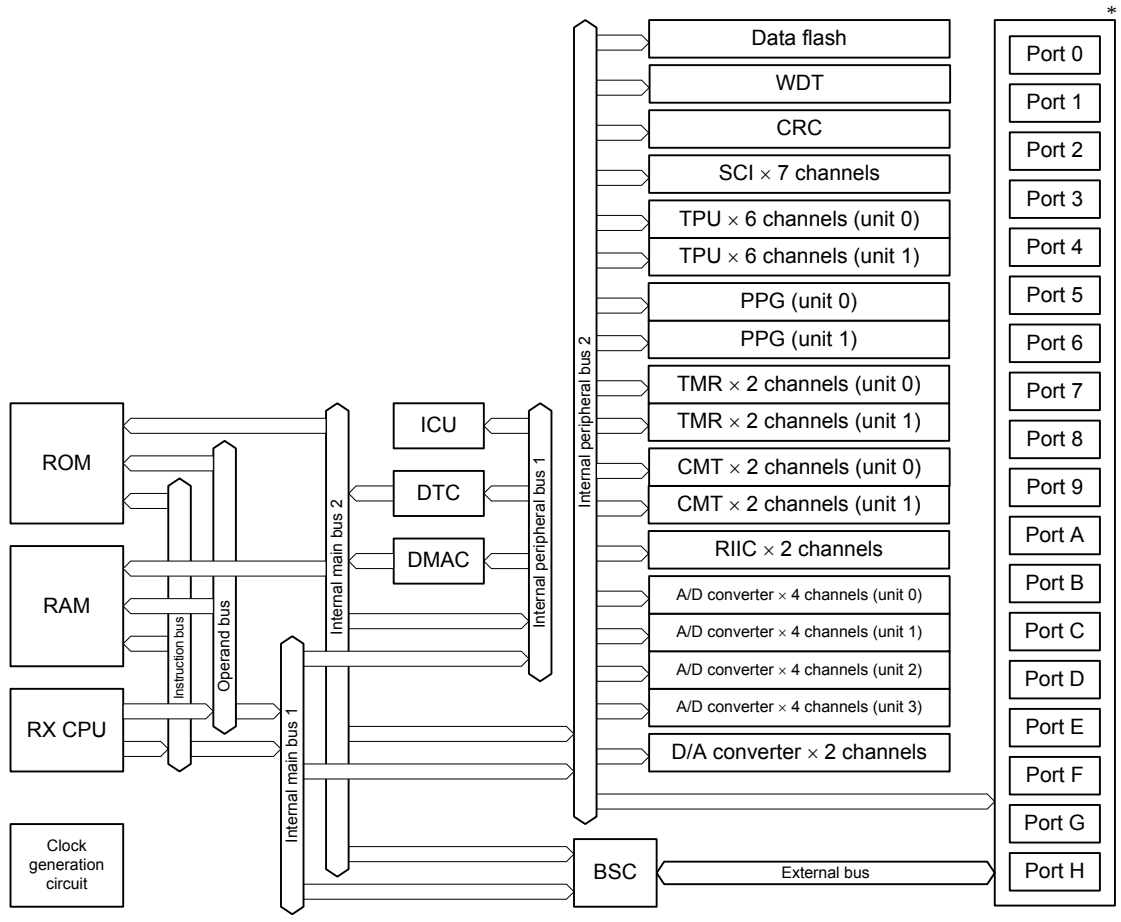


Figure 1.1 How to Read the Product Part No.

1.3 Block Diagram

Figure 1.2 shows a block diagram of the RX610 Group.



[Legend]

ICU:	Interrupt control unit	SCI:	Serial communications interfaces
DTC:	Data transfer controller	TPU:	16-bit timer pulse unit
DMAC:	DMA controller	PPG:	Programmable pulse generator
BSC:	Bus controller	TMR:	8-bit timer
WDT:	Watchdog timer	CMT:	Compare match timer
CRC:	CRC (Cyclic Redundancy Check) calculator	RIIC:	I^2C bus interface

Note: * Ports F and H are not included in the 144-pin LQFP package.

Figure 1.2 Block Diagram

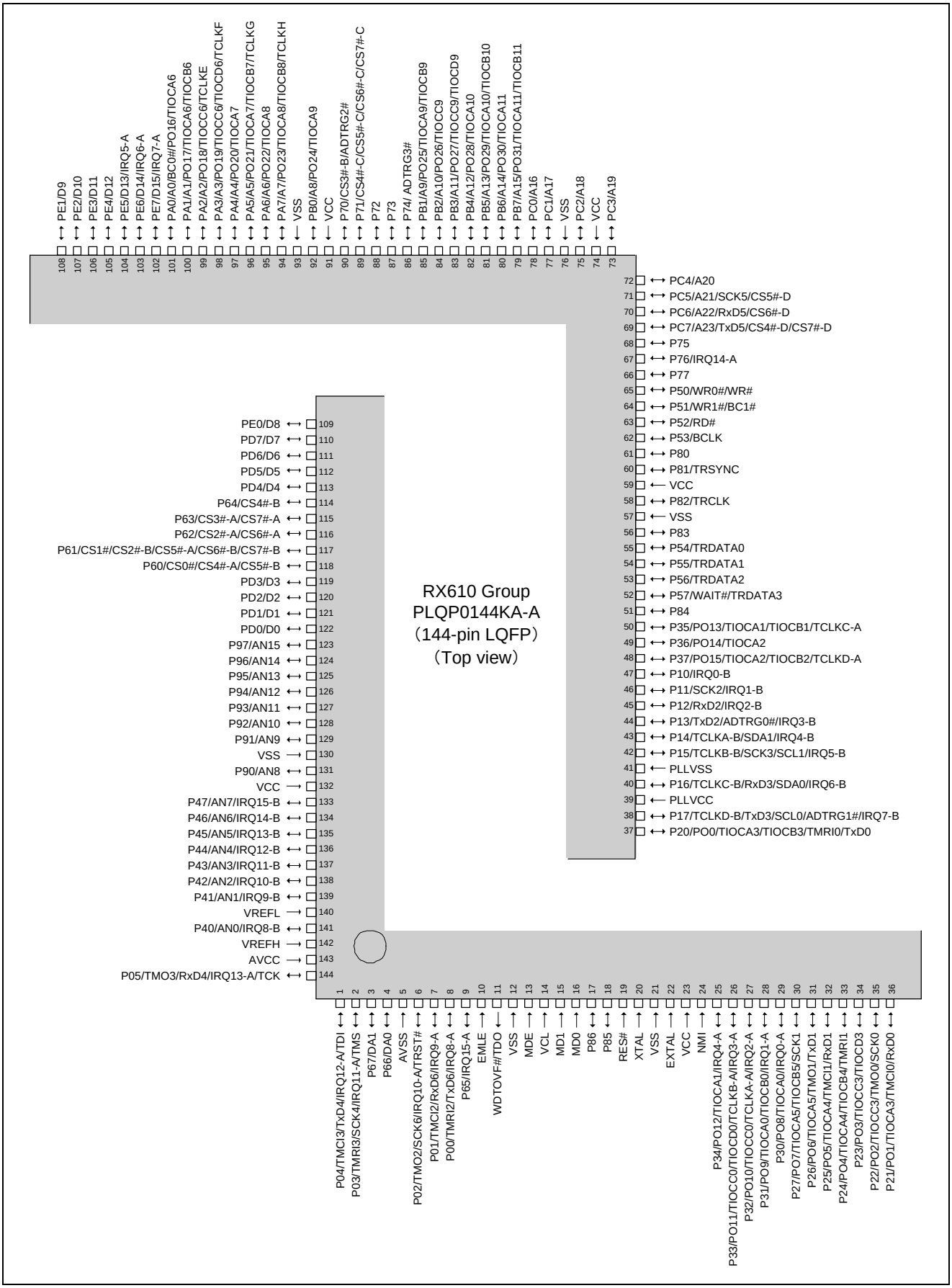


Figure 1.5 Pin Assignment (Assistance Diagram) of the 144-Pin LQFP

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
M6		P37			PO15/ TIOCA2/ TIOCB2/ TCLKD-A			
M7		P57		WAIT#				TRDATA3
M8		P83						
M9		P81						TRSYNC
M10		P51		WR1#/BC1#				
M11		PH4						
M12		PC7		A23/ CS4#-D/ CS7#-D		TxD5		
M13	VSS							
M14		PC0		A16				
M15		PB6		A14	PO30/ TIOCA11			
N1		P25			PO5/ TIOCA4/ TMCI1	RxD1		
N2		P24			PO4/ TIOCA4/ TIOCB4/ TMRI1			
N3		P20			PO0/ TIOCA3/ TIOCB3/ TMRI0	TxD0		
N4		P16	IRQ6-B		TCLKC-B	RxD3/SDA0		
N5		P12	IRQ2-B			RxD2		
N6		P36			PO14/ TIOCA2			
N7		P56						TRDATA2
N8	VSS							
N9		P80						
N10		P50		WR0#/WR#				
N11	VSS							
N12		P76	IRQ14-A					
N13		PH2						
N14		PC2		A18				
N15		PC1		A17				
P1		P23			PO3/ TIOCC3/ TIOCD3			

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
32		P25			PO5/ TIOCA4/ TMCI1	RxD1		
33		P24			PO4/ TIOCA4/ TIOCB4/ TMRI1			
34		P23			PO3/ TIOCC3/ TIOCD3			
35		P22			PO2/ TIOCC3/ TMO0	SCK0		
36		P21			PO1/ TIOCA3/ TMCI0	RxD0		
37		P20			PO0/ TIOCA3/ TIOCB3/ TMRI0	TxD0		
38		P17	IRQ7-B		TCLKD-B	TxD3/SCL0	ADTRG1#	
39	PLLVCC							
40		P16	IRQ6-B		TCLKC-B	RxD3/SDA0		
41	PLLVSS							
42		P15	IRQ5-B		TCLKB-B	SCK3/SCL1		
43		P14	IRQ4-B		TCLKA-B	SDA1		
44		P13	IRQ3-B			TxD2	ADTRG0#	
45		P12	IRQ2-B			RxD2		
46		P11	IRQ1-B			SCK2		
47		P10	IRQ0-B					
48		P37			PO15/ TIOCA2/ TIOCB2/ TCLKD-A			
49		P36			PO14/ TIOCA2			
50		P35			PO13/ TIOCA1/ TIOCB1/ TCLKC-A			
51		P84						
52		P57		WAIT#				TRDATA3
53		P56						TRDATA2
54		P55						TRDATA1

2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

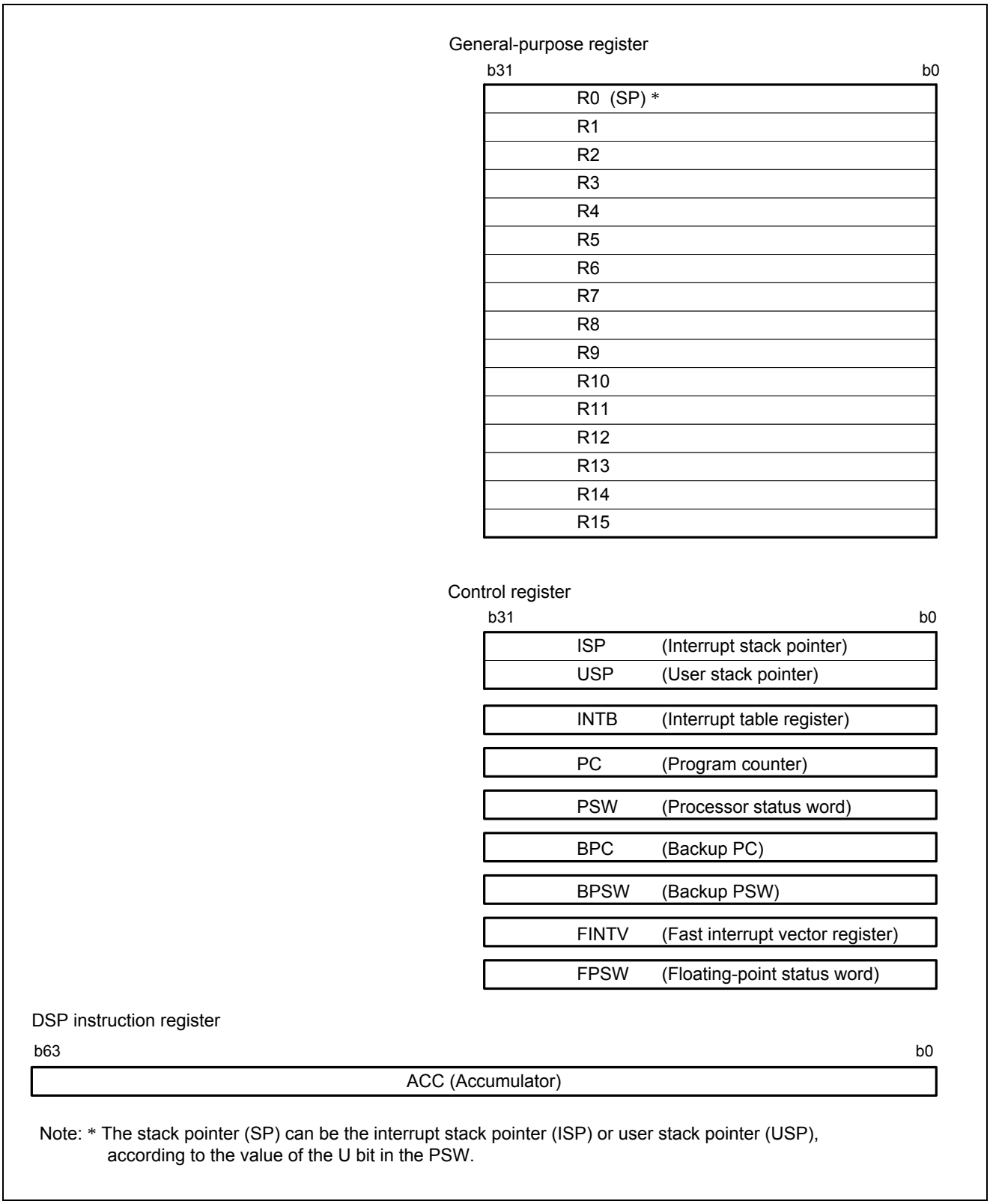


Figure 2.1 Register Set of the CPU

(8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.

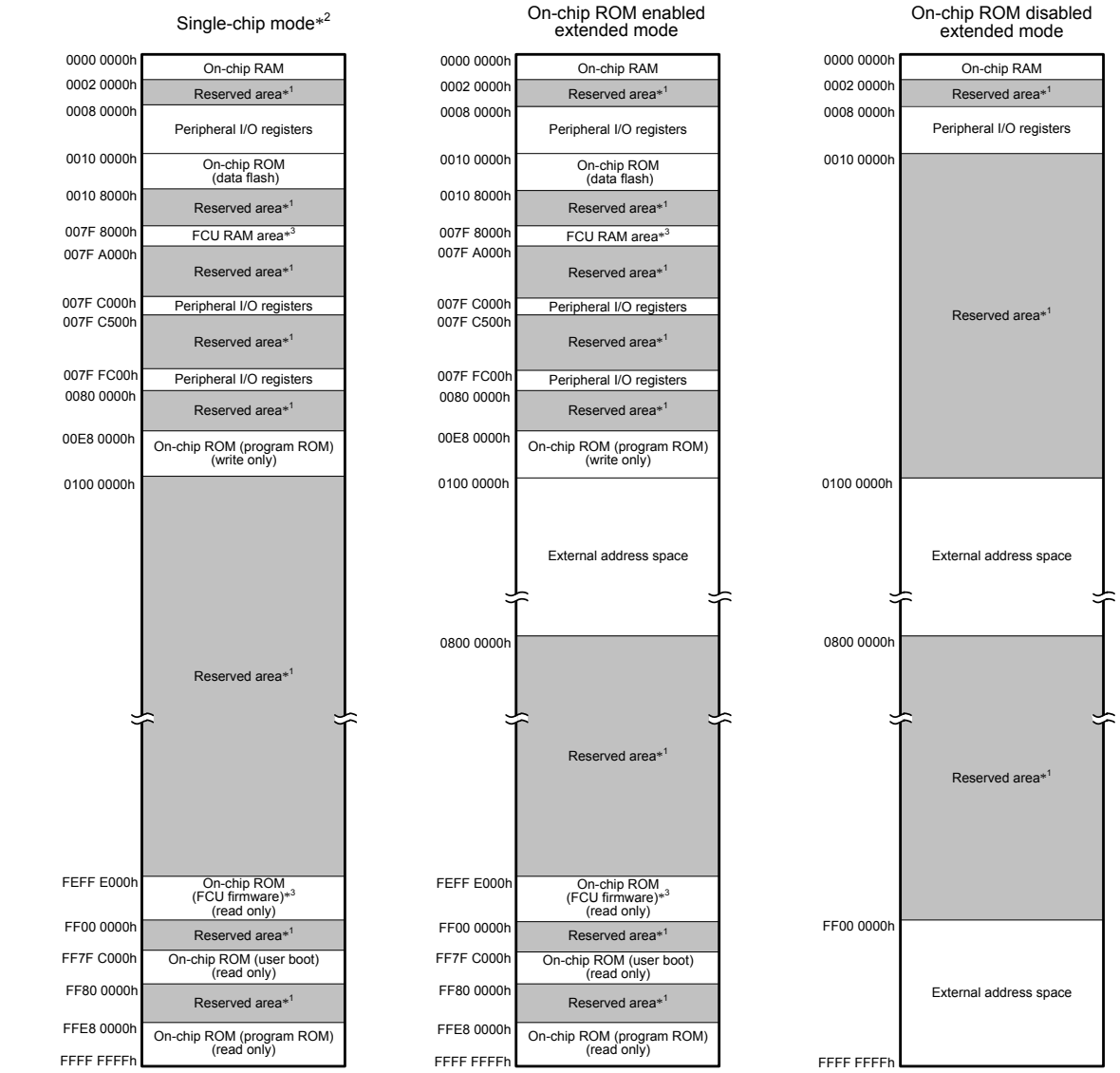
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the corresponding Cj flag indicates the source of the exception within the exception handling routine. If the exception handling is masked (Ej = 0), check the Fj flag at the end of a series of processing whether an exception is generated or not. The Fj flag is the accumulation type flag (j = X, U, Z, O, or V).

(9) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.



Notes: 1. A reserved area should not be accessed.
2. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
3. For details on the FCU, see section 26, ROM (Flash Memory for Code Storage) and section 27, Data Flash (Flash Memory for Data Storage) in the User's manual: Hardware.

Figure 3.2 Memory Map of the R5F56107

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7170h	ICU	Interrupt request destination setting register 112	ISELR112	8	8	2 ICLK
0008 7175h	ICU	Interrupt request destination setting register 117	ISELR117	8	8	2 ICLK
0008 7176h	ICU	Interrupt request destination setting register 118	ISELR118	8	8	2 ICLK
0008 717Ah	ICU	Interrupt request destination setting register 122	ISELR122	8	8	2 ICLK
0008 717Bh	ICU	Interrupt request destination setting register 123	ISELR123	8	8	2 ICLK
0008 717Ch	ICU	Interrupt request destination setting register 124	ISELR124	8	8	2 ICLK
0008 717Dh	ICU	Interrupt request destination setting register 125	ISELR125	8	8	2 ICLK
0008 717Fh	ICU	Interrupt request destination setting register 127	ISELR127	8	8	2 ICLK
0008 7180h	ICU	Interrupt request destination setting register 128	ISELR128	8	8	2 ICLK
0008 7185h	ICU	Interrupt request destination setting register 133	ISELR133	8	8	2 ICLK
0008 7186h	ICU	Interrupt request destination setting register 134	ISELR134	8	8	2 ICLK
0008 718Ah	ICU	Interrupt request destination setting register 138	ISELR138	8	8	2 ICLK
0008 718Bh	ICU	Interrupt request destination setting register 139	ISELR139	8	8	2 ICLK
0008 718Ch	ICU	Interrupt request destination setting register 140	ISELR140	8	8	2 ICLK
0008 718Dh	ICU	Interrupt request destination setting register 141	ISELR141	8	8	2 ICLK
0008 7191h	ICU	Interrupt request destination setting register 145	ISELR145	8	8	2 ICLK
0008 7192h	ICU	Interrupt request destination setting register 146	ISELR146	8	8	2 ICLK
0008 7197h	ICU	Interrupt request destination setting register 151	ISELR151	8	8	2 ICLK
0008 7198h	ICU	Interrupt request destination setting register 152	ISELR152	8	8	2 ICLK
0008 719Ch	ICU	Interrupt request destination setting register 156	ISELR156	8	8	2 ICLK
0008 719Dh	ICU	Interrupt request destination setting register 157	ISELR157	8	8	2 ICLK
0008 719Eh	ICU	Interrupt request destination setting register 158	ISELR158	8	8	2 ICLK
0008 719Fh	ICU	Interrupt request destination setting register 159	ISELR159	8	8	2 ICLK
0008 71A1h	ICU	Interrupt request destination setting register 161	ISELR161	8	8	2 ICLK
0008 71A2h	ICU	Interrupt request destination setting register 162	ISELR162	8	8	2 ICLK
0008 71A7h	ICU	Interrupt request destination setting register 167	ISELR167	8	8	2 ICLK
0008 71A8h	ICU	Interrupt request destination setting register 168	ISELR168	8	8	2 ICLK
0008 71AEh	ICU	Interrupt request destination setting register 174	ISELR174	8	8	2 ICLK
0008 71AFh	ICU	Interrupt request destination setting register 175	ISELR175	8	8	2 ICLK
0008 71B1h	ICU	Interrupt request destination setting register 177	ISELR177	8	8	2 ICLK
0008 71B2h	ICU	Interrupt request destination setting register 178	ISELR178	8	8	2 ICLK
0008 71B4h	ICU	Interrupt request destination setting register 180	ISELR180	8	8	2 ICLK
0008 71B5h	ICU	Interrupt request destination setting register 181	ISELR181	8	8	2 ICLK
0008 71B7h	ICU	Interrupt request destination setting register 183	ISELR183	8	8	2 ICLK
0008 71B8h	ICU	Interrupt request destination setting register 184	ISELR184	8	8	2 ICLK
0008 71C6h	ICU	Interrupt request destination setting register 198	ISELR198	8	8	2 ICLK
0008 71C7h	ICU	Interrupt request destination setting register 199	ISELR199	8	8	2 ICLK
0008 71C8h	ICU	Interrupt request destination setting register 200	ISELR200	8	8	2 ICLK
0008 71C9h	ICU	Interrupt request destination setting register 201	ISELR201	8	8	2 ICLK
0008 71D7h	ICU	Interrupt request destination setting register 215	ISELR215	8	8	2 ICLK
0008 71D8h	ICU	Interrupt request destination setting register 216	ISELR216	8	8	2 ICLK
0008 71DBh	ICU	Interrupt request destination setting register 219	ISELR219	8	8	2 ICLK
0008 71DCh	ICU	Interrupt request destination setting register 220	ISELR220	8	8	2 ICLK
0008 71DFh	ICU	Interrupt request destination setting register 223	ISELR223	8	8	2 ICLK
0008 71E0h	ICU	Interrupt request destination setting register 224	ISELR224	8	8	2 ICLK

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C329h	ICU	IRQ control register 9	IRQCR9	8	8	2 to 3 PCLK *7
0008 C32Ah	ICU	IRQ control register 10	IRQCR10	8	8	2 to 3 PCLK *7
0008 C32Bh	ICU	IRQ control register 11	IRQCR11	8	8	2 to 3 PCLK *7
0008 C32Ch	ICU	IRQ control register 12	IRQCR12	8	8	2 to 3 PCLK *7
0008 C32Dh	ICU	IRQ control register 13	IRQCR13	8	8	2 to 3 PCLK *7
0008 C32Eh	ICU	IRQ control register 14	IRQCR14	8	8	2 to 3 PCLK *7
0008 C32Fh	ICU	IRQ control register 15	IRQCR15	8	8	2 to 3 PCLK *7
0008 C340h	ICU	Software standby release IRQ enable register	SSIER	16	16	2 to 3 PCLK *7
0008 C350h	ICU	Non-maskable interrupt enable register	NMIER	8	8	2 to 3 PCLK *7
0008 C351h	ICU	NMI pin interrupt control register	NMICR	8	8	2 to 3 PCLK *7
0008 C352h	ICU	Non-maskable interrupt status register	NMISR	8	8	2 to 3 PCLK *7
0008 C353h	ICU	Non-maskable interrupt clear register	NMICLR	8	8	2 to 3 PCLK *7
007F C402h	FLASH	Flash mode register	FMODR	8	8	2 to 3 PCLK *7
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2 to 3 PCLK *7
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2 to 3 PCLK *7
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2 to 3 PCLK *7
007F C440h	FLASH	Data flash read enable register	DFLRE	16	16	2 to 3 PCLK *7
007F C450h	FLASH	Data flash programming/erasure enable register	DFLWE	16	16	2 to 3 PCLK *7
007F C454h	FLASH	FCU RAM enable register	FCURAME	16	16	2 to 3 PCLK *7
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2 to 3 PCLK *7
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2 to 3 PCLK *7
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2 to 3 PCLK *7
007F FFB4h	FLASH	Flash protection register	FPROTR	16	16	2 to 3 PCLK *7
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2 to 3 PCLK *7
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2 to 3 PCLK *7
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2 to 3 PCLK *7
007F FFCAh	FLASH	Data flash blank check control register	DFLBCCNT	16	16	2 to 3 PCLK *7
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2 to 3 PCLK *7
007F FFCEh	FLASH	Data flash blank check status register	DFLBCSTAT	16	16	2 to 3 PCLK *7
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2 to 3 PCLK *7

Notes:
1. When the same output trigger is specified for pulse output groups 2 and 3 by the PPG0.PCR setting, the PPG0.NDRH address is 000881ECh. When different output triggers are specified, the PPG0.NDRH addresses for pulse output groups 2 and 3 are 000881EEh and 000881ECh, respectively.
2. When the same output trigger is specified for pulse output groups 0 and 1 by the PPG0.PCR setting, the PPG0.NDRL address is 000881EDh. When different output triggers are specified, the PPG0.NDRL addresses for pulse output groups 0 and 1 are 000881EFh and 000881EDh, respectively.
3. When the same output trigger is specified for pulse output groups 6 and 7 by the PPG1.PCR setting, the PPG1.NDRH address is 000881FCh. When different output triggers are specified, the PPG1.NDRH addresses for pulse output groups 6 and 7 are 000881FEh and 000881FCh, respectively.
4. When the same output trigger is specified for pulse output groups 4 and 5 by the PPG1.PCR setting, the PPG1.NDRL address is 000881FDh. When different output triggers are specified, the PPG1.NDRL addresses for pulse output groups 4 and 5 are 000881FFh and 000881FDh, respectively.
5. 16-bit access to odd addresses is prohibited. When 16-bit access is required, access is at the address corresponding to TMR0 or TMR2.
6. For certain bits, functions differ according to whether the mode is serial communications or smart card interface.
7. The number of access cycles varies depending on the number of divided cycles for clock synchronization (0 to one PCLK).
8. The number of access cycles may be 5 ICLK if the register is accessed during the DMAC operation.

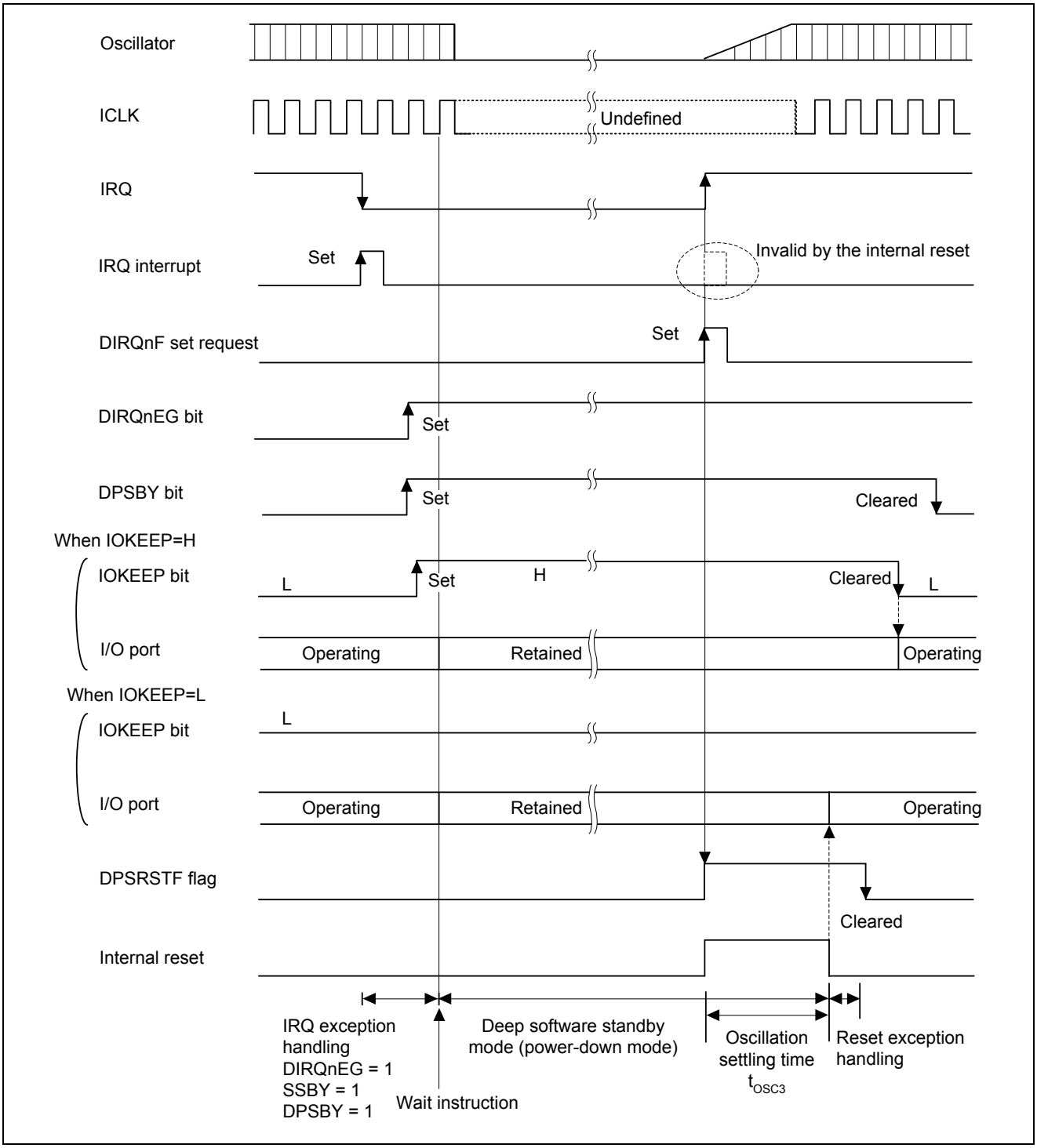


Figure 5.3 Oscillation Settling Timing after Deep Software Standby Mode

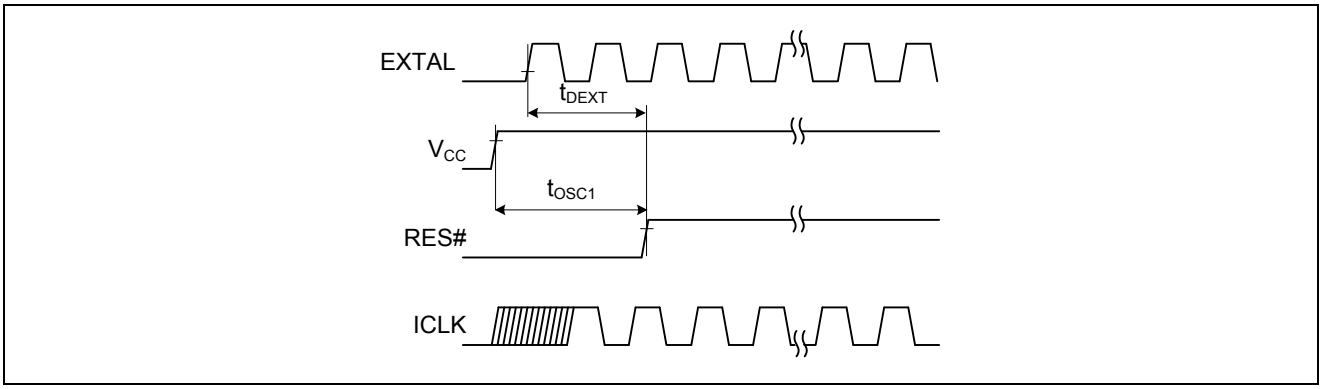


Figure 5.4 Oscillation Settling Timing

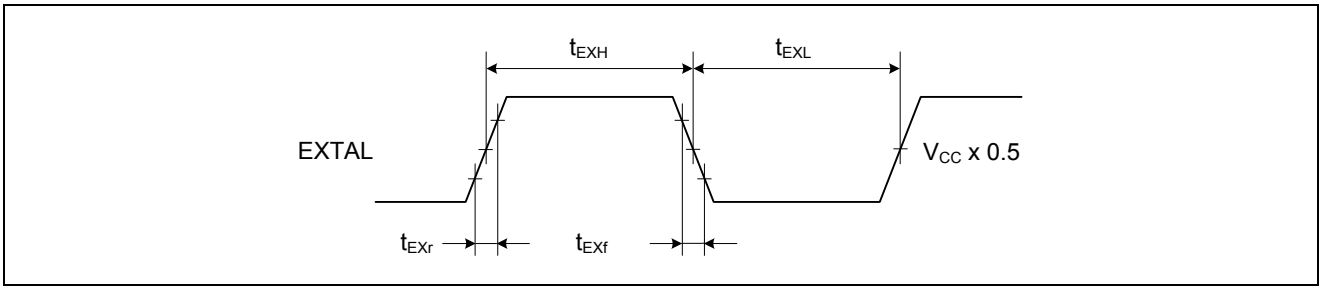


Figure 5.5 External Input Clock Timing

5.3.2 Control Signal Timing

Table 5.6 Control Signal Timing

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V
ICLK = 8 to 100 MHz, BCLK = 8 to 25 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item	Symbol	Min.	Max.	Unit	Test Conditions
RES# pulse width (except for ROM, data flash programming/erasure)	t_{RESW}*1	20	—	t_{cyc}	Figure 5.6
		1.5	—	μs	
Internal reset time (during ROM, data flash programming/erasure)	t_{RESW2} *2	35	—	μs	
NMI pulse width	t_{NMIW}	200	—	ns	Figure 5.7
IRQ pulse width	t_{IRQW}	200	—	ns	Figure 5.8

Notes: 1. Both the time and the number of cycles should satisfy the specifications.
2. This is to specify the FCU reset and the WDT reset.

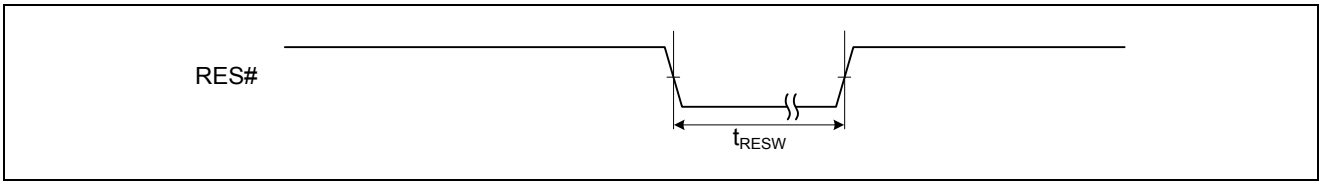


Figure 5.6 Reset Input Timing

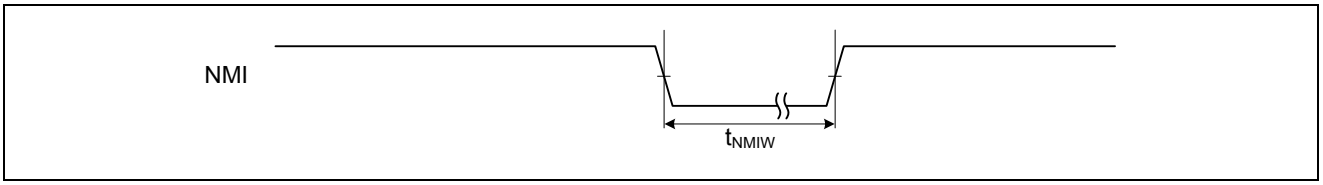


Figure 5.7 NMI Interrupt Input Timing

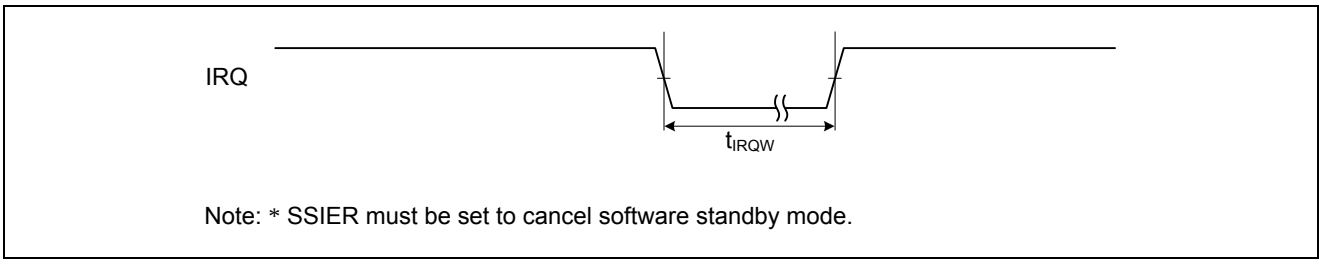
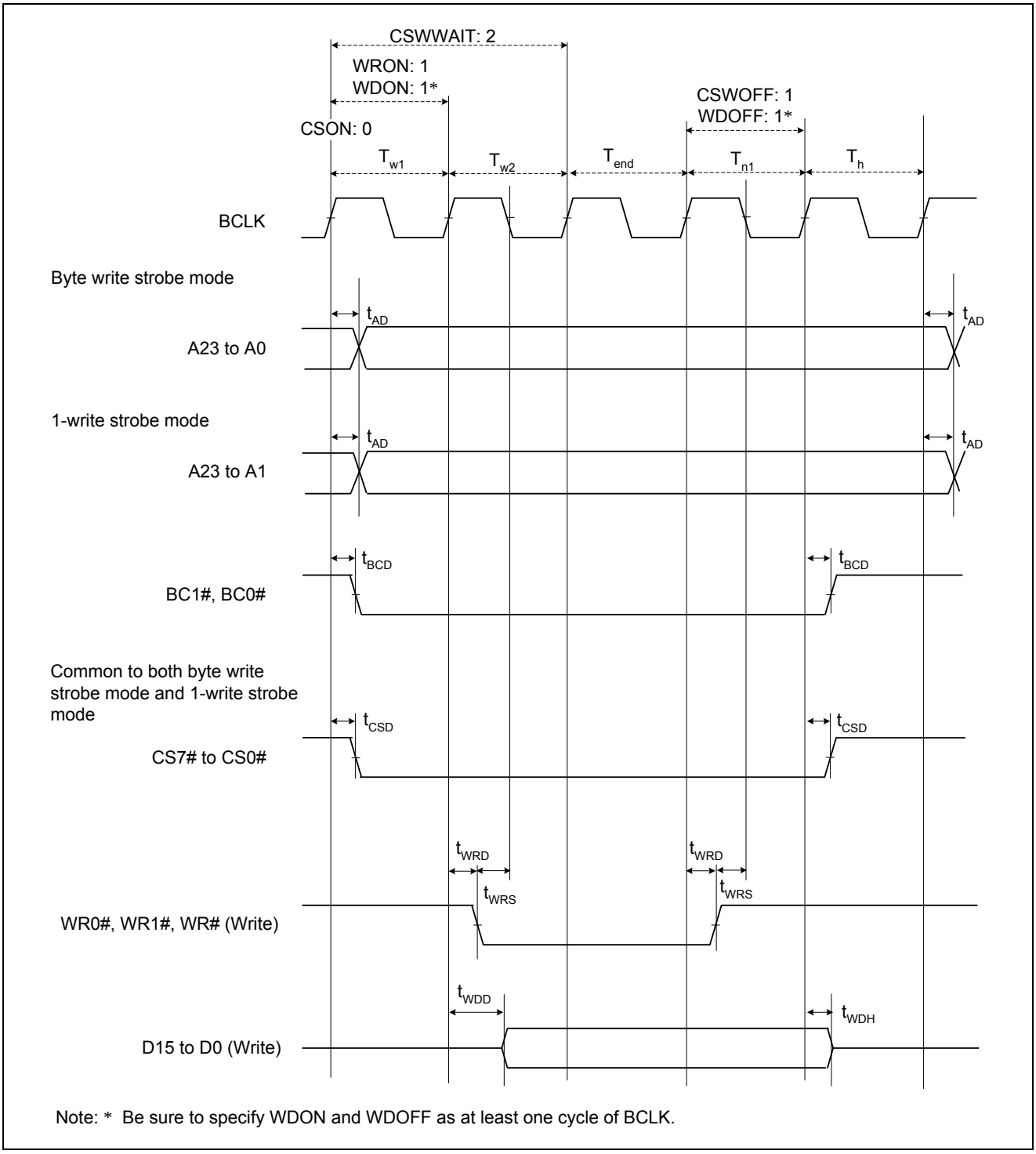


Figure 5.8 IRQ Interrupt Input Timing



Note: * Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 5.10 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

5.3.4 Timing of On-Chip Peripheral Modules

Table 5.8 Timing of On-Chip Peripheral Modules (1)

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V, PCLK = 8 to 50 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)
Output load conditions: V_{OH} = V_{CC} x 0.5, V_{OL} = V_{CC} x 0.5, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item			Symbol	Min.	Max.	Unit	Test Conditions
I/O ports	Output data delay time		t_{PWD}	—	40	ns	Figure 5.14
	Input data setup time		t_{PRS}	25	—	ns	
	Input data hold time		t_{PRH}	25	—	ns	
TPU	Timer output delay time		t_{TOCD}	—	40	ns	Figure 5.15
	Timer input setup time		t_{TICS}	25	—	ns	
	Timer clock input setup time		t_{TCKS}	25	—	ns	Figure 5.16
	Timer clock pulse width	Single-edge setting	t_{TCKWH}	1.5 x (1/PCLK)	—	t_{cyc}	
		Both-edge setting	t_{TCKWL}	2.5 x (1/PCLK)	—	t_{cyc}	
PPG	Pulse output delay time		t_{POD}	—	40	ns	Figure 5.17
8-bit timer	Timer output delay time		t_{TMOD}	—	40	ns	Figure 5.18
	Timer reset input setup time		t_{TMRS}	25	—	ns	Figure 5.19
	Timer clock input setup time		t_{TMCS}	25	—	ns	Figure 5.20
	Timer clock pulse width	Single-edge setting	t_{TMCWH}	1.5 x (1/PCLK)	—	t_{cyc}	
		Both-edge setting	t_{TMCWL}	2.5 x (1/PCLK)	—	t_{cyc}	
WDT	Overflow output delay time		t_{WOVD}	—	40	ns	Figure 5.21
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4 x (1/PCLK)	—	t_{cyc}	Figure 5.22
		Clock synchronous		6 x (1/PCLK)	—		
	Input clock pulse width		t_{SCKW}	0.4 x t_{Scyc}	0.6 x t_{Scyc}	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	20	ns	
	Input clock fall time		t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	4 x (1/PCLK)	—	t_{cyc}	
		Clock synchronous		6 x (1/PCLK)	—		
	Output clock pulse width		t_{SCKW}	0.4 x t_{Scyc}	0.6 x t_{Scyc}	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	20	ns	
	Output clock fall time		t_{SCKf}	—	20	ns	
	Transmit data delay time		t_{TXD}	—	40	ns	Figure 5.23
	Receive data setup time (clock synchronous)		t_{RXS}	40	—	ns	
	Receive data hold time (clock synchronous)		t_{RXH}	40	—	ns	
A/D converter	Trigger input setup time		t_{TRGS}	25	—	ns	Figure 5.24

Table 5.8 Timing of On-Chip Peripheral Modules (3)

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V,
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item		Symbol	Min. *1*2	Max.	Unit	Test Conditions
RIIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	8(10) x (1/PCLK) + 240	—	ns	Figure 5.25
	SCL input high pulse width	t_{SCLH}	3(5) x (1/PCLK) + 120	—	ns	
	SCL input low pulse width	t_{SCLL}	5 x (1/PCLK) + 120	—	ns	
	SCL, SDA input rising time	t_{Sr}	—	120	ns	
	SCL, SDA input falling time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 x (1/PCLK)	ns	
	SDA input bus free time	t_{BUF}	5 x (1/PCLK) + 120	—	ns	
	Start condition input hold time	t_{STAH}	3(5) x (1/PCLK) + 120	—	ns	
	Re-start condition input setup time	t_{STAS}	5 x (1/PCLK) + 120	—	ns	
	Stop condition input setup time	t_{STOS}	3(5) x (1/PCLK) + 120	—	ns	
	Data input setup time	t_{SDAS}	50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	550	pF	
Boundary scan (176-pin LFBGA)	TCK clock cycle time	tTCKcyc	100	—	ns	Figure 5.26
	TCK clock high level pulse width	tTCKH	45	—	ns	
	TCK clock low level pulse width	tTCKL	45	—	ns	
	TCK clock rising time	tTCKr	—	5	ns	
	TCK clock falling time	tTCKf	—	5	ns	
	TRST# pulse width	tTRSTW	20	—	Tcyc	Figure 5.27
	TMS setup time	tTMSS	20	—	ns	Figure 5.28
	TMS hold time	tTMSH	20	—	ns	
	TDI setup time	tTDIS	20	—	ns	
	TDI hold time	tTDIH	20	—	ns	
	TDO data delay time	tTDOD	—	40	ns	

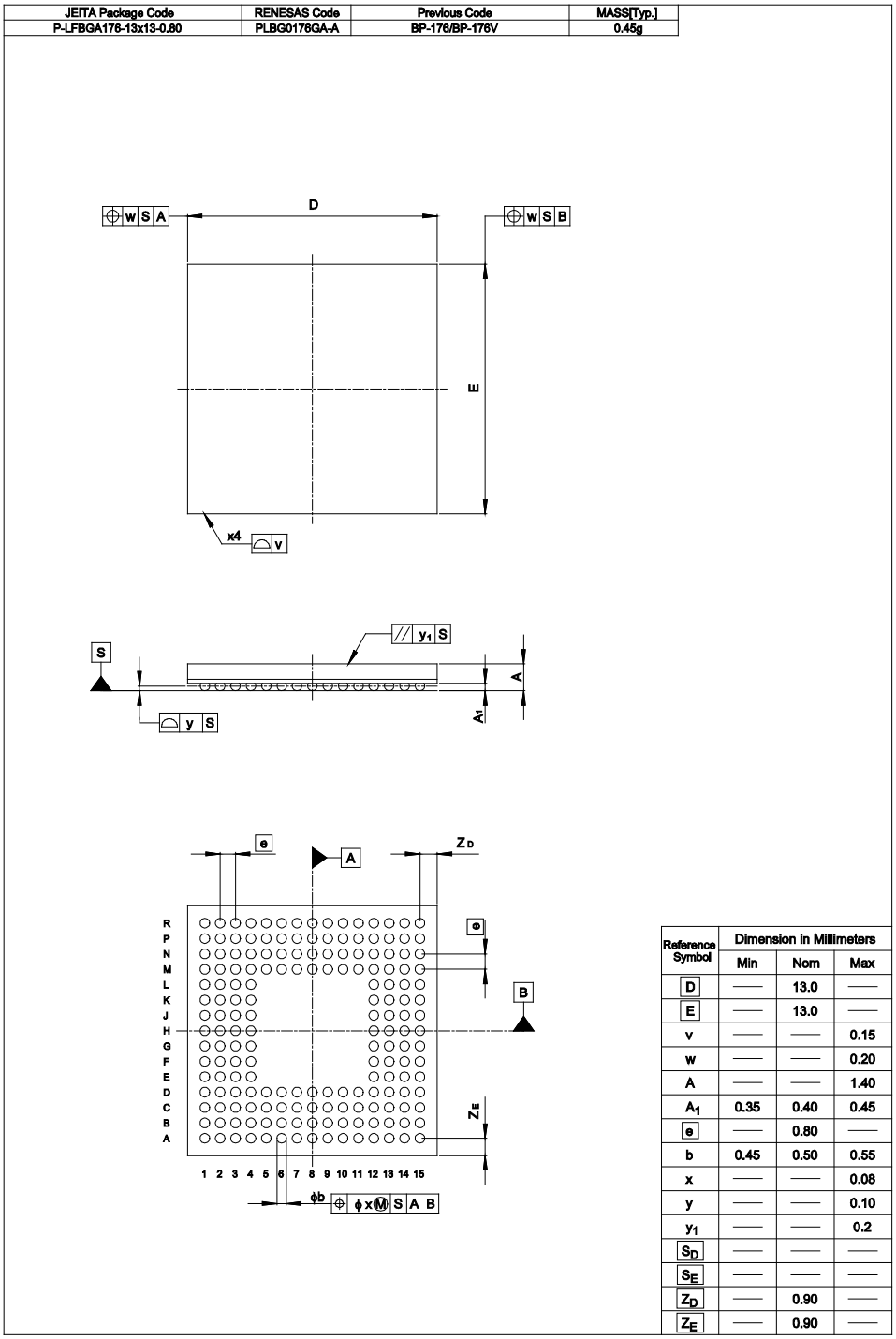
Notes:1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.

2. Cb indicates the total capacity of the bus line.

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in "Packages" on Renesas Technology Corp. website.

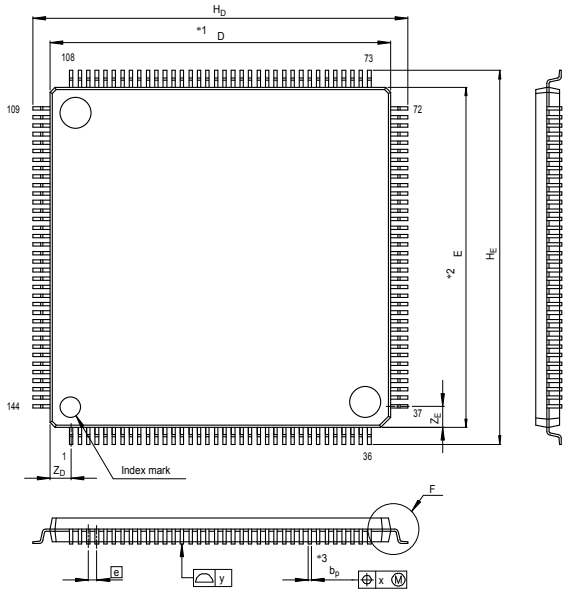
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA176-13x13-0.80	PLBG0176GA-A	BP-176/BP-176V	0.45g

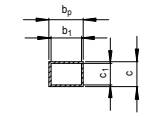


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	13.0	—
E	—	13.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.90	—
Z_E	—	0.90	—

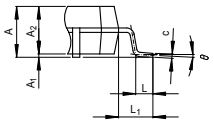
176-pin LFBGA (PLBG0176GA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

144-pin LQFP (PLQP0144KA-A)

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.