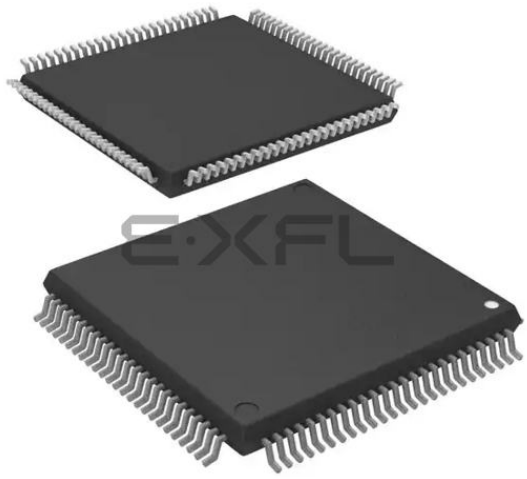

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	117
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 2x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56107vnfp-v0

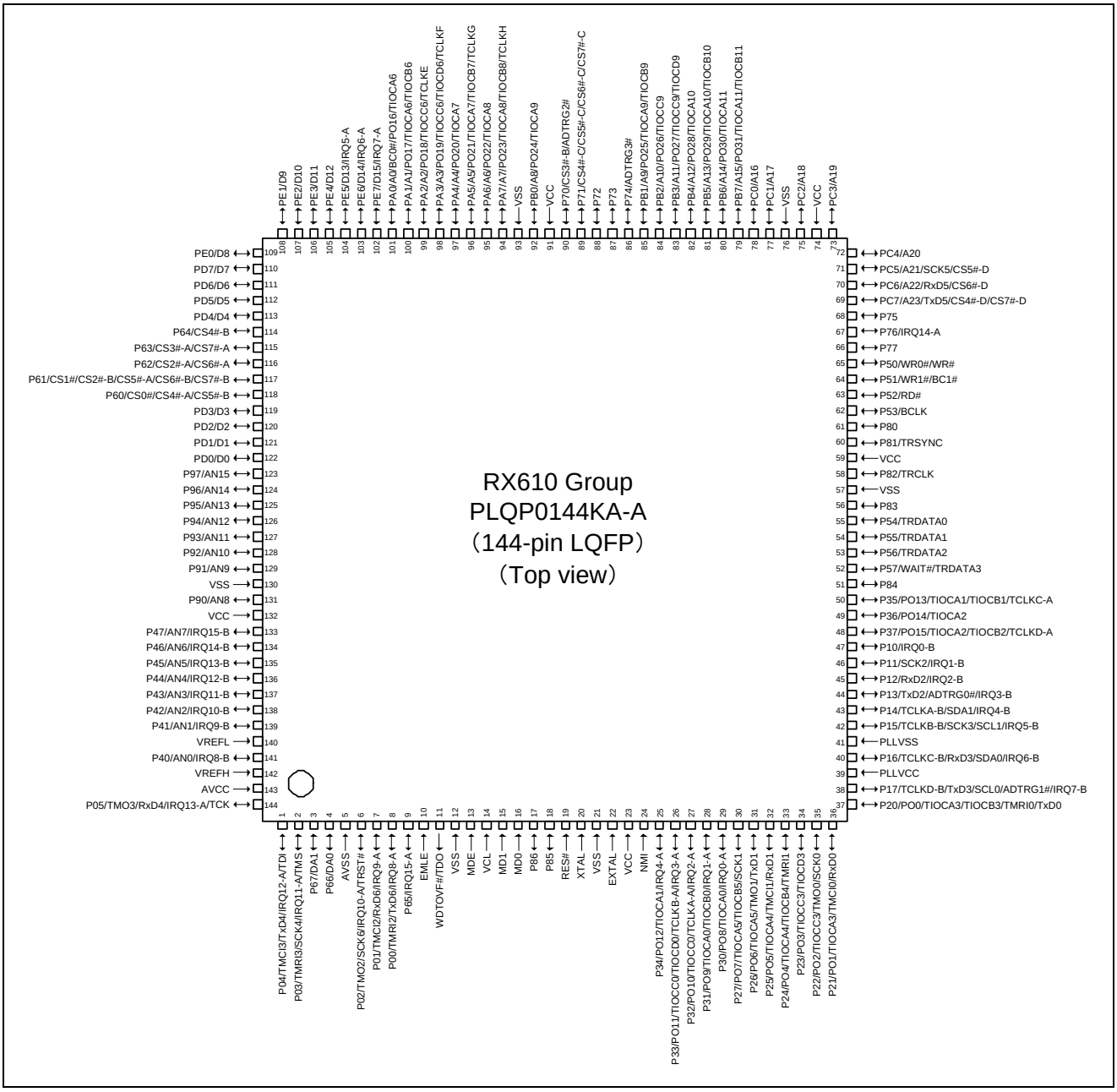

Figure 1.4 Pin Assignment of the 144-Pin LQFP

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
C6	VSS							
C7		P94					AN12	
C8	BSCANP							
C9		PG3						
C10		PD2		D2				
C11		P62		CS2#-A/ CS6#-A				
C12	VSS							
C13		PD7		D7				
C14		PE3		D11				
C15		PE5	IRQ5-A	D13				
D1		P65	IRQ15-A					
D2		P01	IRQ9-A		TMCI2	RxD6		
D3	AVSS							
D4		P40	IRQ8-B				AN0	
D5		P44	IRQ12-B				AN4	
D6		P91					AN9	
D7		P95					AN13	
D8		PG0						
D9		PG4						
D10		PD3		D3				
D11		P64		CS4#-B				
D12		PE4		D12				
D13		PE6	IRQ6-A	D14				
D14		PE7	IRQ7-A	D15				
D15		PG5						
E1	VSS							
E2	WDTOVF#							TDO
E3	EMLE							
E4		P00	IRQ8-A		TMRI2	TxD6		
E12	VCC							
E13		PG7						
E14		PG6						
E15	VSS							
F1	MD1							
F2	MD0							
F3	VCL							
F4	MDE							
F12		PA3		A3	PO19/ TIOCC6/ TIOCD6/ TCLKF			

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
F13		PA2		A2	PO18/ TIOCC6/ TCLKE			
F14		PA0		A0/BC0#	PO16/ TIOCA6			
F15		PA1		A1	PO17/ TIOCA6/ TIOCB6			
G1	RES#							
G2	XTAL							
G3		P85						
G4		P86						
G12		PA7		A7	PO23/ TIOCA8/ TIOCB8/ TCLKH			
G13		PA6		A6	PO22/ TIOCA8			
G14		PA4		A4	PO20/ TIOCA7			
G15		PA5		A5	PO21/ TIOCA7/ TIOCB7/ TCLKG			
H1	VCC							
H2			NMI					
H3	EXTAL							
H4	VSS							
H12		PB0		A8	PO24/ TIOCA9			
H13	VSS							
H14		PH0						
H15		PH1						
J1		PF5						
J2		PF4						
J3		PF6						
J4		P34	IRQ4-A		PO12/ TIOCA1			
J12		P72						
J13		P71		CS4#-C/ CS5#-C/ CS6#-C/ CS7#-C				
J14	VCC							

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
P2		P22			PO2/ TIOCC3/ TMO0	SCK0		
P3	PLLVCC							
P4		P15	IRQ5-B		TCLKB-B	SCK3/SCL1		
P5		P11	IRQ1-B			SCK2		
P6		P84						
P7		P54						TRDATA0
P8	VCC							
P9		P52		RD#				
P10		PH6						
P11	VCC							
P12		P77						
P13		PC6		A22/ CS6#-D		RxD5		
P14		PC4		A20				
P15	VCC							
R1		P21			PO1/ TIOCA3/ TMCI0	RxD0		
R2		P17	IRQ7-B		TCLKD-B	TxD3/SCL0	ADTRG1#	
R3	PLLVSS							
R4		P13	IRQ3-B			TxD2	ADTRG0#	
R5		P10	IRQ0-B					
R6		P35			PO13/ TIOCA1/ TIOCB1/ TCLKC-A			
R7		P55						TRDATA1
R8		P82						TRCLK
R9	BCLK	P53						
R10		PH7						
R11		PH5						
R12		PH3						
R13		P75						
R14		PC5		A21/ CS5#-D		SCK5		
R15		PC3		A19				

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
55		P54						TRDATA0
56		P83						
57	VSS							
58		P82						TRCLK
59	VCC							
60		P81						TRSYNC#
61		P80						
62	BCLK	P53						
63		P52		RD#				
64		P51		WR1#/BC1#				
65		P50		WR0#/WR#				
66		P77						
67		P76	IRQ14-A					
68		P75						
69		PC7		A23/ CS4#-D/ CS7#-D		TxD5		
70		PC6		A22/ CS6#-D		RxD5		
71		PC5		A21/ CS5#-D		SCK5		
72		PC4		A20				
73		PC3		A19				
74	VCC							
75		PC2		A18				
76	VSS							
77		PC1		A17				
78		PC0		A16				
79		PB7		A15	PO31/ TIOCA11/ TIOCB11			
80		PB6		A14	PO30/ TIOCA11			
81		PB5		A13	PO29/ TIOCA10/ TIOCB10			
82		PB4		A12	PO28/ TIOCA10			
83		PB3		A11	PO27/ TIOCC9/ TIOCD9			
84		PB2		A10	PO26/ TIOCC9			

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
108		PE1		D9				
109		PE0		D8				
110		PD7		D7				
111		PD6		D6				
112		PD5		D5				
113		PD4		D4				
114		P64		CS4#-B				
115		P63		CS3#-A/ CS7#-A				
116		P62		CS2#-A/ CS6#-A				
117		P61		CS1#/ CS2#-B/ CS5#-A/ CS6#-B/ CS7#-B				
118		P60		CS0#/ CS4#-A/ CS5#-B				
119		PD3		D3				
120		PD2		D2				
121		PD1		D1				
122		PD0		D0				
123		P97					AN15	
124		P96					AN14	
125		P95					AN13	
126		P94					AN12	
127		P93					AN11	
128		P92					AN10	
129		P91					AN9	
130	VSS							
131		P90					AN8	
132	VCC							
133		P47	IRQ15-B				AN7	
134		P46	IRQ14-B				AN6	
135		P45	IRQ13-B				AN5	
136		P44	IRQ12-B				AN4	
137		P43	IRQ11-B				AN3	
138		P42	IRQ10-B				AN2	
139		P41	IRQ9-B				AN1	
140	VREFL							
141		P40	IRQ8-B				AN0	
142	VREFH							
143	AVCC							
144		P05	IRQ13-A		TMO3	RxD4		TCK

Classifications	Pin Name	I/O	Description
Interrupt	NMI	Input	Non-maskable interrupt request signal
	IRQ0-A/IRQ0-B IRQ1-A/IRQ1-B IRQ2-A/IRQ2-B IRQ3-A/IRQ3-B IRQ4-A/IRQ4-B IRQ5-A/IRQ5-B IRQ6-A/IRQ6-B IRQ7-A/IRQ7-B IRQ8-A/IRQ8-B IRQ9-A/IRQ9-B IRQ10-A/IRQ10-B IRQ11-A/IRQ11-B IRQ12-A/IRQ12-B IRQ13-A/IRQ13-B IRQ14-A/IRQ14-B IRQ15-A/IRQ15-B	Input	Maskable request signals
16-bit timer pulse unit	TIOCA0, TIOCB0 TIOCC0, TIOCD0	I/O	Signals for TGRA0 to TGRD0. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA1, TIOCB1	I/O	Signals for TGRA1 and TGRB1. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA2, TIOCB2	I/O	Signals for TGRA2 and TGRB2. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA3, TIOCB3 TIOCC3, TIOCD3	I/O	Signals for TGRA3 to TGRD3. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA4, TIOCB4	I/O	Signals for TGRA4 and TGRB4. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA5, TIOCB5	I/O	Signals for TGRA5 and TGRB5. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA6, TIOCB6 TIOCC6, TIOCD6	I/O	Signals for TGRA6 to TGRD6. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA7, TIOCB7	I/O	Signals for TGRA7 and TGRB7. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA8, TIOCB8	I/O	Signals for TGRA8 and TGRB8. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA9, TIOCB9 TIOCC9, TIOCD9	I/O	Signals for TGRA9 to TGRD9. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA10, TIOCB10	I/O	Signals for TGRA10 and TGRB10. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA11, TIOCB11	I/O	Signals for TGRA11 and TGRB11. These pins are used as input capture inputs, output compare outputs, or PWM outputs.

Classifications	Pin Name	I/O	Description
Analog power supply	AVCC	Input	Analog power supply pin for the A/D and D/A converters. When the A/D and D/A converters are not in use, connect this pin to the system power supply.
	AVSS	Input	Ground pin for the A/D and D/A converters. Connect this pin to the system power supply (0 V).
	VREFH	Input	Reference power supply pin for the A/D and D/A converters. When the A/D and D/A converters are not in use, connect this pin to the system power supply.
	VREFL	Input	Reference ground pin for the A/D and D/A converters. Make sure to connect this pin to the analog reference power supply (0 V). When the A/D and D/A converters are not in use, connect this pin to the system power supply (0 V). For details, see section 23.6.7, Ranges of Settings for Analog Power Supply and Other Pins.
I/O ports	P00 to P05	I/O	6-bit input/output pins
	P10 to P17	I/O	8-bit input/output pins
	P20 to P27	I/O	8-bit input/output pins
	P30 to P37	I/O	8-bit input/output pins
	P40 to P47	I/O	8-bit input/output pins
	P50 to P57	I/O	8-bit input/output pins. (P53 is an input-only pin.)
	P60 to P67	I/O	8-bit input/output pins
	P70 to P77	I/O	8-bit input/output pins
	P80 to P86	I/O	7-bit input/output pins
	P90 to P97	I/O	8-bit input/output pins
	PA0 to PA7	I/O	8-bit input/output pins
	PB0 to PB7	I/O	8-bit input/output pins
	PC0 to PC7	I/O	8-bit input/output pins
	PD0 to PD7	I/O	8-bit input/output pins
	PE0 to PE7	I/O	8-bit input/output pins
	PF0 to PF6	I/O	7-bit input/output pins
	PG0 to PG7	I/O	8-bit input/output pins
	PH0 to PH7	I/O	8-bit input/output pins

Note 1: The A0 and BC0# pin functions are multiplexed on the same pin: the A0 pin is valid in byte-write mode and the BC0# pin becomes valid in single write-strobe mode. The setting for an eight-bit external bus width is prohibited in single write-strobe mode. For other multiplexed pin functions, refer to section 14, I/O Ports.

Note 2: The BC0# and BC1# signals are valid in both reading and writing.

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7170h	ICU	Interrupt request destination setting register 112	ISELR112	8	8	2 ICLK
0008 7175h	ICU	Interrupt request destination setting register 117	ISELR117	8	8	2 ICLK
0008 7176h	ICU	Interrupt request destination setting register 118	ISELR118	8	8	2 ICLK
0008 717Ah	ICU	Interrupt request destination setting register 122	ISELR122	8	8	2 ICLK
0008 717Bh	ICU	Interrupt request destination setting register 123	ISELR123	8	8	2 ICLK
0008 717Ch	ICU	Interrupt request destination setting register 124	ISELR124	8	8	2 ICLK
0008 717Dh	ICU	Interrupt request destination setting register 125	ISELR125	8	8	2 ICLK
0008 717Fh	ICU	Interrupt request destination setting register 127	ISELR127	8	8	2 ICLK
0008 7180h	ICU	Interrupt request destination setting register 128	ISELR128	8	8	2 ICLK
0008 7185h	ICU	Interrupt request destination setting register 133	ISELR133	8	8	2 ICLK
0008 7186h	ICU	Interrupt request destination setting register 134	ISELR134	8	8	2 ICLK
0008 718Ah	ICU	Interrupt request destination setting register 138	ISELR138	8	8	2 ICLK
0008 718Bh	ICU	Interrupt request destination setting register 139	ISELR139	8	8	2 ICLK
0008 718Ch	ICU	Interrupt request destination setting register 140	ISELR140	8	8	2 ICLK
0008 718Dh	ICU	Interrupt request destination setting register 141	ISELR141	8	8	2 ICLK
0008 7191h	ICU	Interrupt request destination setting register 145	ISELR145	8	8	2 ICLK
0008 7192h	ICU	Interrupt request destination setting register 146	ISELR146	8	8	2 ICLK
0008 7197h	ICU	Interrupt request destination setting register 151	ISELR151	8	8	2 ICLK
0008 7198h	ICU	Interrupt request destination setting register 152	ISELR152	8	8	2 ICLK
0008 719Ch	ICU	Interrupt request destination setting register 156	ISELR156	8	8	2 ICLK
0008 719Dh	ICU	Interrupt request destination setting register 157	ISELR157	8	8	2 ICLK
0008 719Eh	ICU	Interrupt request destination setting register 158	ISELR158	8	8	2 ICLK
0008 719Fh	ICU	Interrupt request destination setting register 159	ISELR159	8	8	2 ICLK
0008 71A1h	ICU	Interrupt request destination setting register 161	ISELR161	8	8	2 ICLK
0008 71A2h	ICU	Interrupt request destination setting register 162	ISELR162	8	8	2 ICLK
0008 71A7h	ICU	Interrupt request destination setting register 167	ISELR167	8	8	2 ICLK
0008 71A8h	ICU	Interrupt request destination setting register 168	ISELR168	8	8	2 ICLK
0008 71AEh	ICU	Interrupt request destination setting register 174	ISELR174	8	8	2 ICLK
0008 71AFh	ICU	Interrupt request destination setting register 175	ISELR175	8	8	2 ICLK
0008 71B1h	ICU	Interrupt request destination setting register 177	ISELR177	8	8	2 ICLK
0008 71B2h	ICU	Interrupt request destination setting register 178	ISELR178	8	8	2 ICLK
0008 71B4h	ICU	Interrupt request destination setting register 180	ISELR180	8	8	2 ICLK
0008 71B5h	ICU	Interrupt request destination setting register 181	ISELR181	8	8	2 ICLK
0008 71B7h	ICU	Interrupt request destination setting register 183	ISELR183	8	8	2 ICLK
0008 71B8h	ICU	Interrupt request destination setting register 184	ISELR184	8	8	2 ICLK
0008 71C6h	ICU	Interrupt request destination setting register 198	ISELR198	8	8	2 ICLK
0008 71C7h	ICU	Interrupt request destination setting register 199	ISELR199	8	8	2 ICLK
0008 71C8h	ICU	Interrupt request destination setting register 200	ISELR200	8	8	2 ICLK
0008 71C9h	ICU	Interrupt request destination setting register 201	ISELR201	8	8	2 ICLK
0008 71D7h	ICU	Interrupt request destination setting register 215	ISELR215	8	8	2 ICLK
0008 71D8h	ICU	Interrupt request destination setting register 216	ISELR216	8	8	2 ICLK
0008 71DBh	ICU	Interrupt request destination setting register 219	ISELR219	8	8	2 ICLK
0008 71DCh	ICU	Interrupt request destination setting register 220	ISELR220	8	8	2 ICLK
0008 71DFh	ICU	Interrupt request destination setting register 223	ISELR223	8	8	2 ICLK
0008 71E0h	ICU	Interrupt request destination setting register 224	ISELR224	8	8	2 ICLK

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7321h	ICU	Interrupt priority register 21	IPR21	8	8	2 ICLK
0008 7322h	ICU	Interrupt priority register 22	IPR22	8	8	2 ICLK
0008 7323h	ICU	Interrupt priority register 23	IPR23	8	8	2 ICLK
0008 7324h	ICU	Interrupt priority register 24	IPR24	8	8	2 ICLK
0008 7325h	ICU	Interrupt priority register 25	IPR25	8	8	2 ICLK
0008 7326h	ICU	Interrupt priority register 26	IPR26	8	8	2 ICLK
0008 7327h	ICU	Interrupt priority register 27	IPR27	8	8	2 ICLK
0008 7328h	ICU	Interrupt priority register 28	IPR28	8	8	2 ICLK
0008 7329h	ICU	Interrupt priority register 29	IPR29	8	8	2 ICLK
0008 732Ah	ICU	Interrupt priority register 2A	IPR2A	8	8	2 ICLK
0008 732Bh	ICU	Interrupt priority register 2B	IPR2B	8	8	2 ICLK
0008 732Ch	ICU	Interrupt priority register 2C	IPR2C	8	8	2 ICLK
0008 732Dh	ICU	Interrupt priority register 2D	IPR2D	8	8	2 ICLK
0008 732Eh	ICU	Interrupt priority register 2E	IPR2E	8	8	2 ICLK
0008 732Fh	ICU	Interrupt priority register 2F	IPR2F	8	8	2 ICLK
0008 7340h	ICU	Interrupt priority register 40	IPR40	8	8	2 ICLK
0008 7344h	ICU	Interrupt priority register 44	IPR44	8	8	2 ICLK
0008 7345h	ICU	Interrupt priority register 45	IPR45	8	8	2 ICLK
0008 7346h	ICU	Interrupt priority register 46	IPR46	8	8	2 ICLK
0008 7347h	ICU	Interrupt priority register 47	IPR47	8	8	2 ICLK
0008 734Ch	ICU	Interrupt priority register 4C	IPR4C	8	8	2 ICLK
0008 734Dh	ICU	Interrupt priority register 4D	IPR4D	8	8	2 ICLK
0008 734Eh	ICU	Interrupt priority register 4E	IPR4E	8	8	2 ICLK
0008 734Fh	ICU	Interrupt priority register 4F	IPR4F	8	8	2 ICLK
0008 7350h	ICU	Interrupt priority register 50	IPR50	8	8	2 ICLK
0008 7351h	ICU	Interrupt priority register 51	IPR51	8	8	2 ICLK
0008 7352h	ICU	Interrupt priority register 52	IPR52	8	8	2 ICLK
0008 7353h	ICU	Interrupt priority register 53	IPR53	8	8	2 ICLK
0008 7354h	ICU	Interrupt priority register 54	IPR54	8	8	2 ICLK
0008 7355h	ICU	Interrupt priority register 55	IPR55	8	8	2 ICLK
0008 7356h	ICU	Interrupt priority register 56	IPR56	8	8	2 ICLK
0008 7357h	ICU	Interrupt priority register 57	IPR57	8	8	2 ICLK
0008 7358h	ICU	Interrupt priority register 58	IPR58	8	8	2 ICLK
0008 7359h	ICU	Interrupt priority register 59	IPR59	8	8	2 ICLK
0008 735Ah	ICU	Interrupt priority register 5A	IPR5A	8	8	2 ICLK
0008 735Bh	ICU	Interrupt priority register 5B	IPR5B	8	8	2 ICLK
0008 735Ch	ICU	Interrupt priority register 5C	IPR5C	8	8	2 ICLK
0008 735Dh	ICU	Interrupt priority register 5D	IPR5D	8	8	2 ICLK
0008 735Eh	ICU	Interrupt priority register 5E	IPR5E	8	8	2 ICLK
0008 735Fh	ICU	Interrupt priority register 5F	IPR5F	8	8	2 ICLK
0008 7360h	ICU	Interrupt priority register 60	IPR60	8	8	2 ICLK
0008 7361h	ICU	Interrupt priority register 61	IPR61	8	8	2 ICLK
0008 7362h	ICU	Interrupt priority register 62	IPR62	8	8	2 ICLK
0008 7363h	ICU	Interrupt priority register 63	IPR63	8	8	2 ICLK
0008 7368h	ICU	Interrupt priority register 68	IPR68	8	8	2 ICLK

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8116h	TPU0	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8118h	TPU0	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 811Ah	TPU0	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 811Ch	TPU0	Timer general register C	TGRC	16	16	2 to 3 PCLK *7
0008 811Eh	TPU0	Timer general register D	TGRD	16	16	2 to 3 PCLK *7
0008 8120h	TPU1	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8121h	TPU1	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8122h	TPU1	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8124h	TPU1	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8125h	TPU1	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8126h	TPU1	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8128h	TPU1	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 812Ah	TPU1	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 8130h	TPU2	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8131h	TPU2	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8132h	TPU2	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8134h	TPU2	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8135h	TPU2	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8136h	TPU2	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8138h	TPU2	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 813Ah	TPU2	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 8140h	TPU3	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8141h	TPU3	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8142h	TPU3	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK *7
0008 8143h	TPU3	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK *7
0008 8144h	TPU3	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8145h	TPU3	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8146h	TPU3	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8148h	TPU3	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 814Ah	TPU3	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 814Ch	TPU3	Timer general register C	TGRC	16	16	2 to 3 PCLK *7
0008 814Eh	TPU3	Timer general register D	TGRD	16	16	2 to 3 PCLK *7
0008 8150h	TPU4	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8151h	TPU4	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8152h	TPU4	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8154h	TPU4	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8155h	TPU4	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8156h	TPU4	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8158h	TPU4	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 815Ah	TPU4	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 8160h	TPU5	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8161h	TPU5	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8162h	TPU5	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8164h	TPU5	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8165h	TPU5	Timer status register	TSR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 830Fh	RIIC0	Slave address register U2	SARU2	8	8	2 to 3 PCLK *7
0008 8310h	RIIC0	I²C bus bit rate low-level register	ICBRL	8	8	2 to 3 PCLK *7
0008 8311h	RIIC0	I²C bus bit rate high-level register	ICBRH	8	8	2 to 3 PCLK *7
0008 8312h	RIIC0	I²C bus transmit data register	ICDRT	8	8	2 to 3 PCLK *7
0008 8313h	RIIC0	I²C bus receive data register	ICDRR	8	8	2 to 3 PCLK *7
0008 8320h	RIIC1	I²C bus control register 1	ICCR1	8	8	2 to 3 PCLK *7
0008 8321h	RIIC1	I²C bus control register 2	ICCR2	8	8	2 to 3 PCLK *7
0008 8322h	RIIC1	I²C bus mode register 1	ICMR1	8	8	2 to 3 PCLK *7
0008 8323h	RIIC1	I²C bus mode register 2	ICMR2	8	8	2 to 3 PCLK *7
0008 8324h	RIIC1	I²C bus mode register 3	ICMR3	8	8	2 to 3 PCLK *7
0008 8325h	RIIC1	I²C bus function enable register	ICFER	8	8	2 to 3 PCLK *7
0008 8326h	RIIC1	I²C bus status enable register	ICSER	8	8	2 to 3 PCLK *7
0008 8327h	RIIC1	I²C bus interrupt enable register	ICIER	8	8	2 to 3 PCLK *7
0008 8328h	RIIC1	I²C bus status register 1	ICSR1	8	8	2 to 3 PCLK *7
0008 8329h	RIIC1	I²C bus status register 2	ICSR2	8	8	2 to 3 PCLK *7
0008 832Ah	RIIC1	Slave address register L0	SARL0	8	8	2 to 3 PCLK *7
0008 832Ah	RIIC1	Internal control for timeout L	TMOCNTL	16	16	2 to 3 PCLK *7
0008 832Bh	RIIC1	Slave address register U0	SARU0	8	8	2 to 3 PCLK *7
0008 832Bh	RIIC1	Internal control for timeout U	TMOCNTU	16	16	2 to 3 PCLK *7
0008 832Ch	RIIC1	Slave address register L1	SARL1	8	8	2 to 3 PCLK *7
0008 832Dh	RIIC1	Slave address register U1	SARU1	8	8	2 to 3 PCLK *7
0008 832Eh	RIIC1	Slave address register L2	SARL2	8	8	2 to 3 PCLK *7
0008 832Fh	RIIC1	Slave address register U2	SARU2	8	8	2 to 3 PCLK *7
0008 8330h	RIIC1	I²C bus bit rate low-level register	ICBRL	8	8	2 to 3 PCLK *7
0008 8331h	RIIC1	I²C bus bit rate high-level register	ICBRH	8	8	2 to 3 PCLK *7
0008 8332h	RIIC1	I²C bus transmit data register	ICDRT	8	8	2 to 3 PCLK *7
0008 8333h	RIIC1	I²C bus receive data register	ICDRR	8	8	2 to 3 PCLK *7
0008 C000h	P0	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C001h	P1	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C002h	P2	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C003h	P3	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C004h	P4	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C005h	P5	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C006h	P6	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C007h	P7	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C008h	P8	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C009h	P9	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Ah	PA	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Bh	PB	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Ch	PC	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Dh	PD	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Eh	PE	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Fh	PF	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C010h	PG	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C011h	PH	Data direction register	DDR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C020h	P0	Data register	DR	8	8	2 to 3 PCLK *7
0008 C021h	P1	Data register	DR	8	8	2 to 3 PCLK *7
0008 C022h	P2	Data register	DR	8	8	2 to 3 PCLK *7
0008 C023h	P3	Data register	DR	8	8	2 to 3 PCLK *7
0008 C024h	P4	Data register	DR	8	8	2 to 3 PCLK *7
0008 C025h	P5	Data register	DR	8	8	2 to 3 PCLK *7
0008 C026h	P6	Data register	DR	8	8	2 to 3 PCLK *7
0008 C027h	P7	Data register	DR	8	8	2 to 3 PCLK *7
0008 C028h	P8	Data register	DR	8	8	2 to 3 PCLK *7
0008 C029h	P9	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Ah	PA	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Bh	PB	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Ch	PC	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Dh	PD	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Eh	PE	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Fh	PF	Data register	DR	8	8	2 to 3 PCLK *7
0008 C030h	PG	Data register	DR	8	8	2 to 3 PCLK *7
0008 C031h	PH	Data register	DR	8	8	2 to 3 PCLK *7
0008 C040h	P0	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C041h	P1	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C042h	P2	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C043h	P3	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C044h	P4	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C045h	P5	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C046h	P6	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C047h	P7	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C048h	P8	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C049h	P9	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Ah	PA	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Bh	PB	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Ch	PC	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Dh	PD	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Eh	PE	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Fh	PF	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C050h	PG	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C051h	PH	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C060h	P0	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C061h	P1	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C062h	P2	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C063h	P3	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C064h	P4	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C065h	P5	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C066h	P6	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C067h	P7	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C068h	P8	Input buffer control register	ICR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C069h	P9	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C06Ah	PA	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C06Bh	PB	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C06Ch	PC	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C06Dh	PD	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C06Eh	PE	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C06Fh	PF	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C070h	PG	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C071h	PH	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C082h	P2	Open drain control register	ODR	8	8	2 to 3 PCLK *7
0008 C08Ch	PC	Open drain control register	ODR	8	8	2 to 3 PCLK *7
0008 C0CAh	PA	Pull-Up resistor control register	PCR	8	8	2 to 3 PCLK *7
0008 C0CBh	PB	Pull-Up resistor control register	PCR	8	8	2 to 3 PCLK *7
0008 C0CCh	PC	Pull-Up resistor control register	PCR	8	8	2 to 3 PCLK *7
0008 C0CDh	PD	Pull-Up resistor control register	PCR	8	8	2 to 3 PCLK *7
0008 C0CEh	PE	Pull-Up resistor control register	PCR	8	8	2 to 3 PCLK *7
0008 C100h	I/O PORT	Port function control register 0	PFCR0	8	8	2 to 3 PCLK *7
0008 C101h	I/O PORT	Port function control register 1	PFCR1	8	8	2 to 3 PCLK *7
0008 C102h	I/O PORT	Port function control register 2	PFCR2	8	8	2 to 3 PCLK *7
0008 C103h	I/O PORT	Port function control register 3	PFCR3	8	8	2 to 3 PCLK *7
0008 C104h	I/O PORT	Port function control register 4	PFCR4	8	8	2 to 3 PCLK *7
0008 C105h	I/O PORT	Port function control register 5	PFCR5	8	8	2 to 3 PCLK *7
0008 C106h	I/O PORT	Port function control register 6	PFCR6	8	8	2 to 3 PCLK *7
0008 C107h	I/O PORT	Port function control register 7	PFCR7	8	8	2 to 3 PCLK *7
0008 C108h	I/O PORT	Port function control register 8	PFCR8	8	8	2 to 3 PCLK *7
0008 C109h	I/O PORT	Port function control register 9	PFCR9	8	8	2 to 3 PCLK *7
0008 C280h	SYSTEM	Deep standby control register	DPSBYCR	8	8	4 to 5 PCLK *7
0008 C281h	SYSTEM	Deep standby wait control register	DPSWCR	8	8	4 to 5 PCLK *7
0008 C282h	SYSTEM	Deep standby interrupt enable register	DPSIER	8	8	4 to 5 PCLK *7
0008 C283h	SYSTEM	Deep standby interrupt flag register	DPSIFR	8	8	4 to 5 PCLK *7
0008 C284h	SYSTEM	Deep standby interrupt edge register	DPSIEGR	8	8	4 to 5 PCLK *7
0008 C285h	SYSTEM	Reset status register	RSTSR	8	8	4 to 5 PCLK *7
0008 C289h	FLASH	Flash write erase protection register	FWEPROR	8	8	4 to 5 PCLK *7
0008 C290h	SYSTEM	Deep standby backup register 0	DPSBKR0	8	8	4 to 5 PCLK *7
0008 C291h	SYSTEM	Deep standby backup register 1	DPSBKR1	8	8	4 to 5 PCLK *7
0008 C292h	SYSTEM	Deep standby backup register 2	DPSBKR2	8	8	4 to 5 PCLK *7
0008 C293h	SYSTEM	Deep standby backup register 3	DPSBKR3	8	8	4 to 5 PCLK *7
0008 C294h	SYSTEM	Deep standby backup register 4	DPSBKR4	8	8	4 to 5 PCLK *7
0008 C295h	SYSTEM	Deep standby backup register 5	DPSBKR5	8	8	4 to 5 PCLK *7
0008 C296h	SYSTEM	Deep standby backup register 6	DPSBKR6	8	8	4 to 5 PCLK *7
0008 C297h	SYSTEM	Deep standby backup register 7	DPSBKR7	8	8	4 to 5 PCLK *7
0008 C298h	SYSTEM	Deep standby backup register 8	DPSBKR8	8	8	4 to 5 PCLK *7
0008 C299h	SYSTEM	Deep standby backup register 9	DPSBKR9	8	8	4 to 5 PCLK *7
0008 C29Ah	SYSTEM	Deep standby backup register 10	DPSBKR10	8	8	4 to 5 PCLK *7
0008 C29Bh	SYSTEM	Deep standby backup register 11	DPSBKR11	8	8	4 to 5 PCLK *7

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}, $PLLV_{CC}$	-0.3 to +4.6	V
Input voltage (except for ports 0, 14 to 17)	V_{in}	-0.3 to V_{CC} +0.3	V
Input voltage (ports 0, 14 to 17*1)	V_{in}	-0.3 to +6.5	V
Reference power supply voltage	V_{REFH}	-0.3 to V_{CC} +0.3	V
Analog power supply voltage	AV_{CC}*2	-0.3 to +4.6	V
Analog input voltage	V_{AN}	-0.3 to V_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: -20 to +85	°C
		Wide-range specifications: -40 to +85	
Storage temperature	T_{stg}	-55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Notes: 1. Ports 0, and 14 to 17 are 5 V tolerant.

2. Connect AV_{CC} to V_{CC}. When neither the A/D converter nor the D/A converter is in use, do not leave the AV_{SS}, V_{REFH}, and V_{REFL} pins open. Connect the AV_{CC} and V_{REFH} pins to V_{CC}, and the AV_{SS} and V_{REFL} pins to V_{SS}, respectively.

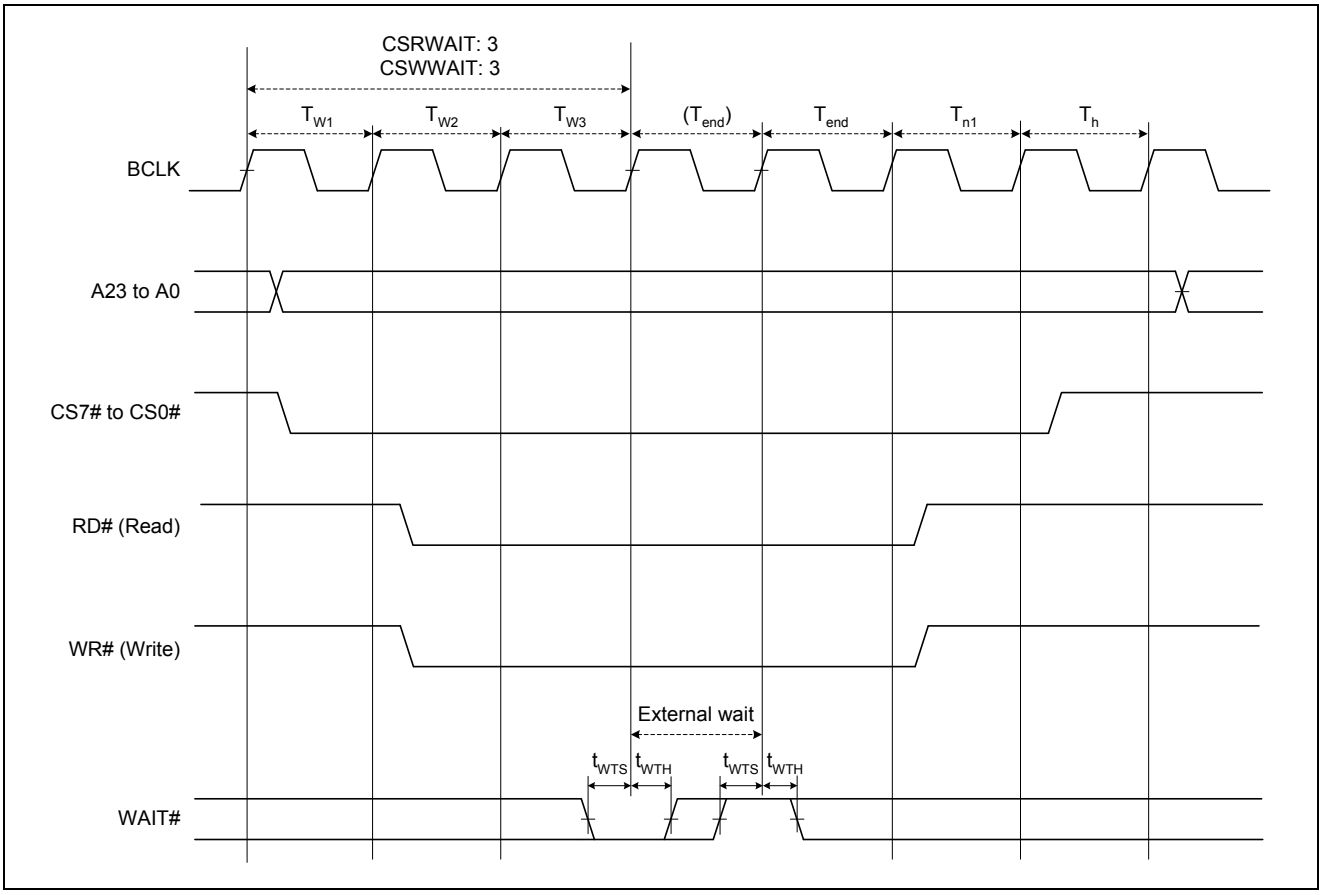

Figure 5.13 External Bus Timing/External Wait Control

5.3.4 Timing of On-Chip Peripheral Modules

Table 5.8 Timing of On-Chip Peripheral Modules (1)

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V, PCLK = 8 to 50 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)
Output load conditions: V_{OH} = V_{CC} x 0.5, V_{OL} = V_{CC} x 0.5, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item			Symbol	Min.	Max.	Unit	Test Conditions
I/O ports	Output data delay time		t_{PWD}	—	40	ns	Figure 5.14
	Input data setup time		t_{PRS}	25	—	ns	
	Input data hold time		t_{PRH}	25	—	ns	
TPU	Timer output delay time		t_{TOCD}	—	40	ns	Figure 5.15
	Timer input setup time		t_{TICS}	25	—	ns	
	Timer clock input setup time		t_{TCKS}	25	—	ns	Figure 5.16
	Timer clock pulse width	Single-edge setting	t_{TCKWH}	1.5 x (1/PCLK)	—	t_{cyc}	
		Both-edge setting	t_{TCKWL}	2.5 x (1/PCLK)	—	t_{cyc}	
PPG	Pulse output delay time		t_{POD}	—	40	ns	Figure 5.17
8-bit timer	Timer output delay time		t_{TMOD}	—	40	ns	Figure 5.18
	Timer reset input setup time		t_{TMRS}	25	—	ns	Figure 5.19
	Timer clock input setup time		t_{TMCS}	25	—	ns	Figure 5.20
	Timer clock pulse width	Single-edge setting	t_{TMCWH}	1.5 x (1/PCLK)	—	t_{cyc}	
		Both-edge setting	t_{TMCWL}	2.5 x (1/PCLK)	—	t_{cyc}	
WDT	Overflow output delay time		t_{WOVD}	—	40	ns	Figure 5.21
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4 x (1/PCLK)	—	t_{cyc}	Figure 5.22
		Clock synchronous		6 x (1/PCLK)	—		
	Input clock pulse width		t_{SCKW}	0.4 x t_{Scyc}	0.6 x t_{Scyc}	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	20	ns	
	Input clock fall time		t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	4 x (1/PCLK)	—	t_{cyc}	
		Clock synchronous		6 x (1/PCLK)	—		
	Output clock pulse width		t_{SCKW}	0.4 x t_{Scyc}	0.6 x t_{Scyc}	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	20	ns	
	Output clock fall time		t_{SCKf}	—	20	ns	
	Transmit data delay time		t_{TXD}	—	40	ns	Figure 5.23
	Receive data setup time (clock synchronous)		t_{RXS}	40	—	ns	
	Receive data hold time (clock synchronous)		t_{RXH}	40	—	ns	
A/D converter	Trigger input setup time		t_{TRGS}	25	—	ns	Figure 5.24

Table 5.8 Timing of On-Chip Peripheral Modules (3)

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V,
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item		Symbol	Min. *1*2	Max.	Unit	Test Conditions
RIIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	8(10) x (1/PCLK) + 240	—	ns	Figure 5.25
	SCL input high pulse width	t_{SCLH}	3(5) x (1/PCLK) + 120	—	ns	
	SCL input low pulse width	t_{SCLL}	5 x (1/PCLK) + 120	—	ns	
	SCL, SDA input rising time	t_{Sr}	—	120	ns	
	SCL, SDA input falling time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 x (1/PCLK)	ns	
	SDA input bus free time	t_{BUF}	5 x (1/PCLK) + 120	—	ns	
	Start condition input hold time	t_{STAH}	3(5) x (1/PCLK) + 120	—	ns	
	Re-start condition input setup time	t_{STAS}	5 x (1/PCLK) + 120	—	ns	
	Stop condition input setup time	t_{STOS}	3(5) x (1/PCLK) + 120	—	ns	
	Data input setup time	t_{SDAS}	50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	550	pF	
Boundary scan (176-pin LFBGA)	TCK clock cycle time	tTCKcyc	100	—	ns	Figure 5.26
	TCK clock high level pulse width	tTCKH	45	—	ns	
	TCK clock low level pulse width	tTCKL	45	—	ns	
	TCK clock rising time	tTCKr	—	5	ns	
	TCK clock falling time	tTCKf	—	5	ns	
	TRST# pulse width	tTRSTW	20	—	Tcyc	Figure 5.27
	TMS setup time	tTMSS	20	—	ns	Figure 5.28
	TMS hold time	tTMSH	20	—	ns	
	TDI setup time	tTDIS	20	—	ns	
	TDI hold time	tTDIH	20	—	ns	
	TDO data delay time	tTDOD	—	40	ns	

Notes:1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.

2. Cb indicates the total capacity of the bus line.

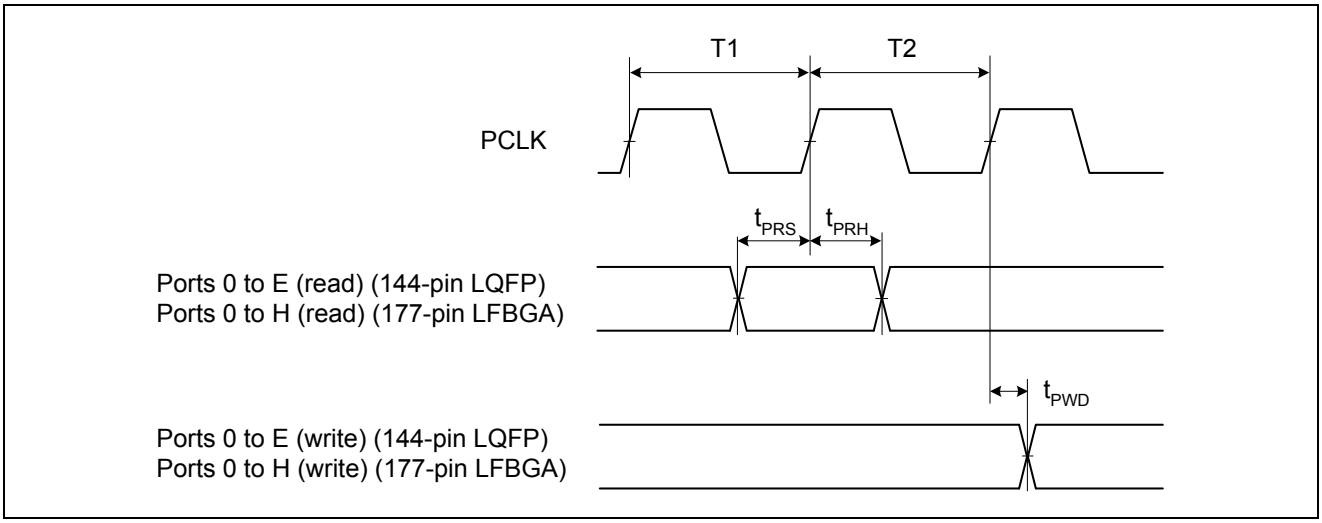

Figure 5.14 I/O Port Input/Output Timing

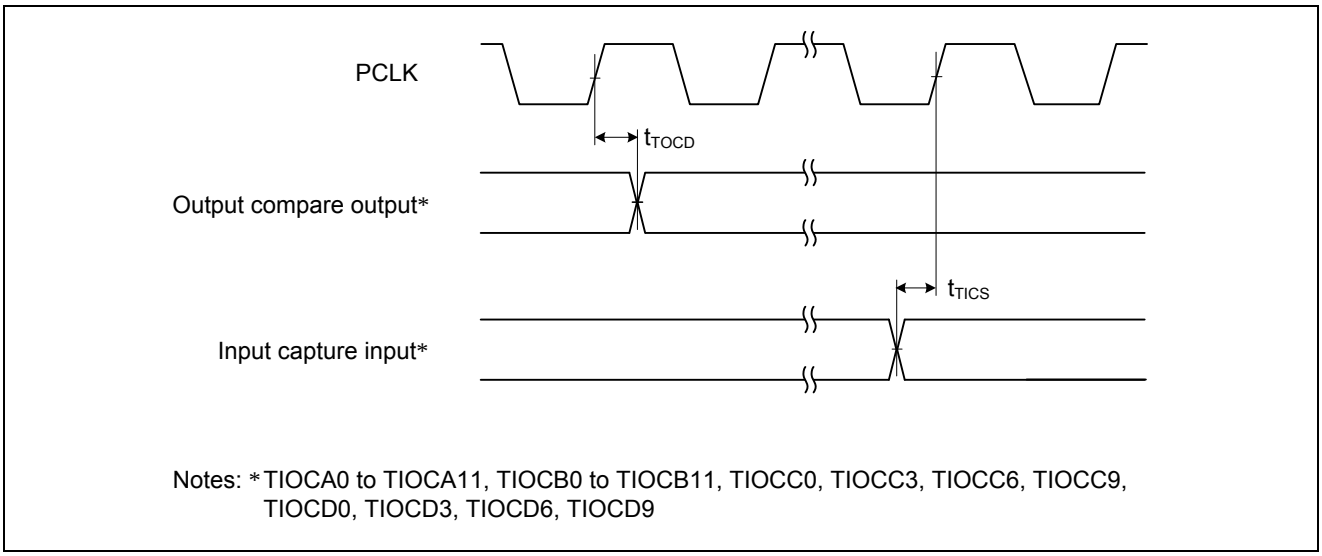

Figure 5.15 TPU Input/Output Timing

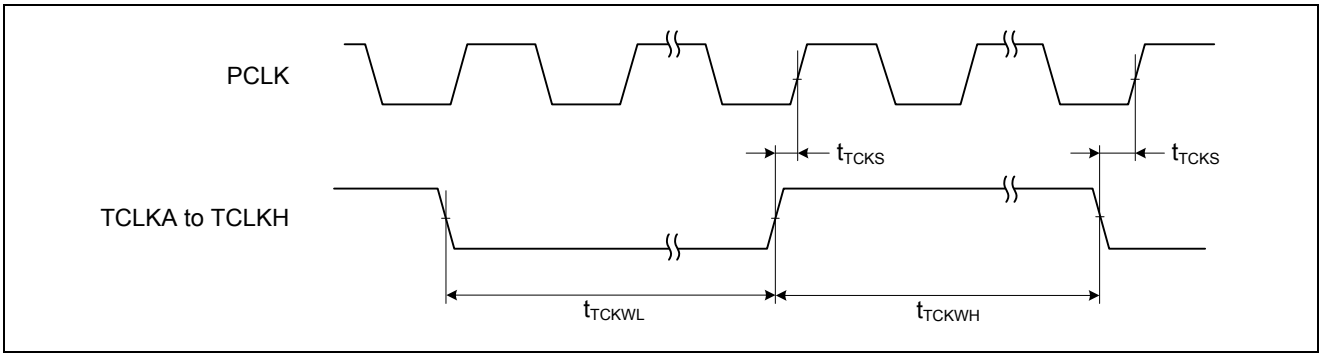

Figure 5.16 TPU Clock Input Timing

5.4 A/D Conversion Characteristics

Table 5.9 A/D Conversion Characteristics

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V, PCLK = 8 to 50 MHz, ADCLK = 4 to 50 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			10	10	10	Bit	
Conversion time*1 (ADCLK = 50-MHz operation)	With 0.1-µF external capacitor	When the capacitor is charged enough*2	0.8 (0.3)*3	—	—	µs	Sampling 15 states
	Without external capacitor	Permissible signal source impedance (max.) = 1.0 kΩ	1.0 (0.5)*3	—	—		Sampling 25 states
		Permissible signal source impedance (max.) = 5.0 kΩ	2.6 (2.1)*3	—	—		Sampling 105 states
Analog input capacitance			—	—	6.0	pF	
INL integral nonlinearity error (INL)			—	±1.5	±3.0	LSB	
Offset error			—	±1.5	±3.0	LSB	
Full-scale error			—	±1.5	±3.0	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	±1.5	±3.0	LSB	
DNL differential nonlinearity error (DNL)			—	±0.5	±1.0	LSB	

Notes: 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
2. The scanning is not supported.
3. The value in parentheses indicates the sampling time.

5.5 D/A Conversion Characteristics

Table 5.10 D/A Conversion Characteristics

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V, PCLK = 8 to 50 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time	—	—	3	µs	20-pF capacitive load
Absolute accuracy	—	±2.0	±4.0	LSB	2-MΩ resistive load
	—	—	±3.0	LSB	4-MΩ resistive load
	—	—	±2.0	LSB	10-MΩ resistive load
RO output resistance	—	3.6	—	kΩ	