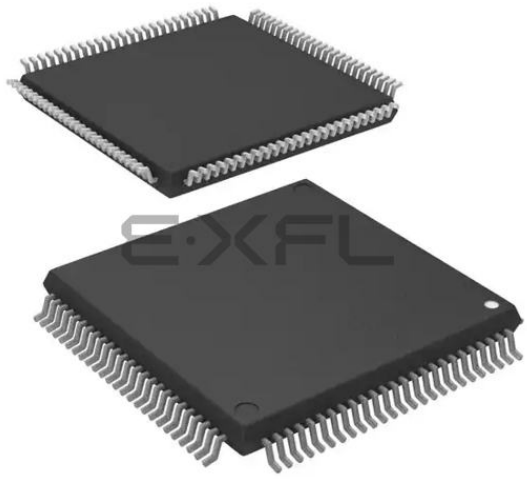
Renesas Electronics America Inc - R5F56108VDFP#V0 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	117
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 2x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56108vdfp-v0

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
32		P25			PO5/ TIOCA4/ TMCI1	RxD1		
33		P24			PO4/ TIOCA4/ TIOCB4/ TMRI1			
34		P23			PO3/ TIOCC3/ TIOCD3			
35		P22			PO2/ TIOCC3/ TMO0	SCK0		
36		P21			PO1/ TIOCA3/ TMCI0	RxD0		
37		P20			PO0/ TIOCA3/ TIOCB3/ TMRI0	TxD0		
38		P17	IRQ7-B		TCLKD-B	TxD3/SCL0	ADTRG1#	
39	PLLVCC							
40		P16	IRQ6-B		TCLKC-B	RxD3/SDA0		
41	PLLVSS							
42		P15	IRQ5-B		TCLKB-B	SCK3/SCL1		
43		P14	IRQ4-B		TCLKA-B	SDA1		
44		P13	IRQ3-B			TxD2	ADTRG0#	
45		P12	IRQ2-B			RxD2		
46		P11	IRQ1-B			SCK2		
47		P10	IRQ0-B					
48		P37			PO15/ TIOCA2/ TIOCB2/ TCLKD-A			
49		P36			PO14/ TIOCA2			
50		P35			PO13/ TIOCA1/ TIOCB1/ TCLKC-A			
51		P84						
52		P57		WAIT#				TRDATA3
53		P56						TRDATA2
54		P55						TRDATA1

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
55		P54						TRDATA0
56		P83						
57	VSS							
58		P82						TRCLK
59	VCC							
60		P81						TRSYNC#
61		P80						
62	BCLK	P53						
63		P52		RD#				
64		P51		WR1#/BC1#				
65		P50		WR0#/WR#				
66		P77						
67		P76	IRQ14-A					
68		P75						
69		PC7		A23/ CS4#-D/ CS7#-D		TxD5		
70		PC6		A22/ CS6#-D		RxD5		
71		PC5		A21/ CS5#-D		SCK5		
72		PC4		A20				
73		PC3		A19				
74	VCC							
75		PC2		A18				
76	VSS							
77		PC1		A17				
78		PC0		A16				
79		PB7		A15	PO31/ TIOCA11/ TIOCB11			
80		PB6		A14	PO30/ TIOCA11			
81		PB5		A13	PO29/ TIOCA10/ TIOCB10			
82		PB4		A12	PO28/ TIOCA10			
83		PB3		A11	PO27/ TIOCC9/ TIOCD9			
84		PB2		A10	PO26/ TIOCC9			

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
85		PB1		A9	PO25/ TIOCA9/ TIOCB9			
86		P74					ADTRG3#	
87		P73						
88		P72						
89		P71		CS4#-C/ CS5#-C/ CS6#-C/ CS7#-C				
90		P70		CS3#-B			ADTRG2#	
91	VCC							
92		PB0		A8	PO24/ TIOCA9			
93	VSS							
94		PA7		A7	PO23/ TIOCA8/ TIOCB8/ TCLKH			
95		PA6		A6	PO22/ TIOCA8			
96		PA5		A5	PO21/ TIOCA7/ TIOCB7/ TCLKG			
97		PA4		A4	PO20/ TIOCA7			
98		PA3		A3	PO19/ TIOCC6/ TIOCD6/ TCLKF			
99		PA2		A2	PO18/ TIOCC6/ TCLKE			
100		PA1		A1	PO17/ TIOCA6/ TIOCB6			
101		PA0		A0/BC0#	PO16/ TIOCA6			
102		PE7	IRQ7-A	D15				
103		PE6	IRQ6-A	D14				
104		PE5	IRQ5-A	D13				
105		PE4		D12				
106		PE3		D11				
107		PE2		D10				

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
108		PE1		D9				
109		PE0		D8				
110		PD7		D7				
111		PD6		D6				
112		PD5		D5				
113		PD4		D4				
114		P64		CS4#-B				
115		P63		CS3#-A/ CS7#-A				
116		P62		CS2#-A/ CS6#-A				
117		P61		CS1#/ CS2#-B/ CS5#-A/ CS6#-B/ CS7#-B				
118		P60		CS0#/ CS4#-A/ CS5#-B				
119		PD3		D3				
120		PD2		D2				
121		PD1		D1				
122		PD0		D0				
123		P97					AN15	
124		P96					AN14	
125		P95					AN13	
126		P94					AN12	
127		P93					AN11	
128		P92					AN10	
129		P91					AN9	
130	VSS							
131		P90					AN8	
132	VCC							
133		P47	IRQ15-B				AN7	
134		P46	IRQ14-B				AN6	
135		P45	IRQ13-B				AN5	
136		P44	IRQ12-B				AN4	
137		P43	IRQ11-B				AN3	
138		P42	IRQ10-B				AN2	
139		P41	IRQ9-B				AN1	
140	VREFL							
141		P40	IRQ8-B				AN0	
142	VREFH							
143	AVCC							
144		P05	IRQ13-A		TMO3	RxD4		TCK

Classifications	Pin Name	I/O	Description
Bus control	RD#	Output	Strobe signal which indicates that reading from the external address space is in progress.
	WR0#	Output	Strobe signal which indicates that the lower-order byte (D0 to D7) is valid in writing to the external address space, in byte strobe mode.
	WR1#	Output	Strobe signal which indicates that the higher-order byte (D8 to D15) is valid in writing to the external address space, in byte strobe mode.
	WR#	Output	Strobe signal which indicates that writing to the external address space is in progress, in 1-write strobe mode.
	BC0# *1, *2	Output	Strobe signal which indicates that the lower-order byte (D0 to D7) is valid in access to the external address space, in 1-write strobe mode.
	BC1# *2	Output	Strobe signal which indicates that the higher-order byte (D8 to D15) is valid in access to the external address space, in 1-write strobe mode.
	CS0#, CS1# CS2#-A/CS2#-B CS3#-A/CS3#-B CS4#-A/CS4#-B/ CS4#-C/CS4#-D CS5#-A/CS5#-B/ CS5#-C/CS5#-D CS6#-A/CS6#-B/ CS6#-C/CS6#-D CS7#-A/CS7#-B/ CS7#-C/CS7#-D	Output	Select signals for areas 0 to 7
	WAIT#	Input	Requests wait cycles in access to the external address space

2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

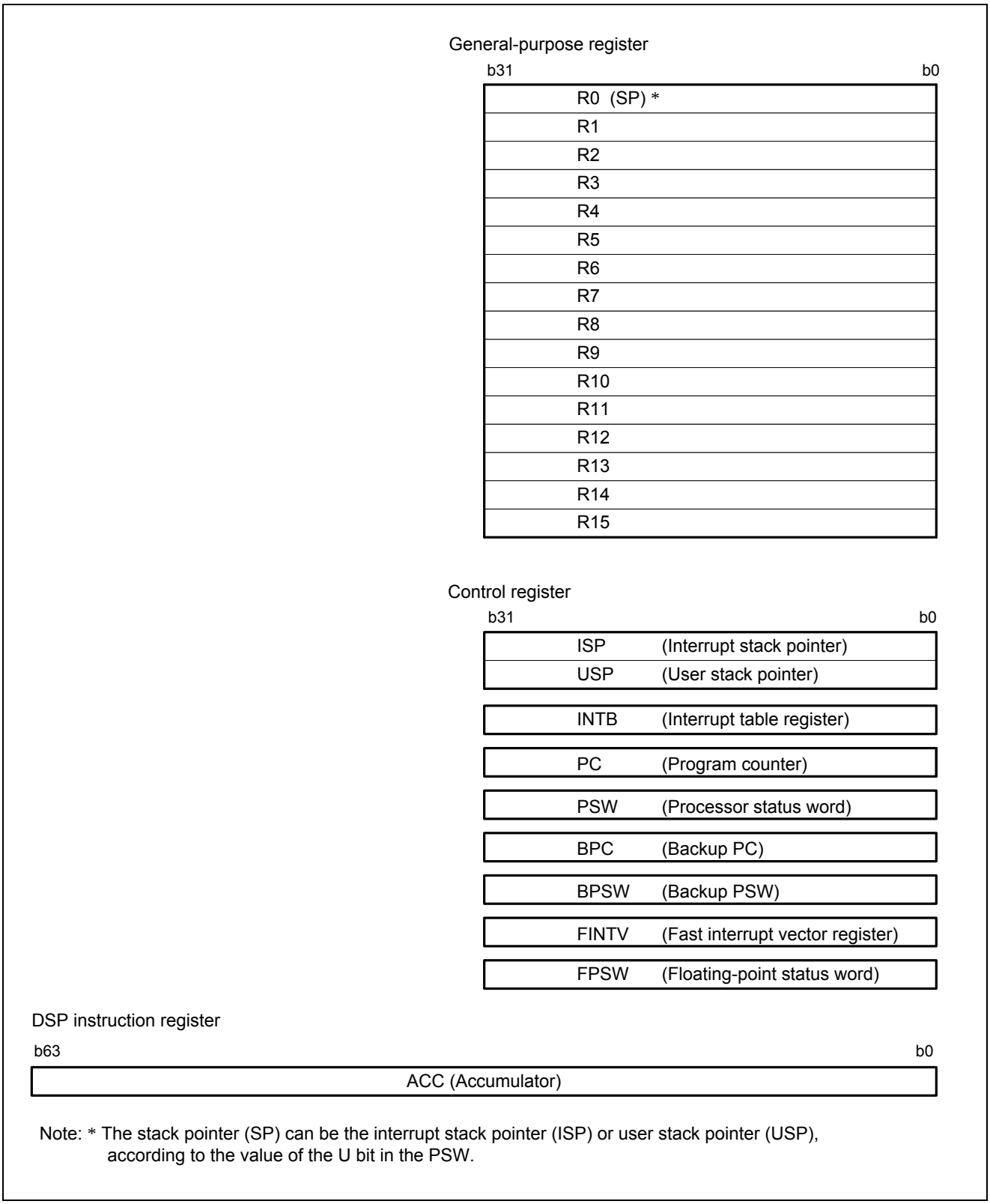
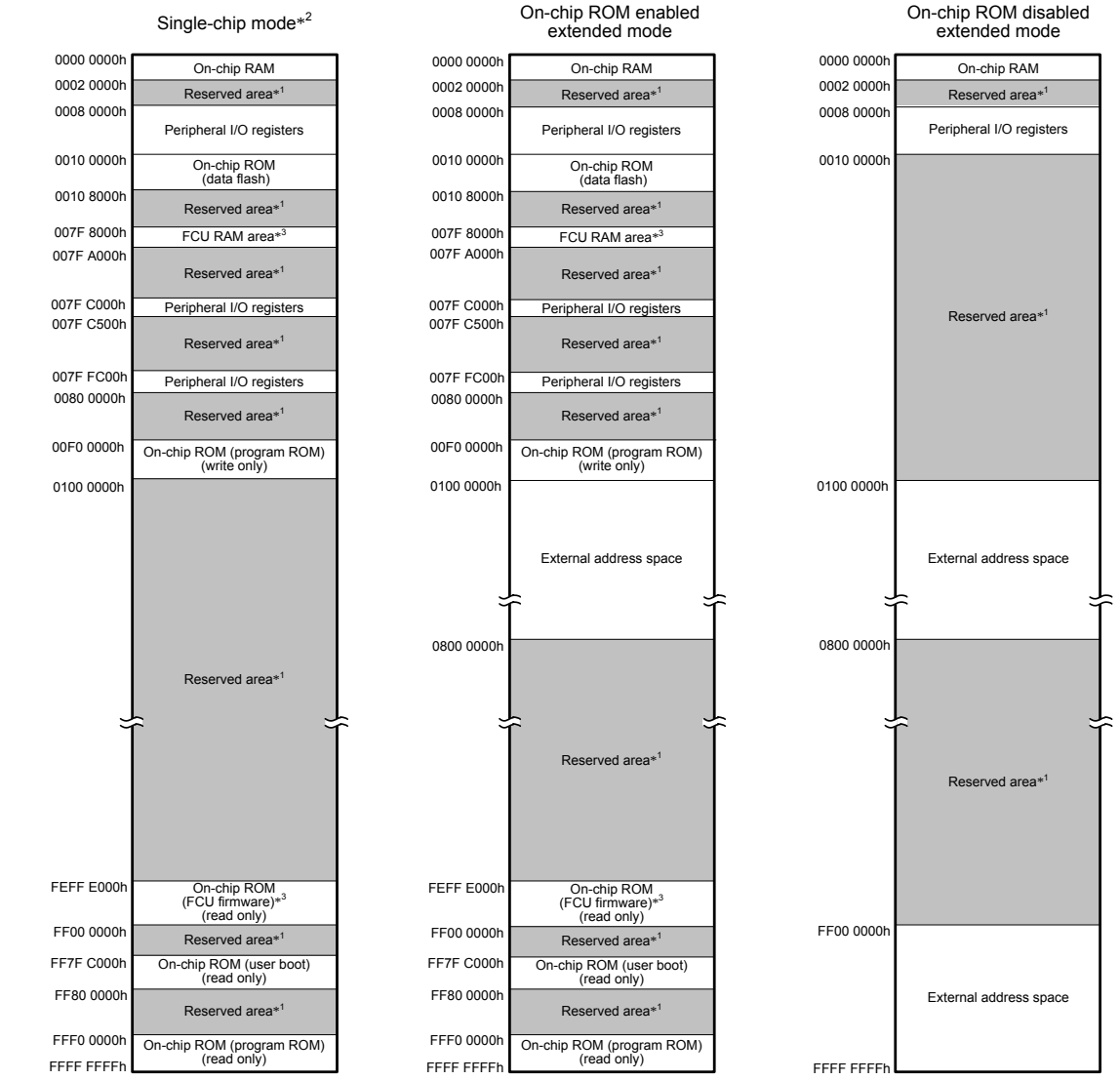


Figure 2.1 Register Set of the CPU



Notes: 1. A reserved area should not be accessed.
2. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
3. For details on the FCU, see section 26, ROM (Flash Memory for Code Storage) and section 27, Data Flash (Flash Memory for Data Storage) in the User's manual: Hardware.

Figure 3.3 Memory Map of the R5F56106

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7064h	ICU	Interrupt request register 100	IR100	8	8	2 ICLK
0008 7065h	ICU	Interrupt request register 101	IR101	8	8	2 ICLK
0008 7068h	ICU	Interrupt request register 104	IR104	8	8	2 ICLK
0008 7069h	ICU	Interrupt request register 105	IR105	8	8	2 ICLK
0008 706Ah	ICU	Interrupt request register 106	IR106	8	8	2 ICLK
0008 706Bh	ICU	Interrupt request register 107	IR107	8	8	2 ICLK
0008 706Ch	ICU	Interrupt request register 108	IR108	8	8	2 ICLK
0008 706Fh	ICU	Interrupt request register 111	IR111	8	8	2 ICLK
0008 7070h	ICU	Interrupt request register 112	IR112	8	8	2 ICLK
0008 7073h	ICU	Interrupt request register 115	IR115	8	8	2 ICLK
0008 7074h	ICU	Interrupt request register 116	IR116	8	8	2 ICLK
0008 7075h	ICU	Interrupt request register 117	IR117	8	8	2 ICLK
0008 7076h	ICU	Interrupt request register 118	IR118	8	8	2 ICLK
0008 7078h	ICU	Interrupt request register 120	IR120	8	8	2 ICLK
0008 7079h	ICU	Interrupt request register 121	IR121	8	8	2 ICLK
0008 707Ah	ICU	Interrupt request register 122	IR122	8	8	2 ICLK
0008 707Bh	ICU	Interrupt request register 123	IR123	8	8	2 ICLK
0008 707Ch	ICU	Interrupt request register 124	IR124	8	8	2 ICLK
0008 707Dh	ICU	Interrupt request register 125	IR125	8	8	2 ICLK
0008 707Eh	ICU	Interrupt request register 126	IR126	8	8	2 ICLK
0008 707Fh	ICU	Interrupt request register 127	IR127	8	8	2 ICLK
0008 7080h	ICU	Interrupt request register 128	IR128	8	8	2 ICLK
0008 7083h	ICU	Interrupt request register 131	IR131	8	8	2 ICLK
0008 7084h	ICU	Interrupt request register 132	IR132	8	8	2 ICLK
0008 7085h	ICU	Interrupt request register 133	IR133	8	8	2 ICLK
0008 7086h	ICU	Interrupt request register 134	IR134	8	8	2 ICLK
0008 7088h	ICU	Interrupt request register 136	IR136	8	8	2 ICLK
0008 7089h	ICU	Interrupt request register 137	IR137	8	8	2 ICLK
0008 708Ah	ICU	Interrupt request register 138	IR138	8	8	2 ICLK
0008 708Bh	ICU	Interrupt request register 139	IR139	8	8	2 ICLK
0008 708Ch	ICU	Interrupt request register 140	IR140	8	8	2 ICLK
0008 708Dh	ICU	Interrupt request register 141	IR141	8	8	2 ICLK
0008 708Eh	ICU	Interrupt request register 142	IR142	8	8	2 ICLK
0008 7091h	ICU	Interrupt request register 145	IR145	8	8	2 ICLK
0008 7092h	ICU	Interrupt request register 146	IR146	8	8	2 ICLK
0008 7095h	ICU	Interrupt request register 149	IR149	8	8	2 ICLK
0008 7096h	ICU	Interrupt request register 150	IR150	8	8	2 ICLK
0008 7097h	ICU	Interrupt request register 151	IR151	8	8	2 ICLK
0008 7098h	ICU	Interrupt request register 152	IR152	8	8	2 ICLK
0008 709Ah	ICU	Interrupt request register 154	IR154	8	8	2 ICLK
0008 709Bh	ICU	Interrupt request register 155	IR155	8	8	2 ICLK
0008 709Ch	ICU	Interrupt request register 156	IR156	8	8	2 ICLK
0008 709Dh	ICU	Interrupt request register 157	IR157	8	8	2 ICLK
0008 709Eh	ICU	Interrupt request register 158	IR158	8	8	2 ICLK
0008 709Fh	ICU	Interrupt request register 159	IR159	8	8	2 ICLK

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 802Bh	WDT	Reset control/status register	RSTCSR	8	8	2 to 3 PCLK *7
0008 8040h	AD0	A/D data register A	ADDRA	16	16	2 to 3 PCLK *7
0008 8042h	AD0	A/D data register B	ADDRB	16	16	2 to 3 PCLK *7
0008 8044h	AD0	A/D data register C	ADDRC	16	16	2 to 3 PCLK *7
0008 8046h	AD0	A/D data register D	ADDRD	16	16	2 to 3 PCLK *7
0008 8050h	AD0	A/D control/status register	ADCSR	8	8	2 to 3 PCLK *7
0008 8051h	AD0	A/D control register	ADCR	8	8	2 to 3 PCLK *7
0008 8052h	AD0	ADDRy format select register	ADDPR	8	8	2 to 3 PCLK *7
0008 8053h	AD0	A/D sampling state register	ADSSTR	8	8	2 to 3 PCLK *7
0008 8060h	AD1	A/D data register A	ADDRA	16	16	2 to 3 PCLK *7
0008 8062h	AD1	A/D data register B	ADDRB	16	16	2 to 3 PCLK *7
0008 8064h	AD1	A/D data register C	ADDRC	16	16	2 to 3 PCLK *7
0008 8066h	AD1	A/D data register D	ADDRD	16	16	2 to 3 PCLK *7
0008 8070h	AD1	A/D control/status register	ADCSR	8	8	2 to 3 PCLK *7
0008 8071h	AD1	A/D control register	ADCR	8	8	2 to 3 PCLK *7
0008 8072h	AD1	ADDRy format select register	ADDPR	8	8	2 to 3 PCLK *7
0008 8073h	AD1	A/D sampling state register	ADSSTR	8	8	2 to 3 PCLK *7
0008 8080h	AD2	A/D data register A	ADDRA	16	16	2 to 3 PCLK *7
0008 8082h	AD2	A/D data register B	ADDRB	16	16	2 to 3 PCLK *7
0008 8084h	AD2	A/D data register C	ADDRC	16	16	2 to 3 PCLK *7
0008 8086h	AD2	A/D data register D	ADDRD	16	16	2 to 3 PCLK *7
0008 8090h	AD2	A/D control/status register	ADCSR	8	8	2 to 3 PCLK *7
0008 8091h	AD2	A/D control register	ADCR	8	8	2 to 3 PCLK *7
0008 8092h	AD2	ADDRy format select register	ADDPR	8	8	2 to 3 PCLK *7
0008 8093h	AD2	A/D sampling state register	ADSSTR	8	8	2 to 3 PCLK *7
0008 80A0h	AD3	A/D data register A	ADDRA	16	16	2 to 3 PCLK *7
0008 80A2h	AD3	A/D data register B	ADDRB	16	16	2 to 3 PCLK *7
0008 80A4h	AD3	A/D data register C	ADDRC	16	16	2 to 3 PCLK *7
0008 80A6h	AD3	A/D data register D	ADDRD	16	16	2 to 3 PCLK *7
0008 80B0h	AD3	A/D control/status register	ADCSR	8	8	2 to 3 PCLK *7
0008 80B1h	AD3	A/D control register	ADCR	8	8	2 to 3 PCLK *7
0008 80B2h	AD3	ADDRy format select register	ADDPR	8	8	2 to 3 PCLK *7
0008 80B3h	AD3	A/D sampling state register	ADSSTR	8	8	2 to 3 PCLK *7
0008 80C0h	D/A	D/A data register 0	DADR0	16	16	2 to 3 PCLK *7
0008 80C2h	D/A	D/A data register 1	DADR1	16	16	2 to 3 PCLK *7
0008 80C4h	D/A	D/A control register	DACR	8	8	2 to 3 PCLK *7
0008 80C5h	D/A	DADRy format select register	DADPR	8	8	2 to 3 PCLK *7
0008 8100h	TPU (unit 0)	Timer start register	TSTRA	8	8	2 to 3 PCLK *7
0008 8101h	TPU (unit 0)	Timer synchronous register	TSYRA	8	8	2 to 3 PCLK *7
0008 8110h	TPU0	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8111h	TPU0	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8112h	TPU0	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK *7
0008 8113h	TPU0	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK *7
0008 8114h	TPU0	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8115h	TPU0	Timer status register	TSR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8116h	TPU0	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8118h	TPU0	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 811Ah	TPU0	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 811Ch	TPU0	Timer general register C	TGRC	16	16	2 to 3 PCLK *7
0008 811Eh	TPU0	Timer general register D	TGRD	16	16	2 to 3 PCLK *7
0008 8120h	TPU1	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8121h	TPU1	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8122h	TPU1	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8124h	TPU1	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8125h	TPU1	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8126h	TPU1	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8128h	TPU1	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 812Ah	TPU1	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 8130h	TPU2	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8131h	TPU2	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8132h	TPU2	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8134h	TPU2	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8135h	TPU2	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8136h	TPU2	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8138h	TPU2	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 813Ah	TPU2	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 8140h	TPU3	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8141h	TPU3	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8142h	TPU3	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK *7
0008 8143h	TPU3	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK *7
0008 8144h	TPU3	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8145h	TPU3	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8146h	TPU3	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8148h	TPU3	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 814Ah	TPU3	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 814Ch	TPU3	Timer general register C	TGRC	16	16	2 to 3 PCLK *7
0008 814Eh	TPU3	Timer general register D	TGRD	16	16	2 to 3 PCLK *7
0008 8150h	TPU4	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8151h	TPU4	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8152h	TPU4	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8154h	TPU4	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8155h	TPU4	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8156h	TPU4	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8158h	TPU4	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 815Ah	TPU4	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 8160h	TPU5	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8161h	TPU5	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8162h	TPU5	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8164h	TPU5	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8165h	TPU5	Timer status register	TSR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8166h	TPU5	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8168h	TPU5	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 816Ah	TPU5	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 8170h	TPU (unit 1)	Timer start register	TSTRB	8	8	2 to 3 PCLK *7
0008 8171h	TPU (unit 1)	Timer synchronous register	TSYRB	8	8	2 to 3 PCLK *7
0008 8180h	TPU6	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8181h	TPU6	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8182h	TPU6	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK *7
0008 8183h	TPU6	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK *7
0008 8184h	TPU6	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8185h	TPU6	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8186h	TPU6	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8188h	TPU6	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 818Ah	TPU6	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 818Ch	TPU6	Timer general register C	TGRC	16	16	2 to 3 PCLK *7
0008 818Eh	TPU6	Timer general register D	TGRD	16	16	2 to 3 PCLK *7
0008 8190h	TPU7	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8191h	TPU7	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8192h	TPU7	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8194h	TPU7	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8195h	TPU7	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8196h	TPU7	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8198h	TPU7	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 819Ah	TPU7	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 81A0h	TPU8	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 81A1h	TPU8	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 81A2h	TPU8	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 81A4h	TPU8	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 81A5h	TPU8	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 81A6h	TPU8	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 81A8h	TPU8	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 81AAh	TPU8	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 81B0h	TPU9	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 81B1h	TPU9	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 81B2h	TPU9	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK *7
0008 81B3h	TPU9	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK *7
0008 81B4h	TPU9	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 81B5h	TPU9	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 81B6h	TPU9	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 81B8h	TPU9	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 81BAh	TPU9	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 81BCh	TPU9	Timer general register C	TGRC	16	16	2 to 3 PCLK *7
0008 81BEh	TPU9	Timer general register D	TGRD	16	16	2 to 3 PCLK *7
0008 81C0h	TPU10	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 81C1h	TPU10	Timer mode register	TMDR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C020h	P0	Data register	DR	8	8	2 to 3 PCLK *7
0008 C021h	P1	Data register	DR	8	8	2 to 3 PCLK *7
0008 C022h	P2	Data register	DR	8	8	2 to 3 PCLK *7
0008 C023h	P3	Data register	DR	8	8	2 to 3 PCLK *7
0008 C024h	P4	Data register	DR	8	8	2 to 3 PCLK *7
0008 C025h	P5	Data register	DR	8	8	2 to 3 PCLK *7
0008 C026h	P6	Data register	DR	8	8	2 to 3 PCLK *7
0008 C027h	P7	Data register	DR	8	8	2 to 3 PCLK *7
0008 C028h	P8	Data register	DR	8	8	2 to 3 PCLK *7
0008 C029h	P9	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Ah	PA	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Bh	PB	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Ch	PC	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Dh	PD	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Eh	PE	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Fh	PF	Data register	DR	8	8	2 to 3 PCLK *7
0008 C030h	PG	Data register	DR	8	8	2 to 3 PCLK *7
0008 C031h	PH	Data register	DR	8	8	2 to 3 PCLK *7
0008 C040h	P0	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C041h	P1	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C042h	P2	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C043h	P3	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C044h	P4	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C045h	P5	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C046h	P6	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C047h	P7	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C048h	P8	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C049h	P9	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Ah	PA	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Bh	PB	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Ch	PC	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Dh	PD	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Eh	PE	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Fh	PF	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C050h	PG	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C051h	PH	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C060h	P0	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C061h	P1	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C062h	P2	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C063h	P3	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C064h	P4	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C065h	P5	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C066h	P6	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C067h	P7	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C068h	P8	Input buffer control register	ICR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C29Ch	SYSTEM	Deep standby backup register 12	DPSBKR12	8	8	4 to 5 PCLK *7
0008 C29Dh	SYSTEM	Deep standby backup register 13	DPSBKR13	8	8	4 to 5 PCLK *7
0008 C29Eh	SYSTEM	Deep standby backup register 14	DPSBKR14	8	8	4 to 5 PCLK *7
0008 C29Fh	SYSTEM	Deep standby backup register 15	DPSBKR15	8	8	4 to 5 PCLK *7
0008 C2A0h	SYSTEM	Deep standby backup register 16	DPSBKR16	8	8	4 to 5 PCLK *7
0008 C2A1h	SYSTEM	Deep standby backup register 17	DPSBKR17	8	8	4 to 5 PCLK *7
0008 C2A2h	SYSTEM	Deep standby backup register 18	DPSBKR18	8	8	4 to 5 PCLK *7
0008 C2A3h	SYSTEM	Deep standby backup register 19	DPSBKR19	8	8	4 to 5 PCLK *7
0008 C2A4h	SYSTEM	Deep standby backup register 20	DPSBKR20	8	8	4 to 5 PCLK *7
0008 C2A5h	SYSTEM	Deep standby backup register 21	DPSBKR21	8	8	4 to 5 PCLK *7
0008 C2A6h	SYSTEM	Deep standby backup register 22	DPSBKR22	8	8	4 to 5 PCLK *7
0008 C2A7h	SYSTEM	Deep standby backup register 23	DPSBKR23	8	8	4 to 5 PCLK *7
0008 C2A8h	SYSTEM	Deep standby backup register 24	DPSBKR24	8	8	4 to 5 PCLK *7
0008 C2A9h	SYSTEM	Deep standby backup register 25	DPSBKR25	8	8	4 to 5 PCLK *7
0008 C2AAh	SYSTEM	Deep standby backup register 26	DPSBKR26	8	8	4 to 5 PCLK *7
0008 C2ABh	SYSTEM	Deep standby backup register 27	DPSBKR27	8	8	4 to 5 PCLK *7
0008 C2ACh	SYSTEM	Deep standby backup register 28	DPSBKR28	8	8	4 to 5 PCLK *7
0008 C2ADh	SYSTEM	Deep standby backup register 29	DPSBKR29	8	8	4 to 5 PCLK *7
0008 C2AEh	SYSTEM	Deep standby backup register 30	DPSBKR30	8	8	4 to 5 PCLK *7
0008 C2AFh	SYSTEM	Deep standby backup register 31	DPSBKR31	8	8	4 to 5 PCLK *7
0008 C300h	ICU	IRQ detection enable registrar 0	IRQER0	8	8	2 to 3 PCLK *7
0008 C301h	ICU	IRQ detection enable registrar 1	IRQER1	8	8	2 to 3 PCLK *7
0008 C302h	ICU	IRQ detection enable registrar 2	IRQER2	8	8	2 to 3 PCLK *7
0008 C303h	ICU	IRQ detection enable registrar 3	IRQER3	8	8	2 to 3 PCLK *7
0008 C304h	ICU	IRQ detection enable registrar 4	IRQER4	8	8	2 to 3 PCLK *7
0008 C305h	ICU	IRQ detection enable registrar 5	IRQER5	8	8	2 to 3 PCLK *7
0008 C306h	ICU	IRQ detection enable registrar 6	IRQER6	8	8	2 to 3 PCLK *7
0008 C307h	ICU	IRQ detection enable registrar 7	IRQER7	8	8	2 to 3 PCLK *7
0008 C308h	ICU	IRQ detection enable registrar 8	IRQER8	8	8	2 to 3 PCLK *7
0008 C309h	ICU	IRQ detection enable registrar 9	IRQER9	8	8	2 to 3 PCLK *7
0008 C30Ah	ICU	IRQ detection enable registrar 10	IRQER10	8	8	2 to 3 PCLK *7
0008 C30Bh	ICU	IRQ detection enable registrar 11	IRQER11	8	8	2 to 3 PCLK *7
0008 C30Ch	ICU	IRQ detection enable registrar 12	IRQER12	8	8	2 to 3 PCLK *7
0008 C30Dh	ICU	IRQ detection enable registrar 13	IRQER13	8	8	2 to 3 PCLK *7
0008 C30Eh	ICU	IRQ detection enable registrar 14	IRQER14	8	8	2 to 3 PCLK *7
0008 C30Fh	ICU	IRQ detection enable registrar 15	IRQER15	8	8	2 to 3 PCLK *7
0008 C320h	ICU	IRQ control register 0	IRQCR0	8	8	2 to 3 PCLK *7
0008 C321h	ICU	IRQ control register 1	IRQCR1	8	8	2 to 3 PCLK *7
0008 C322h	ICU	IRQ control register 2	IRQCR2	8	8	2 to 3 PCLK *7
0008 C323h	ICU	IRQ control register 3	IRQCR3	8	8	2 to 3 PCLK *7
0008 C324h	ICU	IRQ control register 4	IRQCR4	8	8	2 to 3 PCLK *7
0008 C325h	ICU	IRQ control register 5	IRQCR5	8	8	2 to 3 PCLK *7
0008 C326h	ICU	IRQ control register 6	IRQCR6	8	8	2 to 3 PCLK *7
0008 C327h	ICU	IRQ control register 7	IRQCR7	8	8	2 to 3 PCLK *7
0008 C328h	ICU	IRQ control register 8	IRQCR8	8	8	2 to 3 PCLK *7

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}, $PLLV_{CC}$	-0.3 to +4.6	V
Input voltage (except for ports 0, 14 to 17)	V_{in}	-0.3 to V_{CC} +0.3	V
Input voltage (ports 0, 14 to 17*1)	V_{in}	-0.3 to +6.5	V
Reference power supply voltage	V_{REFH}	-0.3 to V_{CC} +0.3	V
Analog power supply voltage	AV_{CC}*2	-0.3 to +4.6	V
Analog input voltage	V_{AN}	-0.3 to V_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: -20 to +85	°C
		Wide-range specifications: -40 to +85	
Storage temperature	T_{stg}	-55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Notes: 1. Ports 0, and 14 to 17 are 5 V tolerant.

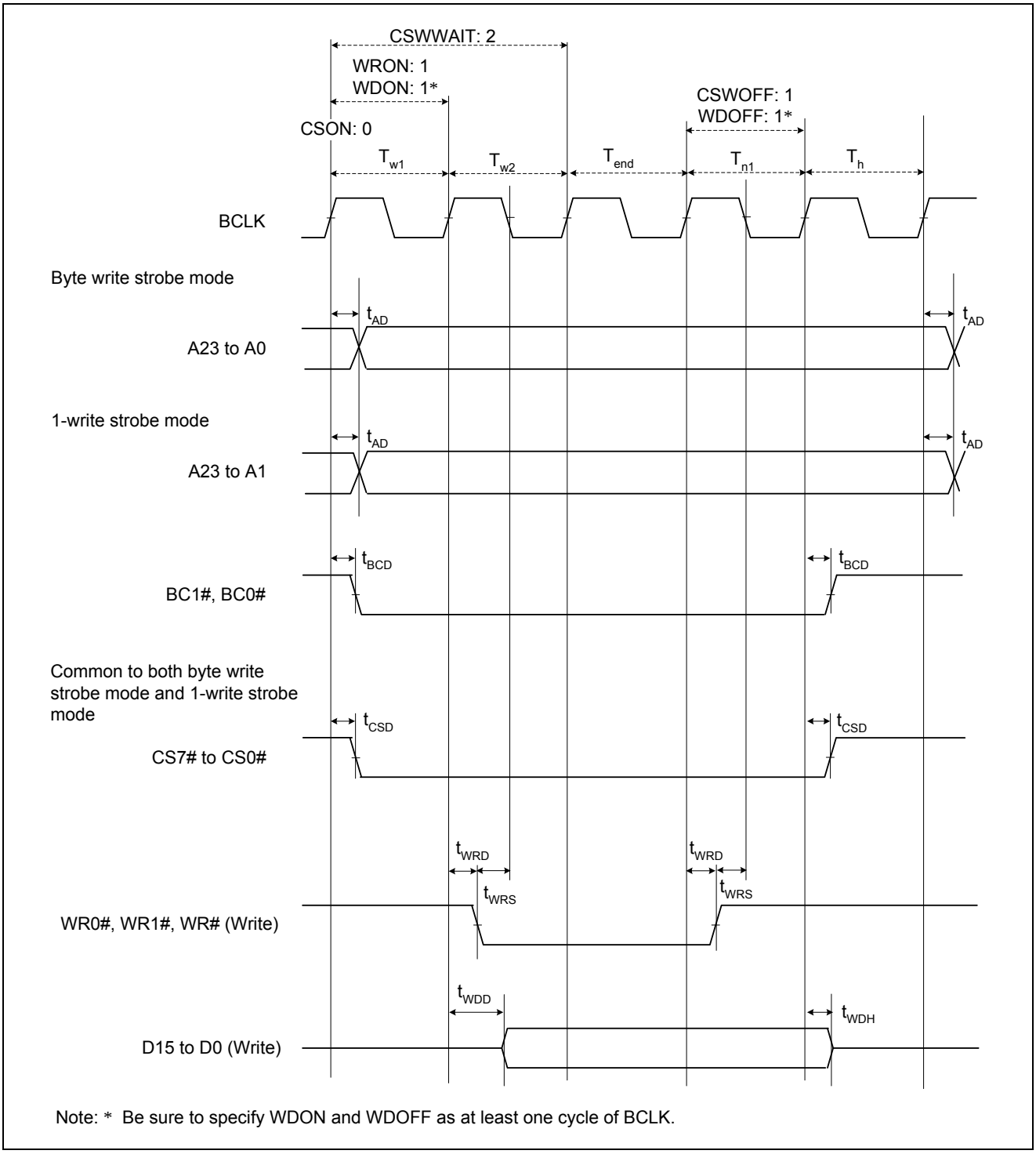
2. Connect AV_{CC} to V_{CC}. When neither the A/D converter nor the D/A converter is in use, do not leave the AV_{SS}, V_{REFH}, and V_{REFL} pins open. Connect the AV_{CC} and V_{REFH} pins to V_{CC}, and the AV_{SS} and V_{REFL} pins to V_{SS}, respectively.

5.2 DC Characteristics

Table 5.2 DC Characteristics

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin*1 TPU input pin*1 TMR input pin*1 SCI input pin*1 ADTRG# input pin*1 RES#, NMI	V_{IH}	V_{CC} x 0.8	—	V_{CC} + 0.3	V	
		V_{IL}	-0.3	—	V_{CC} x 0.2		
		ΔV_T	V_{CC} x 0.06	—	—		
	RIIC input pin	V_{IH}	V_{CC} x 0.7	—	5.8		
		V_{IL}	-0.3	—	V_{CC} x 0.3		
		ΔV_T	V_{CC} x 0.05	—	—		
	Ports 0, 14 to 17*2	V_{IH}	V_{CC} x 0.8	—	5.8		
		V_{IL}	-0.3	—	V_{CC} x 0.2		
	Ports 10 to 13, ports 2 to E (144-pin LQFP) ports 2 to H (176-pin LFBGA) Other input pins	V_{IH}	V_{CC} x 0.8	—	V_{CC} + 0.3		
		V_{IL}	-0.3	—	V_{CC} x 0.2		
Input high voltage (except Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	V_{CC} x 0.9	—	V_{CC} + 0.3	V	
	EXTAL		V_{CC} x 0.8	—	V_{CC} + 0.3		
	D0 to D15		V_{CC} x 0.7	—	V_{CC} + 0.3		
Input low voltage (except Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	-0.3	—	V_{CC} x 0.1	V	
	EXTAL		-0.3	—	V_{CC} x 0.2		
	D0 to D15		-0.3	—	V_{CC} x 0.3		
Output high voltage	All output pins	V_{OH}	V_{CC}-0.5	—	—	V	I_{OH} = -1 mA
Output low voltage	All output pins (except for RIIC pins)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	RIIC pins		—	—	0.4		I_{OL} = 3.0 mA
			—	—	0.6		I_{OL} = 6.0 mA
	RIIC pins (only P14 and P15 in channel 1)		—	—	0.4		I_{OL} = 15 mA (ICFER.FMPE = 1)
			—	0.4	—		I_{OL} = 20 mA (ICFER.FMPE = 1)
Input leakage current	RES#, MD pin, EMLE, NMI	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, V_{CC}
Three-state leakage current (off state)	Ports 10 to 13, ports 2 to E (144-pin LQFP) ports 2 to H (176-pin LFBGA)	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, V_{CC}
	Port 0, ports 14 to 17		—	—	5.0		



Note: * Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 5.10 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

Table 5.8 Timing of On-Chip Peripheral Modules (3)

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V,
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item		Symbol	Min. *1*2	Max.	Unit	Test Conditions
RIIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	8(10) x (1/PCLK) + 240	—	ns	Figure 5.25
	SCL input high pulse width	t_{SCLH}	3(5) x (1/PCLK) + 120	—	ns	
	SCL input low pulse width	t_{SCLL}	5 x (1/PCLK) + 120	—	ns	
	SCL, SDA input rising time	t_{Sr}	—	120	ns	
	SCL, SDA input falling time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 x (1/PCLK)	ns	
	SDA input bus free time	t_{BUF}	5 x (1/PCLK) + 120	—	ns	
	Start condition input hold time	t_{STAH}	3(5) x (1/PCLK) + 120	—	ns	
	Re-start condition input setup time	t_{STAS}	5 x (1/PCLK) + 120	—	ns	
	Stop condition input setup time	t_{STOS}	3(5) x (1/PCLK) + 120	—	ns	
	Data input setup time	t_{SDAS}	50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	550	pF	
Boundary scan (176-pin LFBGA)	TCK clock cycle time	tTCKcyc	100	—	ns	Figure 5.26
	TCK clock high level pulse width	tTCKH	45	—	ns	
	TCK clock low level pulse width	tTCKL	45	—	ns	
	TCK clock rising time	tTCKr	—	5	ns	
	TCK clock falling time	tTCKf	—	5	ns	
	TRST# pulse width	tTRSTW	20	—	Tcyc	Figure 5.27
	TMS setup time	tTMSS	20	—	ns	Figure 5.28
	TMS hold time	tTMSH	20	—	ns	
	TDI setup time	tTDIS	20	—	ns	
	TDI hold time	tTDIH	20	—	ns	
	TDO data delay time	tTDOD	—	40	ns	

Notes:1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.

2. Cb indicates the total capacity of the bus line.

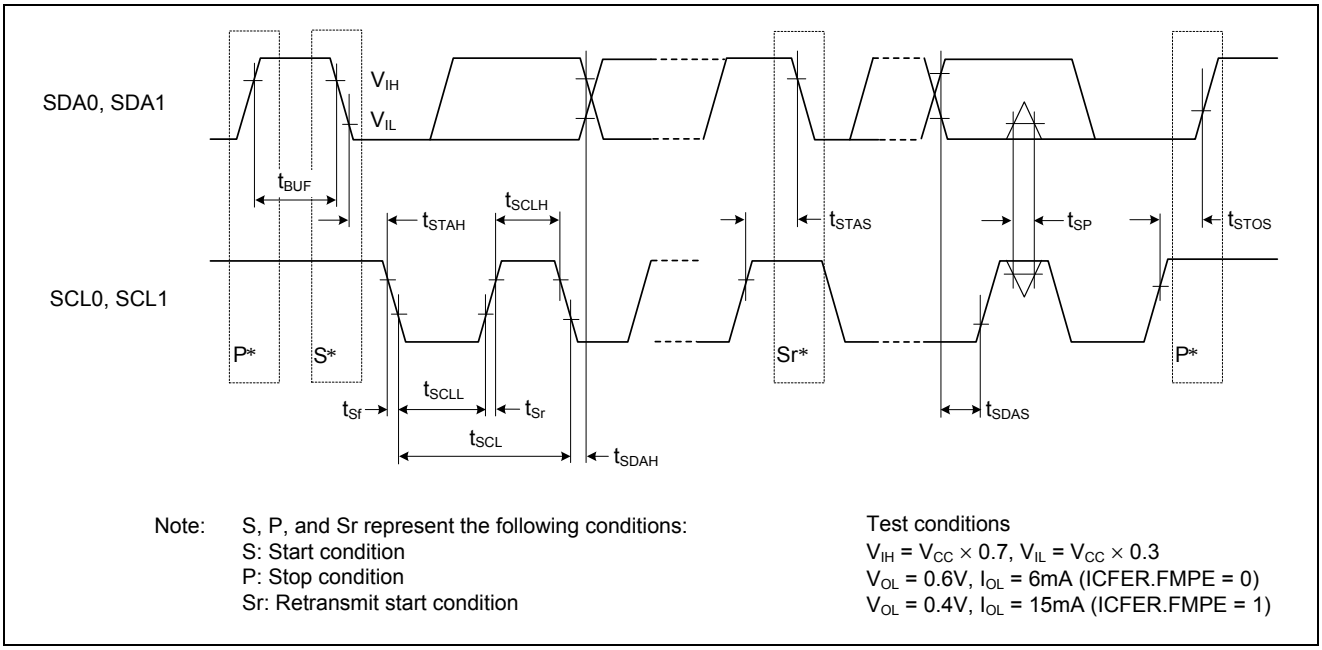


Figure 5.25 I²C Bus Interface Input/Output Timing

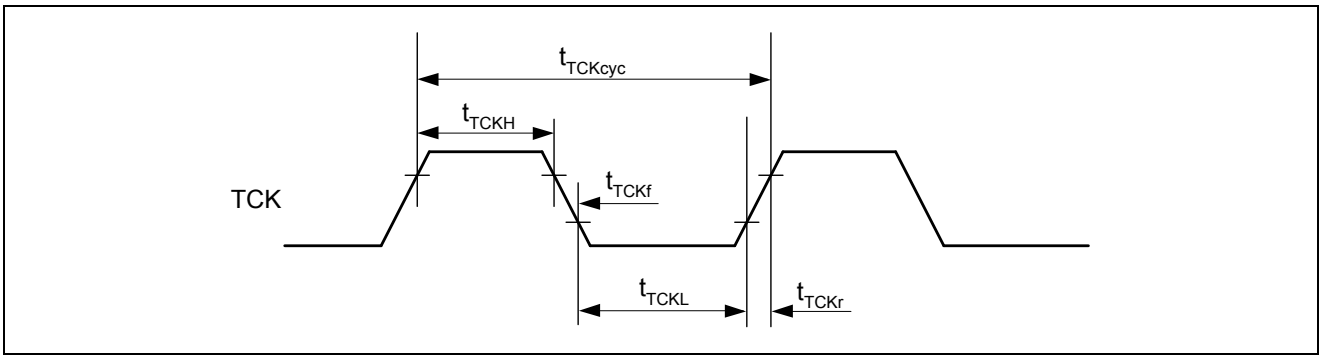


Figure 5.26 Boundary Scan TCK Timing

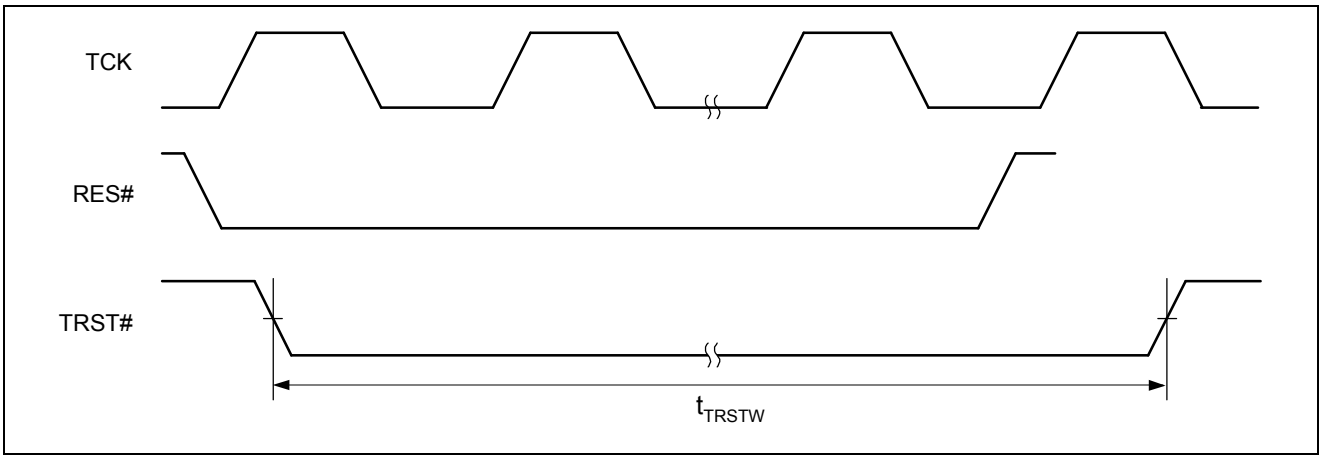


Figure 5.27 Boundary Scan TRST# Timing

5.6 ROM (Flash Memory for Code Storage) Characteristics

Table 5.11 ROM (Flash Memory for Code Storage) Characteristics

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V
Operating temperature range during programming/erasing:
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

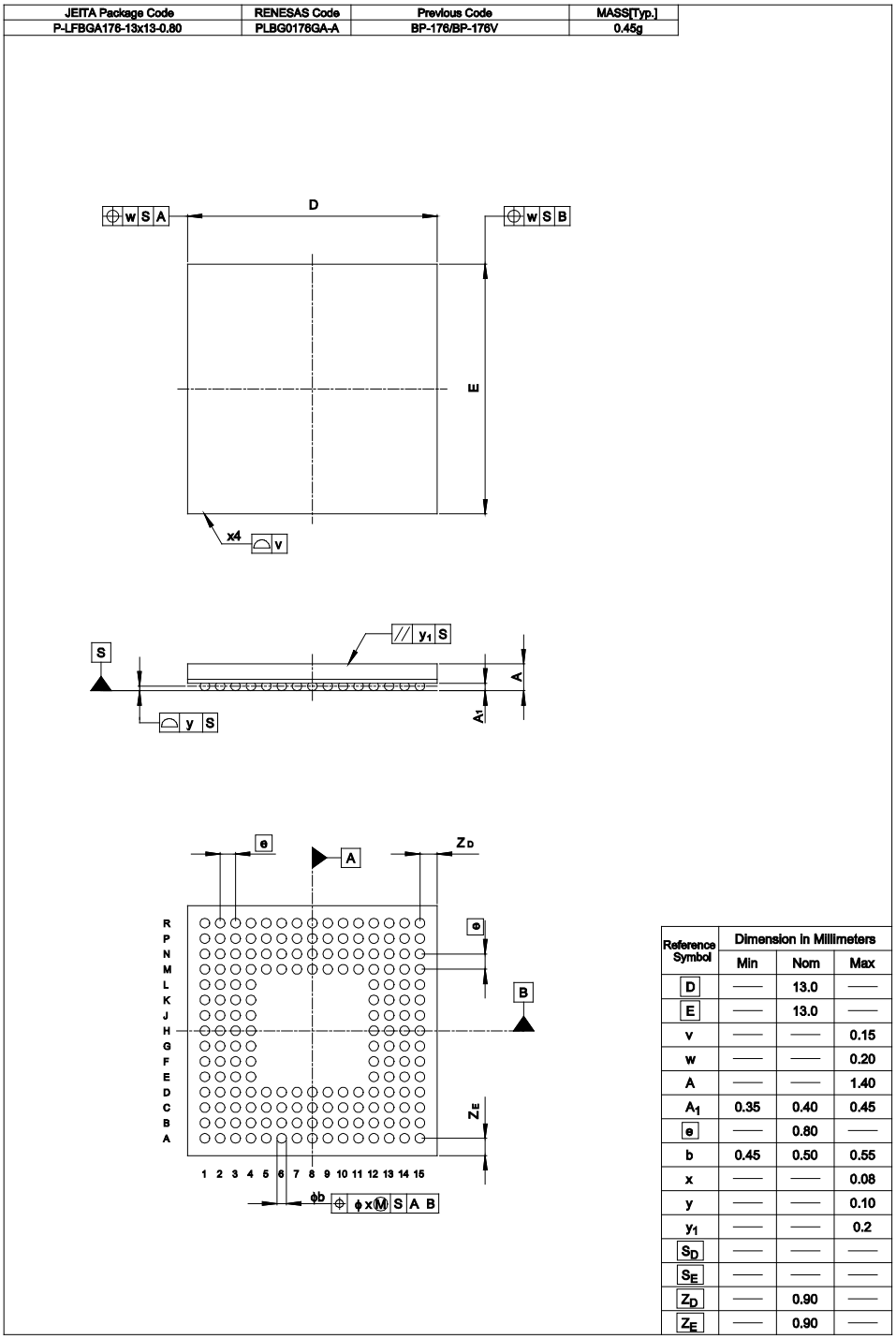
Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time	256 bytes	t_{P256}	—	2	12	ms	PCLK = 50 MHz $N_{PEC} \leq 100$
	8 Kbytes	t_{P8K}	—	45	100	ms	
	256 bytes	t_{P256}	—	2.4	14.4	ms	PCLK = 50 MHz $N_{PEC} > 100$
	8 Kbytes	t_{P8K}	—	54	120	ms	
Erasure time	8 Kbytes	t_{E8K}	—	50	120	ms	PCLK = 50 MHz $N_{PEC} \leq 100$
	64 Kbytes	t_{E64K}	—	400	875	ms	
	128 Kbytes	t_{E128K}	—	800	1750	ms	
	8 Kbytes	t_{E8K}	—	60	144	ms	PCLK = 50 MHz $N_{PEC} > 100$
	64 Kbytes	t_{E64K}	—	480	1050	ms	
	128 Kbytes	t_{E128K}	—	960	2100	ms	
Rewrite/erase cycle*[1]		N_{PEC}	1000*[2]	—	—	Times	
Suspend delay time during writing		t_{SPD}	—	—	120	µs	Figure 5.29 PCLK = 50 MHz
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t_{SEED}	—	—	1.7	ms	
Data hold time*[3]		T_{DRP}	10	—	—	Year	

Notes: 1. Definition of rewrite/erase cycle:
The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte writing is performed 32 times for different addresses in 8-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (over writing is prohibited).
2. This indicates the minimum number that guarantees the characteristics after rewriting. (The guaranteed value is in the range from one to the minimum number.)
3. This indicates the characteristic when rewrite is performed within the specification range including the minimum number.

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in "Packages" on Renesas Technology Corp. website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA176-13x13-0.80	PLBG0176GA-A	BP-176/BP-176V	0.45g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	13.0	—
E	—	13.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.90	—
Z_E	—	0.90	—

176-pin LFBGA (PLBG0176GA-A)