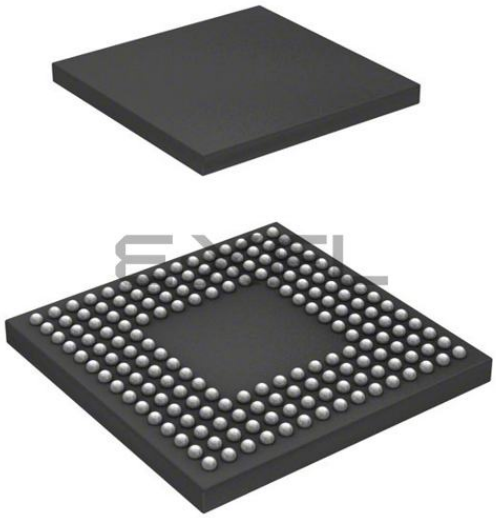
Renesas Electronics America Inc - R5F56108WDBG#U0 Datasheet



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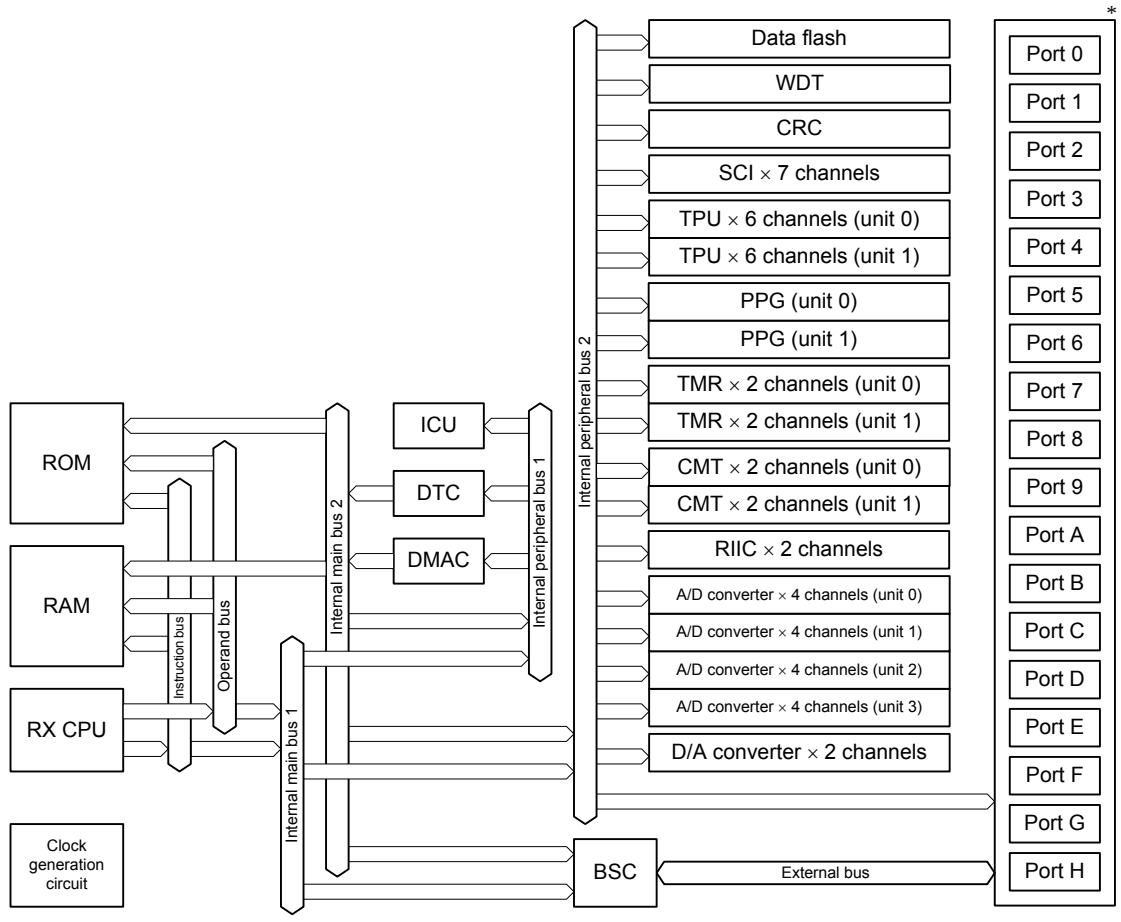
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	140
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 2x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56108wdbg-u0

1.3 Block Diagram

Figure 1.2 shows a block diagram of the RX610 Group.



[Legend]

ICU:	Interrupt control unit	SCI:	Serial communications interfaces
DTC:	Data transfer controller	TPU:	16-bit timer pulse unit
DMAC:	DMA controller	PPG:	Programmable pulse generator
BSC:	Bus controller	TMR:	8-bit timer
WDT:	Watchdog timer	CMT:	Compare match timer
CRC:	CRC (Cyclic Redundancy Check) calculator	RIIC:	I^2C bus interface

Note: * Ports F and H are not included in the 144-pin LQFP package.

Figure 1.2 Block Diagram

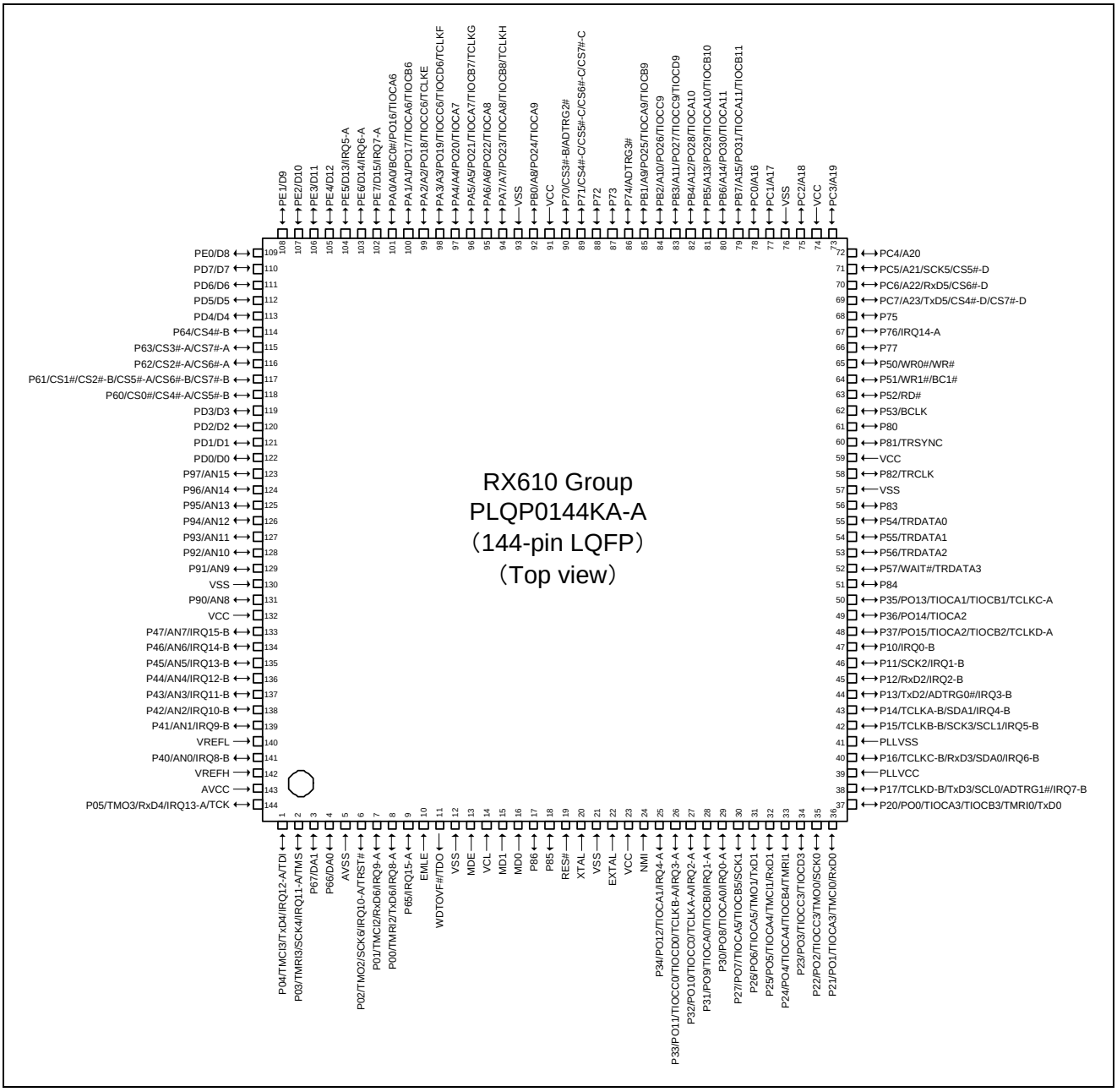


Figure 1.4 Pin Assignment of the 144-Pin LQFP

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
C6	VSS							
C7		P94					AN12	
C8	BSCANP							
C9		PG3						
C10		PD2		D2				
C11		P62		CS2#-A/ CS6#-A				
C12	VSS							
C13		PD7		D7				
C14		PE3		D11				
C15		PE5	IRQ5-A	D13				
D1		P65	IRQ15-A					
D2		P01	IRQ9-A		TMCI2	RxD6		
D3	AVSS							
D4		P40	IRQ8-B				AN0	
D5		P44	IRQ12-B				AN4	
D6		P91					AN9	
D7		P95					AN13	
D8		PG0						
D9		PG4						
D10		PD3		D3				
D11		P64		CS4#-B				
D12		PE4		D12				
D13		PE6	IRQ6-A	D14				
D14		PE7	IRQ7-A	D15				
D15		PG5						
E1	VSS							
E2	WDTOVF#							TDO
E3	EMLE							
E4		P00	IRQ8-A		TMRI2	TxD6		
E12	VCC							
E13		PG7						
E14		PG6						
E15	VSS							
F1	MD1							
F2	MD0							
F3	VCL							
F4	MDE							
F12		PA3		A3	PO19/ TIOCC6/ TIOCD6/ TCLKF			

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
M6		P37			PO15/ TIOCA2/ TIOCB2/ TCLKD-A			
M7		P57		WAIT#				TRDATA3
M8		P83						
M9		P81						TRSYNC
M10		P51		WR1#/BC1#				
M11		PH4						
M12		PC7		A23/ CS4#-D/ CS7#-D		TxD5		
M13	VSS							
M14		PC0		A16				
M15		PB6		A14	PO30/ TIOCA11			
N1		P25			PO5/ TIOCA4/ TMCI1	RxD1		
N2		P24			PO4/ TIOCA4/ TIOCB4/ TMRI1			
N3		P20			PO0/ TIOCA3/ TIOCB3/ TMRI0	TxD0		
N4		P16	IRQ6-B		TCLKC-B	RxD3/SDA0		
N5		P12	IRQ2-B			RxD2		
N6		P36			PO14/ TIOCA2			
N7		P56						TRDATA2
N8	VSS							
N9		P80						
N10		P50		WR0#/WR#				
N11	VSS							
N12		P76	IRQ14-A					
N13		PH2						
N14		PC2		A18				
N15		PC1		A17				
P1		P23			PO3/ TIOCC3/ TIOCD3			

Table 1.4 List of Pins and Pin Functions (144-Pin LQFP)

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
1		P04	IRQ12-A		TMCI3	TxD4		TDI
2		P03	IRQ11-A		TMRI3	SCK4		TMS
3		P67					DA1	
4		P66					DA0	
5	AVSS							
6		P02	IRQ10-A		TMO2	SCK6		TRST#
7		P01	IRQ9-A		TMCI2	RxD6		
8		P00	IRQ8-A		TMRI2	TxD6		
9		P65	IRQ15-A					
10	EMLE							
11	WDTOVF#							TDO
12	VSS							
13	MDE							
14	VCL							
15	MD1							
16	MD0							
17		P86						
18		P85						
19	RES#							
20	XTAL							
21	VSS							
22	EXTAL							
23	VCC							
24			NMI					
25		P34	IRQ4-A		PO12/ TIOCA1			
26		P33	IRQ3-A		PO11/ TIOCC0/ TIOCD0/ TCLKB-A			
27		P32	IRQ2-A		PO10/ TIOCC0/ TCLKA-A			
28		P31	IRQ1-A		PO9/ TIOCA0/ TIOCB0			
29		P30	IRQ0-A		PO8/ TIOCA0			
30		P27			PO7/ TIOCA5/ TIOCB5	SCK1		
31		P26			PO6/ TIOCA5/ TMO1	TxD1		

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
85		PB1		A9	PO25/ TIOCA9/ TIOCB9			
86		P74					ADTRG3#	
87		P73						
88		P72						
89		P71		CS4#-C/ CS5#-C/ CS6#-C/ CS7#-C				
90		P70		CS3#-B			ADTRG2#	
91	VCC							
92		PB0		A8	PO24/ TIOCA9			
93	VSS							
94		PA7		A7	PO23/ TIOCA8/ TIOCB8/ TCLKH			
95		PA6		A6	PO22/ TIOCA8			
96		PA5		A5	PO21/ TIOCA7/ TIOCB7/ TCLKG			
97		PA4		A4	PO20/ TIOCA7			
98		PA3		A3	PO19/ TIOCC6/ TIOCD6/ TCLKF			
99		PA2		A2	PO18/ TIOCC6/ TCLKE			
100		PA1		A1	PO17/ TIOCA6/ TIOCB6			
101		PA0		A0/BC0#	PO16/ TIOCA6			
102		PE7	IRQ7-A	D15				
103		PE6	IRQ6-A	D14				
104		PE5	IRQ5-A	D13				
105		PE4		D12				
106		PE3		D11				
107		PE2		D10				

1.5 Pin Functions

Table 1.5 lists the pin functions.

Table 1.5 Pin Functions

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	Input	Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	PLLVCC	Input	Power supply pin for the PLL circuit. Connect it to the system power supply.
	PLLVSS	Input	Ground pin for the PLL circuit
Clock	XTAL	Input	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the system clock for external devices.
Operating mode control	MD0, MD1, MDE	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	Input pin to enable on-chip emulator signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
	BSCANP	Input	Input pin to enable boundary-scan signal. When this pin is driven high, the boundary scan is enabled. When the boundary scan is not used, this pin should be driven low.
On-chip emulator	TRST#	Input	On-chip emulator pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid.
	TRDATA0 to TRDATA3	Output	These pins output the trace information.
Address bus	A0 to A23*1	Output	Output pins for the address
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus

Classifications	Pin Name	I/O	Description
Analog power supply	AVCC	Input	Analog power supply pin for the A/D and D/A converters. When the A/D and D/A converters are not in use, connect this pin to the system power supply.
	AVSS	Input	Ground pin for the A/D and D/A converters. Connect this pin to the system power supply (0 V).
	VREFH	Input	Reference power supply pin for the A/D and D/A converters. When the A/D and D/A converters are not in use, connect this pin to the system power supply.
	VREFL	Input	Reference ground pin for the A/D and D/A converters. Make sure to connect this pin to the analog reference power supply (0 V). When the A/D and D/A converters are not in use, connect this pin to the system power supply (0 V). For details, see section 23.6.7, Ranges of Settings for Analog Power Supply and Other Pins.
I/O ports	P00 to P05	I/O	6-bit input/output pins
	P10 to P17	I/O	8-bit input/output pins
	P20 to P27	I/O	8-bit input/output pins
	P30 to P37	I/O	8-bit input/output pins
	P40 to P47	I/O	8-bit input/output pins
	P50 to P57	I/O	8-bit input/output pins. (P53 is an input-only pin.)
	P60 to P67	I/O	8-bit input/output pins
	P70 to P77	I/O	8-bit input/output pins
	P80 to P86	I/O	7-bit input/output pins
	P90 to P97	I/O	8-bit input/output pins
	PA0 to PA7	I/O	8-bit input/output pins
	PB0 to PB7	I/O	8-bit input/output pins
	PC0 to PC7	I/O	8-bit input/output pins
	PD0 to PD7	I/O	8-bit input/output pins
	PE0 to PE7	I/O	8-bit input/output pins
	PF0 to PF6	I/O	7-bit input/output pins
	PG0 to PG7	I/O	8-bit input/output pins
	PH0 to PH7	I/O	8-bit input/output pins

Note 1: The A0 and BC0# pin functions are multiplexed on the same pin: the A0 pin is valid in byte-write mode and the BC0# pin becomes valid in single write-strobe mode. The setting for an eight-bit external bus width is prohibited in single write-strobe mode. For other multiplexed pin functions, refer to section 14, I/O Ports.

Note 2: The BC0# and BC1# signals are valid in both reading and writing.

(8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.

When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the corresponding Cj flag indicates the source of the exception within the exception handling routine. If the exception handling is masked (Ej = 0), check the Fj flag at the end of a series of processing whether an exception is generated or not. The Fj flag is the accumulation type flag (j = X, U, Z, O, or V).

(9) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.

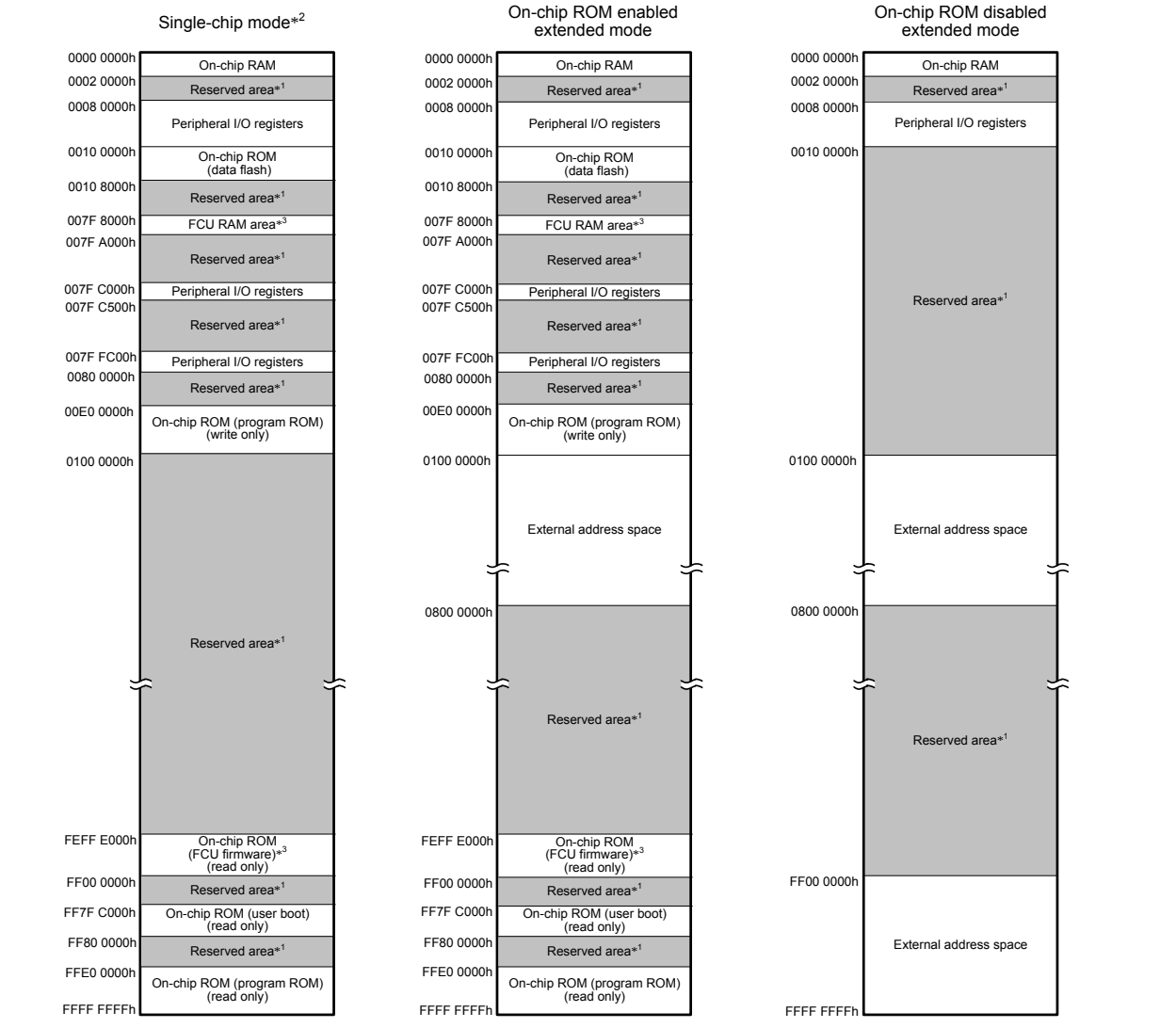
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

3. Address Space

3.1 Address Space

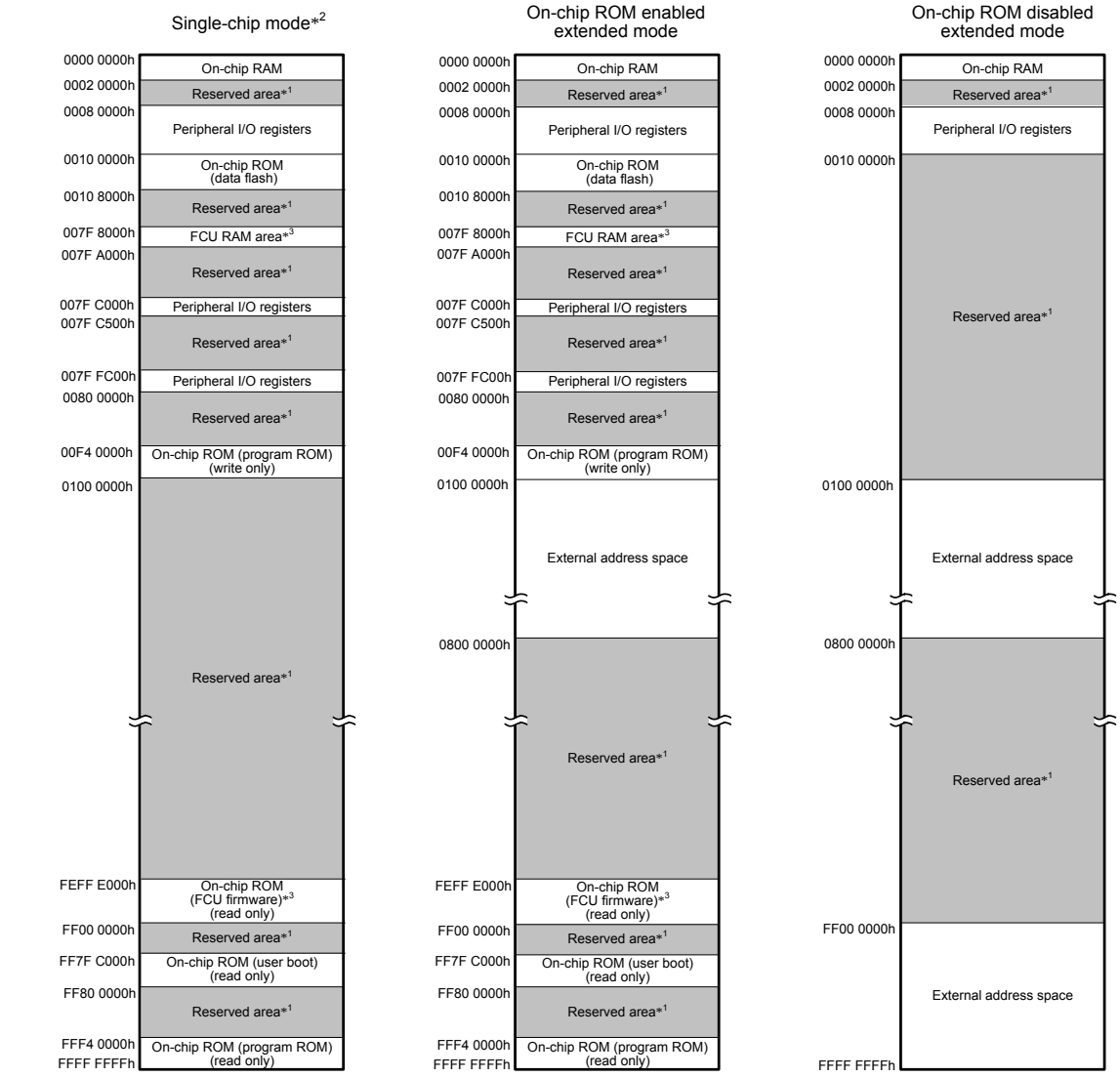
This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figures 3.1 to 3.4 show the memory maps in the respective operating modes of each product. Accessible areas will differ according to the operating mode and states of control bits.



Notes: 1. A reserved area should not be accessed.
2. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
3. For details on the FCU, see section 26, ROM (Flash Memory for Code Storage) and section 27, Data Flash (Flash Memory for Data Storage) in the User's manual: Hardware.

Figure 3.1 Memory Map of the R5F56108



Notes: 1. A reserved area should not be accessed.
2. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
3. For details on the FCU, see section 26, ROM (Flash Memory for Code Storage) and section 27, Data Flash (Flash Memory for Data Storage) in the User's manual: Hardware.

Figure 3.4 Memory Map of the R5F56104

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 820Ah	TMR0	Timer counter control register	TCCR	8	8 or 16	2 to 3 PCLK *7
0008 820Bh	TMR1	Timer counter control register	TCCR	8	8 or 16	2 to 3 PCLK *7
0008 8210h	TMR2	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8211h	TMR3	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8212h	TMR2	Timer control/status register	TCSR	8	8	2 to 3 PCLK *7
0008 8213h	TMR3	Timer control/status register	TCSR	8	8	2 to 3 PCLK *7
0008 8214h	TMR2	Time constant register A	TCORA	8	8 or 16	2 to 3 PCLK *7
0008 8215h	TMR3	Time constant register A	TCORA	8	8 or 16*5	2 to 3 PCLK *7
0008 8216h	TMR2	Time constant register B	TCORB	8	8 or 16	2 to 3 PCLK *7
0008 8217h	TMR3	Time constant register B	TCORB	8	8 or 16*5	2 to 3 PCLK *7
0008 8218h	TMR2	Timer counter	TCNT	8	8 or 16	2 to 3 PCLK *7
0008 8219h	TMR3	Timer counter	TCNT	8	8 or 16*5	2 to 3 PCLK *7
0008 821Ah	TMR2	Timer counter control register	TCCR	8	8 or 16	2 to 3 PCLK *7
0008 821Bh	TMR3	Timer counter control register	TCCR	8	8 or 16	2 to 3 PCLK *7
0008 8240h	SCI0	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8241h	SCI0	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 8242h	SCI0	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 8243h	SCI0	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 8244h	SCI0	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 8245h	SCI0	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 8246h	SCI0	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7
0008 8247h	SCI0	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8248h	SCI1	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8249h	SCI1	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 824Ah	SCI1	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 824Bh	SCI1	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 824Ch	SCI1	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 824Dh	SCI1	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 824Eh	SCI1	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7
0008 824Fh	SCI1	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8250h	SCI2	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8251h	SCI2	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 8252h	SCI2	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 8253h	SCI2	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 8254h	SCI2	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 8255h	SCI2	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 8256h	SCI2	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7
0008 8257h	SCI2	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8258h	SCI3	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8259h	SCI3	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 825Ah	SCI3	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 825Bh	SCI3	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 825Ch	SCI3	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 825Dh	SCI3	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 825Eh	SCI3	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 825Fh	SCI3	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8260h	SCI4	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8261h	SCI4	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 8262h	SCI4	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 8263h	SCI4	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 8264h	SCI4	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 8265h	SCI4	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 8266h	SCI4	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7
0008 8267h	SCI4	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8268h	SCI5	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8269h	SCI5	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 826Ah	SCI5	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 826Bh	SCI5	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 826Ch	SCI5	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 826Dh	SCI5	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 826Eh	SCI5	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7
0008 826Fh	SCI5	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8270h	SCI6	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8271h	SCI6	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 8272h	SCI6	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 8273h	SCI6	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 8274h	SCI6	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 8275h	SCI6	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 8276h	SCI6	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7
0008 8277h	SCI6	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8280h	CRC	CRC control register	CRCCR	8	8	2 to 3 PCLK *7
0008 8281h	CRC	CRC data input register	CRCDIR	8	8	2 to 3 PCLK *7
0008 8282h	CRC	CRC data output register	CRCDOR	16	16	2 to 3 PCLK *7
0008 8300h	RIIC0	I^2C bus control register 1	ICCR1	8	8	2 to 3 PCLK *7
0008 8301h	RIIC0	I^2C bus control register 2	ICCR2	8	8	2 to 3 PCLK *7
0008 8302h	RIIC0	I^2C bus mode register 1	ICMR1	8	8	2 to 3 PCLK *7
0008 8303h	RIIC0	I^2C bus mode register 2	ICMR2	8	8	2 to 3 PCLK *7
0008 8304h	RIIC0	I^2C bus mode register 3	ICMR3	8	8	2 to 3 PCLK *7
0008 8305h	RIIC0	I^2C bus function enable register	ICFER	8	8	2 to 3 PCLK *7
0008 8306h	RIIC0	I^2C bus status enable register	ICSER	8	8	2 to 3 PCLK *7
0008 8307h	RIIC0	I^2C bus interrupt enable register	ICIER	8	8	2 to 3 PCLK *7
0008 8308h	RIIC0	I^2C bus status register 1	ICSR1	8	8	2 to 3 PCLK *7
0008 8309h	RIIC0	I^2C bus status register 2	ICSR2	8	8	2 to 3 PCLK *7
0008 830Ah	RIIC0	Slave address register L0	SARL0	8	8	2 to 3 PCLK *7
0008 830Ah	RIIC0	Internal control for timeout L	TMOCNTL	16	16	2 to 3 PCLK *7
0008 830Bh	RIIC0	Slave address register U0	SARU0	8	8	2 to 3 PCLK *7
0008 830Bh	RIIC0	Internal control for timeout U	TMOCNTU	16	16	2 to 3 PCLK *7
0008 830Ch	RIIC0	Slave address register L1	SARL1	8	8	2 to 3 PCLK *7
0008 830Dh	RIIC0	Slave address register U1	SARU1	8	8	2 to 3 PCLK *7
0008 830Eh	RIIC0	Slave address register L2	SARL2	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 830Fh	RIIC0	Slave address register U2	SARU2	8	8	2 to 3 PCLK *7
0008 8310h	RIIC0	I²C bus bit rate low-level register	ICBRL	8	8	2 to 3 PCLK *7
0008 8311h	RIIC0	I²C bus bit rate high-level register	ICBRH	8	8	2 to 3 PCLK *7
0008 8312h	RIIC0	I²C bus transmit data register	ICDRT	8	8	2 to 3 PCLK *7
0008 8313h	RIIC0	I²C bus receive data register	ICDRR	8	8	2 to 3 PCLK *7
0008 8320h	RIIC1	I²C bus control register 1	ICCR1	8	8	2 to 3 PCLK *7
0008 8321h	RIIC1	I²C bus control register 2	ICCR2	8	8	2 to 3 PCLK *7
0008 8322h	RIIC1	I²C bus mode register 1	ICMR1	8	8	2 to 3 PCLK *7
0008 8323h	RIIC1	I²C bus mode register 2	ICMR2	8	8	2 to 3 PCLK *7
0008 8324h	RIIC1	I²C bus mode register 3	ICMR3	8	8	2 to 3 PCLK *7
0008 8325h	RIIC1	I²C bus function enable register	ICFER	8	8	2 to 3 PCLK *7
0008 8326h	RIIC1	I²C bus status enable register	ICSER	8	8	2 to 3 PCLK *7
0008 8327h	RIIC1	I²C bus interrupt enable register	ICIER	8	8	2 to 3 PCLK *7
0008 8328h	RIIC1	I²C bus status register 1	ICSR1	8	8	2 to 3 PCLK *7
0008 8329h	RIIC1	I²C bus status register 2	ICSR2	8	8	2 to 3 PCLK *7
0008 832Ah	RIIC1	Slave address register L0	SARL0	8	8	2 to 3 PCLK *7
0008 832Ah	RIIC1	Internal control for timeout L	TMOCNTL	16	16	2 to 3 PCLK *7
0008 832Bh	RIIC1	Slave address register U0	SARU0	8	8	2 to 3 PCLK *7
0008 832Bh	RIIC1	Internal control for timeout U	TMOCNTU	16	16	2 to 3 PCLK *7
0008 832Ch	RIIC1	Slave address register L1	SARL1	8	8	2 to 3 PCLK *7
0008 832Dh	RIIC1	Slave address register U1	SARU1	8	8	2 to 3 PCLK *7
0008 832Eh	RIIC1	Slave address register L2	SARL2	8	8	2 to 3 PCLK *7
0008 832Fh	RIIC1	Slave address register U2	SARU2	8	8	2 to 3 PCLK *7
0008 8330h	RIIC1	I²C bus bit rate low-level register	ICBRL	8	8	2 to 3 PCLK *7
0008 8331h	RIIC1	I²C bus bit rate high-level register	ICBRH	8	8	2 to 3 PCLK *7
0008 8332h	RIIC1	I²C bus transmit data register	ICDRT	8	8	2 to 3 PCLK *7
0008 8333h	RIIC1	I²C bus receive data register	ICDRR	8	8	2 to 3 PCLK *7
0008 C000h	P0	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C001h	P1	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C002h	P2	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C003h	P3	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C004h	P4	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C005h	P5	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C006h	P6	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C007h	P7	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C008h	P8	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C009h	P9	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Ah	PA	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Bh	PB	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Ch	PC	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Dh	PD	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Eh	PE	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Fh	PF	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C010h	PG	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C011h	PH	Data direction register	DDR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C020h	P0	Data register	DR	8	8	2 to 3 PCLK *7
0008 C021h	P1	Data register	DR	8	8	2 to 3 PCLK *7
0008 C022h	P2	Data register	DR	8	8	2 to 3 PCLK *7
0008 C023h	P3	Data register	DR	8	8	2 to 3 PCLK *7
0008 C024h	P4	Data register	DR	8	8	2 to 3 PCLK *7
0008 C025h	P5	Data register	DR	8	8	2 to 3 PCLK *7
0008 C026h	P6	Data register	DR	8	8	2 to 3 PCLK *7
0008 C027h	P7	Data register	DR	8	8	2 to 3 PCLK *7
0008 C028h	P8	Data register	DR	8	8	2 to 3 PCLK *7
0008 C029h	P9	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Ah	PA	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Bh	PB	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Ch	PC	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Dh	PD	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Eh	PE	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Fh	PF	Data register	DR	8	8	2 to 3 PCLK *7
0008 C030h	PG	Data register	DR	8	8	2 to 3 PCLK *7
0008 C031h	PH	Data register	DR	8	8	2 to 3 PCLK *7
0008 C040h	P0	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C041h	P1	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C042h	P2	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C043h	P3	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C044h	P4	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C045h	P5	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C046h	P6	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C047h	P7	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C048h	P8	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C049h	P9	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Ah	PA	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Bh	PB	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Ch	PC	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Dh	PD	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Eh	PE	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Fh	PF	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C050h	PG	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C051h	PH	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C060h	P0	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C061h	P1	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C062h	P2	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C063h	P3	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C064h	P4	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C065h	P5	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C066h	P6	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C067h	P7	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C068h	P8	Input buffer control register	ICR	8	8	2 to 3 PCLK *7

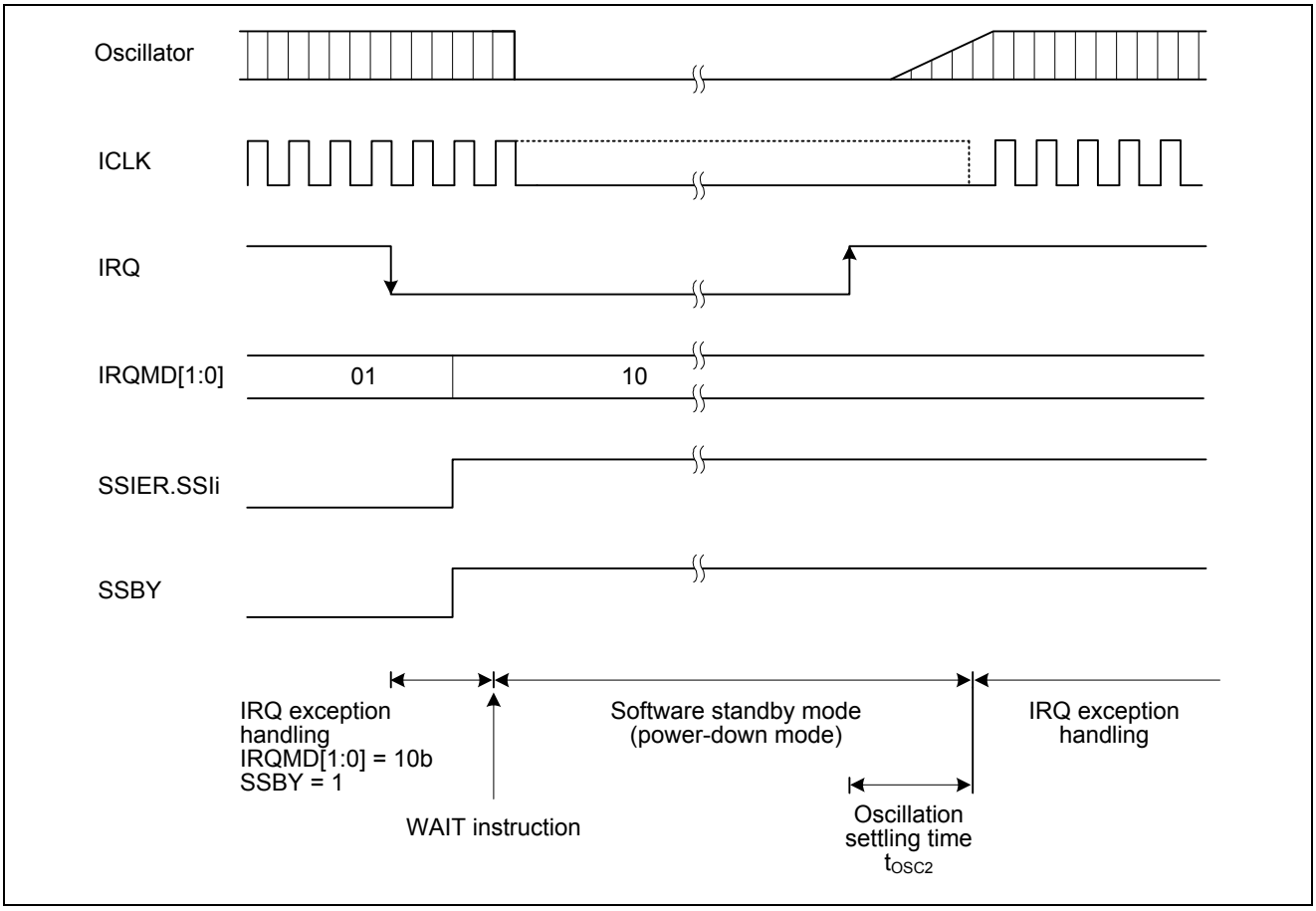


Figure 5.2 Oscillation Settling Timing after Software Standby Mode

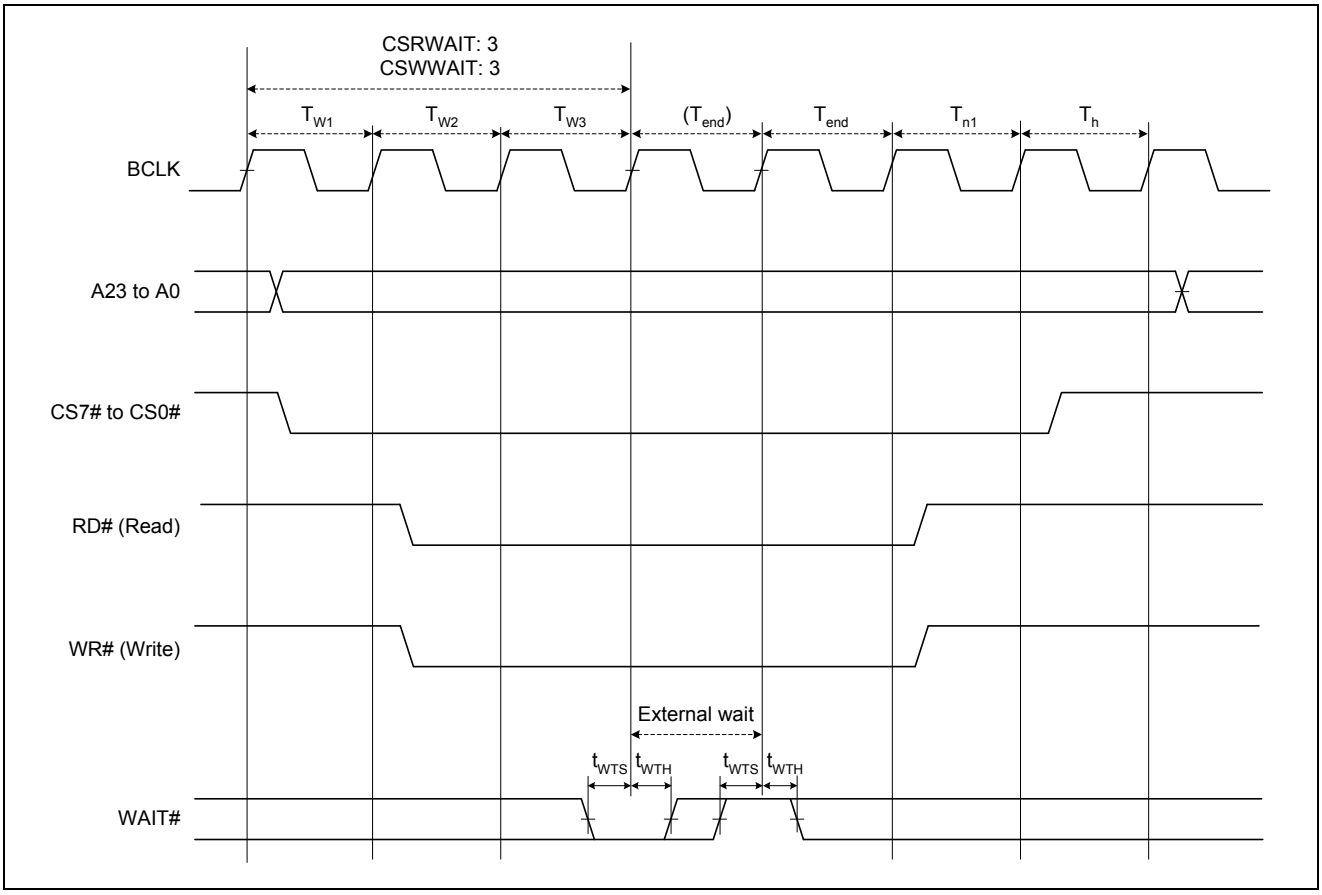


Figure 5.13 External Bus Timing/External Wait Control

5.3.4 Timing of On-Chip Peripheral Modules

Table 5.8 Timing of On-Chip Peripheral Modules (1)

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V, PCLK = 8 to 50 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)
Output load conditions: V_{OH} = V_{CC} x 0.5, V_{OL} = V_{CC} x 0.5, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item			Symbol	Min.	Max.	Unit	Test Conditions
I/O ports	Output data delay time		t_{PWD}	—	40	ns	Figure 5.14
	Input data setup time		t_{PRS}	25	—	ns	
	Input data hold time		t_{PRH}	25	—	ns	
TPU	Timer output delay time		t_{TOCD}	—	40	ns	Figure 5.15
	Timer input setup time		t_{TICS}	25	—	ns	
	Timer clock input setup time		t_{TCKS}	25	—	ns	Figure 5.16
	Timer clock pulse width	Single-edge setting	t_{TCKWH}	1.5 x (1/PCLK)	—	t_{cyc}	
		Both-edge setting	t_{TCKWL}	2.5 x (1/PCLK)	—	t_{cyc}	
PPG	Pulse output delay time		t_{POD}	—	40	ns	Figure 5.17
8-bit timer	Timer output delay time		t_{TMOD}	—	40	ns	Figure 5.18
	Timer reset input setup time		t_{TMRS}	25	—	ns	Figure 5.19
	Timer clock input setup time		t_{TMCS}	25	—	ns	Figure 5.20
	Timer clock pulse width	Single-edge setting	t_{TMCWH}	1.5 x (1/PCLK)	—	t_{cyc}	
		Both-edge setting	t_{TMCWL}	2.5 x (1/PCLK)	—	t_{cyc}	
WDT	Overflow output delay time		t_{WOVD}	—	40	ns	Figure 5.21
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4 x (1/PCLK)	—	t_{cyc}	Figure 5.22
		Clock synchronous		6 x (1/PCLK)	—		
	Input clock pulse width		t_{SCKW}	0.4 x t_{Scyc}	0.6 x t_{Scyc}	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	20	ns	
	Input clock fall time		t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	4 x (1/PCLK)	—	t_{cyc}	
		Clock synchronous		6 x (1/PCLK)	—		
	Output clock pulse width		t_{SCKW}	0.4 x t_{Scyc}	0.6 x t_{Scyc}	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	20	ns	
	Output clock fall time		t_{SCKf}	—	20	ns	
	Transmit data delay time		t_{TXD}	—	40	ns	Figure 5.23
	Receive data setup time (clock synchronous)		t_{RXS}	40	—	ns	
	Receive data hold time (clock synchronous)		t_{RXH}	40	—	ns	
A/D converter	Trigger input setup time		t_{TRGS}	25	—	ns	Figure 5.24

Table 5.8 Timing of On-Chip Peripheral Modules (2)

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V, PCLK = 8 to 50 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item		Symbol	Min. *1*2	Max.	Unit	Test Conditions
RIIC (Standard-mode) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	8(10) x (1/PCLK) + 1300	—	ns	Figure 5.25
	SCL input high pulse width	t_{SCLH}	3(5) x (1/PCLK) + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	5x (1/PCLK) + 1000	—	ns	
	SCL, SDA input rising time	t_{Sr}	—	1000	ns	
	SCL, SDA input falling time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 x (1/PCLK)	ns	
	SDA input bus free time	t_{BUF}	5x (1/PCLK) + 1000	—	ns	
	Start condition input hold time	t_{STAH}	3(5) x (1/PCLK) + 300	—	ns	
	Re-start condition input setup time	t_{STAS}	5x (1/PCLK) + 1000	—	ns	
	Stop condition input setup time	t_{STOS}	3(5) x (1/PCLK) + 300	—	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	8(10) x (1/PCLK) + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(5) x (1/PCLK) + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	5 x (1/PCLK) + 300	—	ns	
	SCL, SDA input rising time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input falling time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 x (1/PCLK)	ns	
	SDA input bus free time	t_{BUF}	5 x (1/PCLK) + 300	—	ns	
	Start condition input hold time	t_{STAH}	3(5) x (1/PCLK) + 300	—	ns	
	Re-start condition input setup time	t_{STAS}	5 x (1/PCLK) + 300	—	ns	
	Stop condition input setup time	t_{STOS}	3(5) x (1/PCLK) + 300	—	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

REVISION HISTORY — RX610 Group Datasheet

		Description	
Rev.	**Data**	**Page**	**Summary**
0.50	Mar. 24, 2009	–	First edition issued
1.00	Apr. 22, 2011		1. Overview
		6	Figure 1.2 Block Diagram: Ports F to H added
		7	Figure 1.3 Pin Assignment of the 176-pin LFBGA, added
		10 to 15	Table 1.3 List of Pins and Pin Functions (176-Pin LFBGA), added
			Table 1.5 Pin Functions:
		21, 25	Description on the BSCANP, PF0 to PF6, PG0 to PG7, and PH0 to PH7 pins added
			4. I/O Registers
		34 to 54	Table 4.1 List of I/O Registers (Address Order), changed
			5. Electrical Characteristics
		58	Table 5.3 Permissible Output Currents, changed
		59	Table 5.5 Clock Timing: Oscillation settling time after leaving deep software standby mode (crystal), $t_{OSC3,}$ added
		60	Figure 5.2 Oscillation Settling Timing after Software Standby Mode, changed
		61	Figure 5.3 Oscillation Settling Timing after Deep Software Standby Mode, added
		71	Table 5.8 Timing of On-Chip Peripheral Modules (3), changed
		75	Figure 5.26 Boundary Scan TCK Timing, added
		75	Figure 5.27 Boundary Scan TRST# Timing, added
		76	Figure 5.28 Boundary Scan Input/Output Timing, added
1.20	Feb.20, 2013		1. Overview
		5	Table 1.2 List of Products, product lineup added
		23, 26	Table 1.5 Pin Functions, description on bus control changed, note added
			5. I/O register
		35 to 55	Table 5.1 List of I/O Registers (Address Order), changed