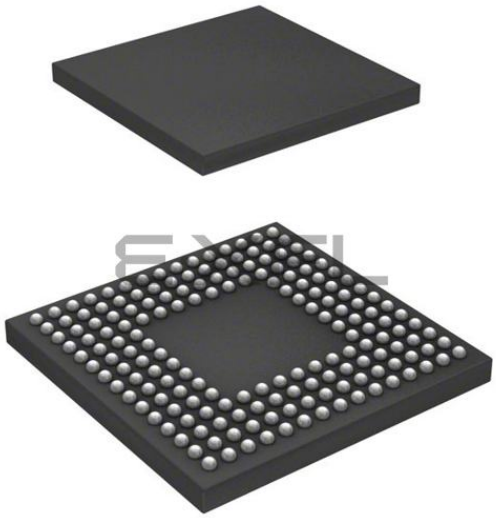
Renesas Electronics America Inc - R5F56108WNBG#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	140
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 2x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56108wnbg-u0

1.1.2 Outline of Specifications

Table 1.1 lists the specifications of the RX610 Group in outline.

Table 1.1 Outline of Specifications

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 100 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction in one state (in one system clock cycle) • Address space: 4-Gbyte linear address • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Nine 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point operation instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 x 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions conforming to the IEEE754 standard
Memory	Flash	• Flash capacity: 2 Mbytes (max.) • Three types of on-board programming modes SCI boot mode, user program mode, and user boot mode
	RAM	RAM capacity: 128 Kbytes
	Data flash	Data flash capacity: 32 Kbytes
MCU operating modes		Single-chip mode, on-chip ROM enabled extended mode, and on-chip ROM disabled extended mode
Clock	Clock generation circuit	• One main clock oscillation circuit • Includes a PLL circuit and frequency divider, so the operating frequency is selectable • System clock, peripheral module clock, and external bus clock are independently specifiable. The CPU, DMAC, DTC, ROM, and RAM run in synchronization with the system clock (ICLK): 8 to 100 MHz Peripheral modules run in synchronization with the peripheral module clock (PCLK): 8 to 50 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): 8 to 25 MHz
Power down	Power-down function	• Module stop function • Four power-down modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode

Classification	Module/Function	Description
Interrupt	Interrupt control unit	• Peripheral function interrupts: 116 • External interrupts: 16 (pins IRQ15 to IRQ0) • Non-maskable interrupt: 1 (the NMI pin) • Eight priority orders specifiable
External bus extension		• The external address space can be divided into eight areas (CS0 to CS7), each of which is independently controllable. Capacity of each area: 16 Mbytes Chip-select signals (CS0# to CS7#) can be output for each area. 8-bit or 16-bit bus space can be specified for each area. The data arrangement is selectable as little endian or big endian for each area. (only for data) • Separate bus system • Wait control • Write buffer programming
DMA	DMA controller	• 4-channel DMA transfer available • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activated by interrupt requests (chain transfer enabled)
I/O ports	Programmable I/O ports	• I/O pins: 117 (144-pin LQFP), 140 (176-pin LFBGA) • Pull-up resistors: 40 • Open-drain outputs: 16 • 5-V tolerance: 10
Timer	16-bit timer pulse unit	• (16 bits x 6 channels) x 2 units • Up to 16 pulse inputs and outputs • Select from among 7 or 8 counter-input clocks for each channel • Input capture/output compare function • Maximum of 15-phase PWM output possible in PWM mode • Buffered operation, phase counting mode (two-phase encoder input), and cascaded operation (32 bits x 2 channels) settable for each channel • PPG output trigger can be generated • Conversion start trigger for the A/D converter can be generated
	Programmable pulse generator	• (4 bits x 4 groups) x 2 units • Provides pulse outputs by using the TPU output as a trigger • Maximum of 32-bit pulse output possible
	8-bit timer	• (8 bits x 2 channels) x 2 units • Select from among 8 clock sources (7 internal clocks and 1 external clock) • Allows the output of pulse trains with a desired duty cycle or PWM signals • Cascading of 2 channels enables it to be used as a 16-bit timer • Generation of trigger to start A/D converter conversion • Capable of generating baud rate clock for SCI5 and SCI6
	Compare match timer	• (16 bits x 2 channels) x 2 units • Select from among 4 counter-input clocks

Watchdog timer		• 8 bits x 1 channel • Select from among 8 counter-input clocks • Switchable between watchdog timer mode and interval timer mode
Communication function	Serial communication interface	• 7 channels • Serial communication mode: Asynchronous, clock synchronous, and smart card interface • On-chip baud rate generator allows any bit rate to be selected • Choice of LSB-first or MSB-first transfer • Enables average transfer rate clock input from TMR (SCI5, SCI6)
	I^2C bus interface	• 2 channels • Communication format I^2C bus format/SMBus format Master/slave selectable (For multi-master operation) • Maximum transfer rate: 1 Mbps
A/D converter		• 4 units (1 unit x 4 channels) • 10-bit resolution • Conversion time: 1.0 μs per channel (at 50-MHz (PCLK) operation) • Two kinds of operating modes Single mode and scan mode (single scan mode or continuous scan mode) • Sample-and-hold function • Three types of A/D conversion start Conversion can be started by software, a conversion start trigger by the timer (TPU or TMR), or an external trigger signal.
D/A converter		• 2 channels • 10-bit resolution • Output voltage: 0 V to VREFH
CRC calculator		• CRC code generation for arbitrary data lengths in 8-bit units • One of three generating polynomials selectable $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$ • CRC code generation for LSB-first or MSB-first communication selectable
Operating frequency		8 to 100 MHz
Power supply voltage		V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6V, VREFH = 3.0 to AV_{CC}
Supply current		50 mA (typ.) (regular specifications)
Operating temperature		−20 to +85°C (regular specifications), −40 to +85°C (wide-range specifications)
Package		176-pin LFBGA (PLBG0176GA-A) 144-pin LQFP (PLQP0144KA-A)

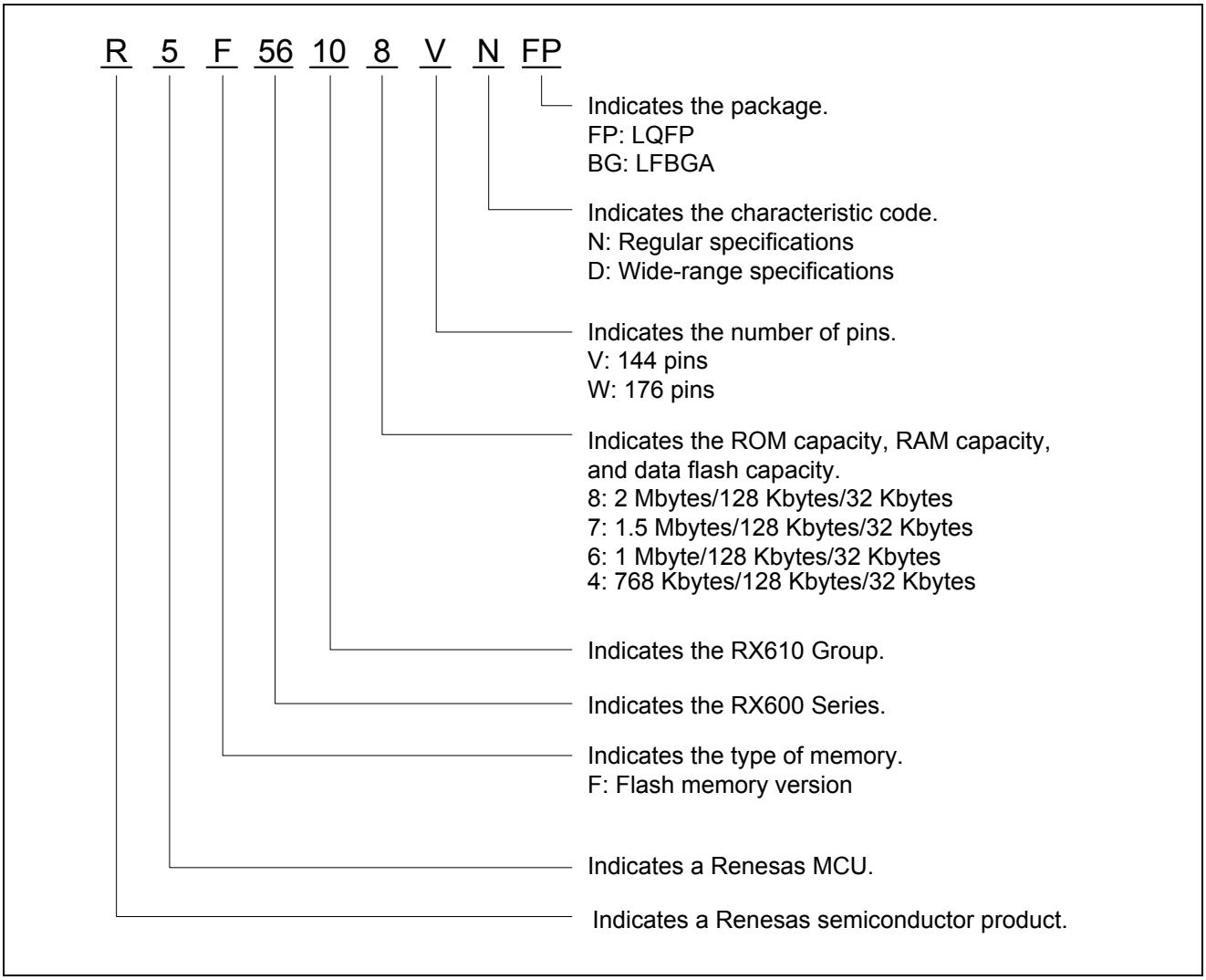
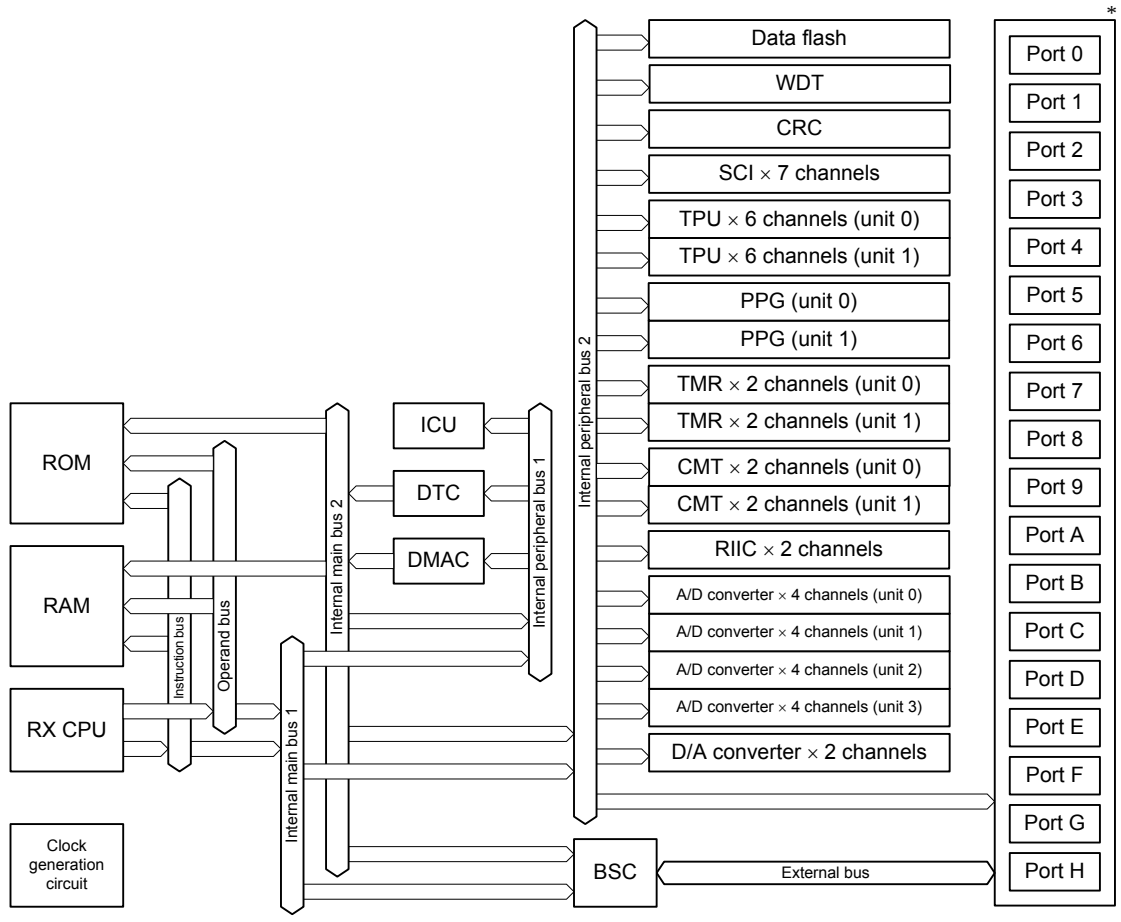


Figure 1.1 How to Read the Product Part No.

1.3 Block Diagram

Figure 1.2 shows a block diagram of the RX610 Group.



[Legend]

ICU:	Interrupt control unit	SCI:	Serial communications interfaces
DTC:	Data transfer controller	TPU:	16-bit timer pulse unit
DMAC:	DMA controller	PPG:	Programmable pulse generator
BSC:	Bus controller	TMR:	8-bit timer
WDT:	Watchdog timer	CMT:	Compare match timer
CRC:	CRC (Cyclic Redundancy Check) calculator	RIIC:	I^2C bus interface

Note: * Ports F and H are not included in the 144-pin LQFP package.

Figure 1.2 Block Diagram

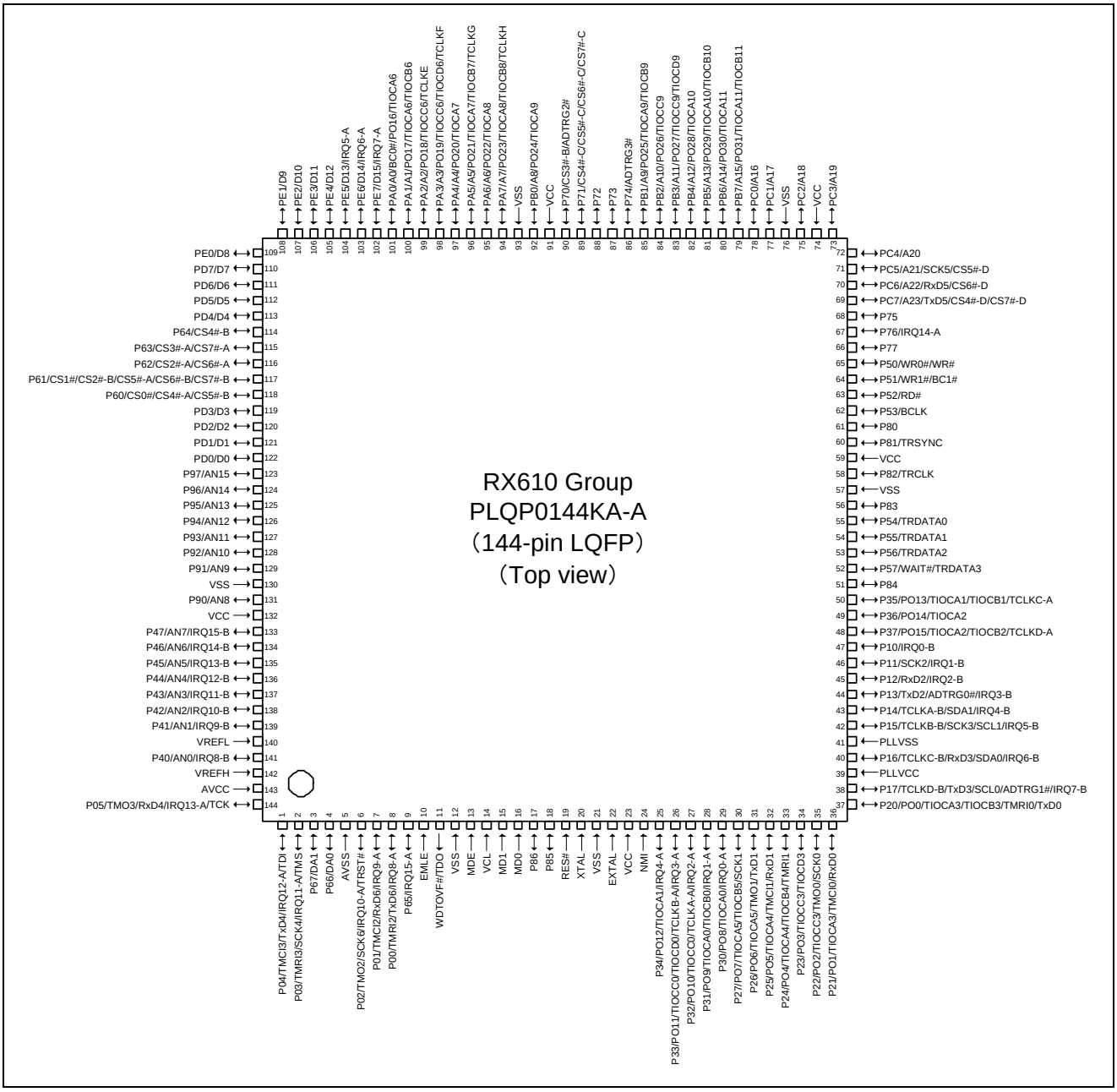


Figure 1.4 Pin Assignment of the 144-Pin LQFP

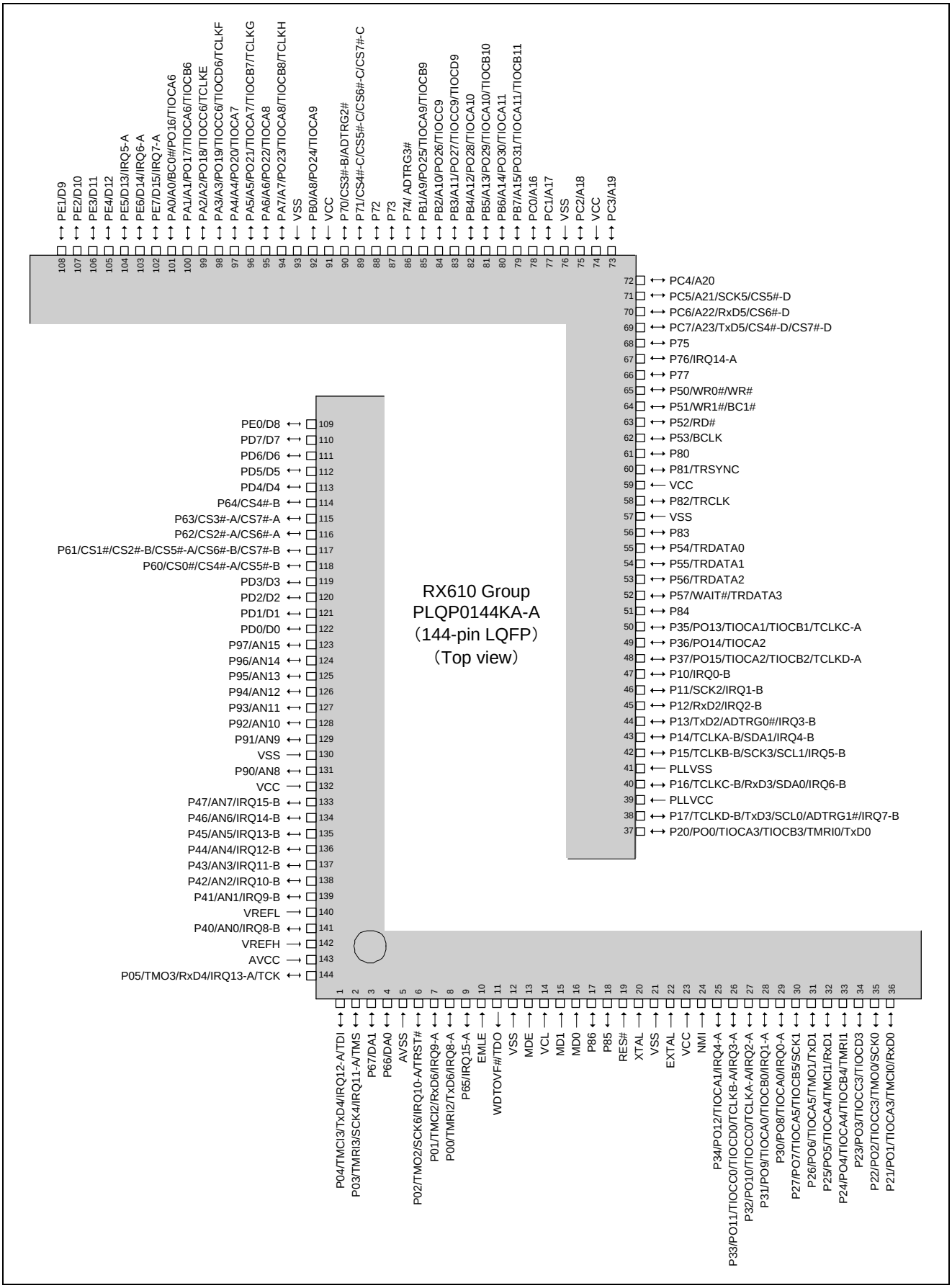


Figure 1.5 Pin Assignment (Assistance Diagram) of the 144-Pin LQFP

(8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.

When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the corresponding Cj flag indicates the source of the exception within the exception handling routine. If the exception handling is masked (Ej = 0), check the Fj flag at the end of a series of processing whether an exception is generated or not. The Fj flag is the accumulation type flag (j = X, U, Z, O, or V).

(9) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7170h	ICU	Interrupt request destination setting register 112	ISELR112	8	8	2 ICLK
0008 7175h	ICU	Interrupt request destination setting register 117	ISELR117	8	8	2 ICLK
0008 7176h	ICU	Interrupt request destination setting register 118	ISELR118	8	8	2 ICLK
0008 717Ah	ICU	Interrupt request destination setting register 122	ISELR122	8	8	2 ICLK
0008 717Bh	ICU	Interrupt request destination setting register 123	ISELR123	8	8	2 ICLK
0008 717Ch	ICU	Interrupt request destination setting register 124	ISELR124	8	8	2 ICLK
0008 717Dh	ICU	Interrupt request destination setting register 125	ISELR125	8	8	2 ICLK
0008 717Fh	ICU	Interrupt request destination setting register 127	ISELR127	8	8	2 ICLK
0008 7180h	ICU	Interrupt request destination setting register 128	ISELR128	8	8	2 ICLK
0008 7185h	ICU	Interrupt request destination setting register 133	ISELR133	8	8	2 ICLK
0008 7186h	ICU	Interrupt request destination setting register 134	ISELR134	8	8	2 ICLK
0008 718Ah	ICU	Interrupt request destination setting register 138	ISELR138	8	8	2 ICLK
0008 718Bh	ICU	Interrupt request destination setting register 139	ISELR139	8	8	2 ICLK
0008 718Ch	ICU	Interrupt request destination setting register 140	ISELR140	8	8	2 ICLK
0008 718Dh	ICU	Interrupt request destination setting register 141	ISELR141	8	8	2 ICLK
0008 7191h	ICU	Interrupt request destination setting register 145	ISELR145	8	8	2 ICLK
0008 7192h	ICU	Interrupt request destination setting register 146	ISELR146	8	8	2 ICLK
0008 7197h	ICU	Interrupt request destination setting register 151	ISELR151	8	8	2 ICLK
0008 7198h	ICU	Interrupt request destination setting register 152	ISELR152	8	8	2 ICLK
0008 719Ch	ICU	Interrupt request destination setting register 156	ISELR156	8	8	2 ICLK
0008 719Dh	ICU	Interrupt request destination setting register 157	ISELR157	8	8	2 ICLK
0008 719Eh	ICU	Interrupt request destination setting register 158	ISELR158	8	8	2 ICLK
0008 719Fh	ICU	Interrupt request destination setting register 159	ISELR159	8	8	2 ICLK
0008 71A1h	ICU	Interrupt request destination setting register 161	ISELR161	8	8	2 ICLK
0008 71A2h	ICU	Interrupt request destination setting register 162	ISELR162	8	8	2 ICLK
0008 71A7h	ICU	Interrupt request destination setting register 167	ISELR167	8	8	2 ICLK
0008 71A8h	ICU	Interrupt request destination setting register 168	ISELR168	8	8	2 ICLK
0008 71AEh	ICU	Interrupt request destination setting register 174	ISELR174	8	8	2 ICLK
0008 71AFh	ICU	Interrupt request destination setting register 175	ISELR175	8	8	2 ICLK
0008 71B1h	ICU	Interrupt request destination setting register 177	ISELR177	8	8	2 ICLK
0008 71B2h	ICU	Interrupt request destination setting register 178	ISELR178	8	8	2 ICLK
0008 71B4h	ICU	Interrupt request destination setting register 180	ISELR180	8	8	2 ICLK
0008 71B5h	ICU	Interrupt request destination setting register 181	ISELR181	8	8	2 ICLK
0008 71B7h	ICU	Interrupt request destination setting register 183	ISELR183	8	8	2 ICLK
0008 71B8h	ICU	Interrupt request destination setting register 184	ISELR184	8	8	2 ICLK
0008 71C6h	ICU	Interrupt request destination setting register 198	ISELR198	8	8	2 ICLK
0008 71C7h	ICU	Interrupt request destination setting register 199	ISELR199	8	8	2 ICLK
0008 71C8h	ICU	Interrupt request destination setting register 200	ISELR200	8	8	2 ICLK
0008 71C9h	ICU	Interrupt request destination setting register 201	ISELR201	8	8	2 ICLK
0008 71D7h	ICU	Interrupt request destination setting register 215	ISELR215	8	8	2 ICLK
0008 71D8h	ICU	Interrupt request destination setting register 216	ISELR216	8	8	2 ICLK
0008 71DBh	ICU	Interrupt request destination setting register 219	ISELR219	8	8	2 ICLK
0008 71DCh	ICU	Interrupt request destination setting register 220	ISELR220	8	8	2 ICLK
0008 71DFh	ICU	Interrupt request destination setting register 223	ISELR223	8	8	2 ICLK
0008 71E0h	ICU	Interrupt request destination setting register 224	ISELR224	8	8	2 ICLK

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7321h	ICU	Interrupt priority register 21	IPR21	8	8	2 ICLK
0008 7322h	ICU	Interrupt priority register 22	IPR22	8	8	2 ICLK
0008 7323h	ICU	Interrupt priority register 23	IPR23	8	8	2 ICLK
0008 7324h	ICU	Interrupt priority register 24	IPR24	8	8	2 ICLK
0008 7325h	ICU	Interrupt priority register 25	IPR25	8	8	2 ICLK
0008 7326h	ICU	Interrupt priority register 26	IPR26	8	8	2 ICLK
0008 7327h	ICU	Interrupt priority register 27	IPR27	8	8	2 ICLK
0008 7328h	ICU	Interrupt priority register 28	IPR28	8	8	2 ICLK
0008 7329h	ICU	Interrupt priority register 29	IPR29	8	8	2 ICLK
0008 732Ah	ICU	Interrupt priority register 2A	IPR2A	8	8	2 ICLK
0008 732Bh	ICU	Interrupt priority register 2B	IPR2B	8	8	2 ICLK
0008 732Ch	ICU	Interrupt priority register 2C	IPR2C	8	8	2 ICLK
0008 732Dh	ICU	Interrupt priority register 2D	IPR2D	8	8	2 ICLK
0008 732Eh	ICU	Interrupt priority register 2E	IPR2E	8	8	2 ICLK
0008 732Fh	ICU	Interrupt priority register 2F	IPR2F	8	8	2 ICLK
0008 7340h	ICU	Interrupt priority register 40	IPR40	8	8	2 ICLK
0008 7344h	ICU	Interrupt priority register 44	IPR44	8	8	2 ICLK
0008 7345h	ICU	Interrupt priority register 45	IPR45	8	8	2 ICLK
0008 7346h	ICU	Interrupt priority register 46	IPR46	8	8	2 ICLK
0008 7347h	ICU	Interrupt priority register 47	IPR47	8	8	2 ICLK
0008 734Ch	ICU	Interrupt priority register 4C	IPR4C	8	8	2 ICLK
0008 734Dh	ICU	Interrupt priority register 4D	IPR4D	8	8	2 ICLK
0008 734Eh	ICU	Interrupt priority register 4E	IPR4E	8	8	2 ICLK
0008 734Fh	ICU	Interrupt priority register 4F	IPR4F	8	8	2 ICLK
0008 7350h	ICU	Interrupt priority register 50	IPR50	8	8	2 ICLK
0008 7351h	ICU	Interrupt priority register 51	IPR51	8	8	2 ICLK
0008 7352h	ICU	Interrupt priority register 52	IPR52	8	8	2 ICLK
0008 7353h	ICU	Interrupt priority register 53	IPR53	8	8	2 ICLK
0008 7354h	ICU	Interrupt priority register 54	IPR54	8	8	2 ICLK
0008 7355h	ICU	Interrupt priority register 55	IPR55	8	8	2 ICLK
0008 7356h	ICU	Interrupt priority register 56	IPR56	8	8	2 ICLK
0008 7357h	ICU	Interrupt priority register 57	IPR57	8	8	2 ICLK
0008 7358h	ICU	Interrupt priority register 58	IPR58	8	8	2 ICLK
0008 7359h	ICU	Interrupt priority register 59	IPR59	8	8	2 ICLK
0008 735Ah	ICU	Interrupt priority register 5A	IPR5A	8	8	2 ICLK
0008 735Bh	ICU	Interrupt priority register 5B	IPR5B	8	8	2 ICLK
0008 735Ch	ICU	Interrupt priority register 5C	IPR5C	8	8	2 ICLK
0008 735Dh	ICU	Interrupt priority register 5D	IPR5D	8	8	2 ICLK
0008 735Eh	ICU	Interrupt priority register 5E	IPR5E	8	8	2 ICLK
0008 735Fh	ICU	Interrupt priority register 5F	IPR5F	8	8	2 ICLK
0008 7360h	ICU	Interrupt priority register 60	IPR60	8	8	2 ICLK
0008 7361h	ICU	Interrupt priority register 61	IPR61	8	8	2 ICLK
0008 7362h	ICU	Interrupt priority register 62	IPR62	8	8	2 ICLK
0008 7363h	ICU	Interrupt priority register 63	IPR63	8	8	2 ICLK
0008 7368h	ICU	Interrupt priority register 68	IPR68	8	8	2 ICLK

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 802Bh	WDT	Reset control/status register	RSTCSR	8	8	2 to 3 PCLK *7
0008 8040h	AD0	A/D data register A	ADDRA	16	16	2 to 3 PCLK *7
0008 8042h	AD0	A/D data register B	ADDRB	16	16	2 to 3 PCLK *7
0008 8044h	AD0	A/D data register C	ADDRC	16	16	2 to 3 PCLK *7
0008 8046h	AD0	A/D data register D	ADDRD	16	16	2 to 3 PCLK *7
0008 8050h	AD0	A/D control/status register	ADCSR	8	8	2 to 3 PCLK *7
0008 8051h	AD0	A/D control register	ADCR	8	8	2 to 3 PCLK *7
0008 8052h	AD0	ADDRy format select register	ADDPR	8	8	2 to 3 PCLK *7
0008 8053h	AD0	A/D sampling state register	ADSSTR	8	8	2 to 3 PCLK *7
0008 8060h	AD1	A/D data register A	ADDRA	16	16	2 to 3 PCLK *7
0008 8062h	AD1	A/D data register B	ADDRB	16	16	2 to 3 PCLK *7
0008 8064h	AD1	A/D data register C	ADDRC	16	16	2 to 3 PCLK *7
0008 8066h	AD1	A/D data register D	ADDRD	16	16	2 to 3 PCLK *7
0008 8070h	AD1	A/D control/status register	ADCSR	8	8	2 to 3 PCLK *7
0008 8071h	AD1	A/D control register	ADCR	8	8	2 to 3 PCLK *7
0008 8072h	AD1	ADDRy format select register	ADDPR	8	8	2 to 3 PCLK *7
0008 8073h	AD1	A/D sampling state register	ADSSTR	8	8	2 to 3 PCLK *7
0008 8080h	AD2	A/D data register A	ADDRA	16	16	2 to 3 PCLK *7
0008 8082h	AD2	A/D data register B	ADDRB	16	16	2 to 3 PCLK *7
0008 8084h	AD2	A/D data register C	ADDRC	16	16	2 to 3 PCLK *7
0008 8086h	AD2	A/D data register D	ADDRD	16	16	2 to 3 PCLK *7
0008 8090h	AD2	A/D control/status register	ADCSR	8	8	2 to 3 PCLK *7
0008 8091h	AD2	A/D control register	ADCR	8	8	2 to 3 PCLK *7
0008 8092h	AD2	ADDRy format select register	ADDPR	8	8	2 to 3 PCLK *7
0008 8093h	AD2	A/D sampling state register	ADSSTR	8	8	2 to 3 PCLK *7
0008 80A0h	AD3	A/D data register A	ADDRA	16	16	2 to 3 PCLK *7
0008 80A2h	AD3	A/D data register B	ADDRB	16	16	2 to 3 PCLK *7
0008 80A4h	AD3	A/D data register C	ADDRC	16	16	2 to 3 PCLK *7
0008 80A6h	AD3	A/D data register D	ADDRD	16	16	2 to 3 PCLK *7
0008 80B0h	AD3	A/D control/status register	ADCSR	8	8	2 to 3 PCLK *7
0008 80B1h	AD3	A/D control register	ADCR	8	8	2 to 3 PCLK *7
0008 80B2h	AD3	ADDRy format select register	ADDPR	8	8	2 to 3 PCLK *7
0008 80B3h	AD3	A/D sampling state register	ADSSTR	8	8	2 to 3 PCLK *7
0008 80C0h	D/A	D/A data register 0	DADR0	16	16	2 to 3 PCLK *7
0008 80C2h	D/A	D/A data register 1	DADR1	16	16	2 to 3 PCLK *7
0008 80C4h	D/A	D/A control register	DACR	8	8	2 to 3 PCLK *7
0008 80C5h	D/A	DADRy format select register	DADPR	8	8	2 to 3 PCLK *7
0008 8100h	TPU (unit 0)	Timer start register	TSTRA	8	8	2 to 3 PCLK *7
0008 8101h	TPU (unit 0)	Timer synchronous register	TSYRA	8	8	2 to 3 PCLK *7
0008 8110h	TPU0	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8111h	TPU0	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8112h	TPU0	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK *7
0008 8113h	TPU0	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK *7
0008 8114h	TPU0	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8115h	TPU0	Timer status register	TSR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 830Fh	RIIC0	Slave address register U2	SARU2	8	8	2 to 3 PCLK *7
0008 8310h	RIIC0	I²C bus bit rate low-level register	ICBRL	8	8	2 to 3 PCLK *7
0008 8311h	RIIC0	I²C bus bit rate high-level register	ICBRH	8	8	2 to 3 PCLK *7
0008 8312h	RIIC0	I²C bus transmit data register	ICDRT	8	8	2 to 3 PCLK *7
0008 8313h	RIIC0	I²C bus receive data register	ICDRR	8	8	2 to 3 PCLK *7
0008 8320h	RIIC1	I²C bus control register 1	ICCR1	8	8	2 to 3 PCLK *7
0008 8321h	RIIC1	I²C bus control register 2	ICCR2	8	8	2 to 3 PCLK *7
0008 8322h	RIIC1	I²C bus mode register 1	ICMR1	8	8	2 to 3 PCLK *7
0008 8323h	RIIC1	I²C bus mode register 2	ICMR2	8	8	2 to 3 PCLK *7
0008 8324h	RIIC1	I²C bus mode register 3	ICMR3	8	8	2 to 3 PCLK *7
0008 8325h	RIIC1	I²C bus function enable register	ICFER	8	8	2 to 3 PCLK *7
0008 8326h	RIIC1	I²C bus status enable register	ICSER	8	8	2 to 3 PCLK *7
0008 8327h	RIIC1	I²C bus interrupt enable register	ICIER	8	8	2 to 3 PCLK *7
0008 8328h	RIIC1	I²C bus status register 1	ICSR1	8	8	2 to 3 PCLK *7
0008 8329h	RIIC1	I²C bus status register 2	ICSR2	8	8	2 to 3 PCLK *7
0008 832Ah	RIIC1	Slave address register L0	SARL0	8	8	2 to 3 PCLK *7
0008 832Ah	RIIC1	Internal control for timeout L	TMOCNTL	16	16	2 to 3 PCLK *7
0008 832Bh	RIIC1	Slave address register U0	SARU0	8	8	2 to 3 PCLK *7
0008 832Bh	RIIC1	Internal control for timeout U	TMOCNTU	16	16	2 to 3 PCLK *7
0008 832Ch	RIIC1	Slave address register L1	SARL1	8	8	2 to 3 PCLK *7
0008 832Dh	RIIC1	Slave address register U1	SARU1	8	8	2 to 3 PCLK *7
0008 832Eh	RIIC1	Slave address register L2	SARL2	8	8	2 to 3 PCLK *7
0008 832Fh	RIIC1	Slave address register U2	SARU2	8	8	2 to 3 PCLK *7
0008 8330h	RIIC1	I²C bus bit rate low-level register	ICBRL	8	8	2 to 3 PCLK *7
0008 8331h	RIIC1	I²C bus bit rate high-level register	ICBRH	8	8	2 to 3 PCLK *7
0008 8332h	RIIC1	I²C bus transmit data register	ICDRT	8	8	2 to 3 PCLK *7
0008 8333h	RIIC1	I²C bus receive data register	ICDRR	8	8	2 to 3 PCLK *7
0008 C000h	P0	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C001h	P1	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C002h	P2	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C003h	P3	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C004h	P4	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C005h	P5	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C006h	P6	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C007h	P7	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C008h	P8	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C009h	P9	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Ah	PA	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Bh	PB	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Ch	PC	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Dh	PD	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Eh	PE	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Fh	PF	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C010h	PG	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C011h	PH	Data direction register	DDR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C020h	P0	Data register	DR	8	8	2 to 3 PCLK *7
0008 C021h	P1	Data register	DR	8	8	2 to 3 PCLK *7
0008 C022h	P2	Data register	DR	8	8	2 to 3 PCLK *7
0008 C023h	P3	Data register	DR	8	8	2 to 3 PCLK *7
0008 C024h	P4	Data register	DR	8	8	2 to 3 PCLK *7
0008 C025h	P5	Data register	DR	8	8	2 to 3 PCLK *7
0008 C026h	P6	Data register	DR	8	8	2 to 3 PCLK *7
0008 C027h	P7	Data register	DR	8	8	2 to 3 PCLK *7
0008 C028h	P8	Data register	DR	8	8	2 to 3 PCLK *7
0008 C029h	P9	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Ah	PA	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Bh	PB	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Ch	PC	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Dh	PD	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Eh	PE	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Fh	PF	Data register	DR	8	8	2 to 3 PCLK *7
0008 C030h	PG	Data register	DR	8	8	2 to 3 PCLK *7
0008 C031h	PH	Data register	DR	8	8	2 to 3 PCLK *7
0008 C040h	P0	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C041h	P1	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C042h	P2	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C043h	P3	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C044h	P4	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C045h	P5	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C046h	P6	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C047h	P7	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C048h	P8	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C049h	P9	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Ah	PA	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Bh	PB	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Ch	PC	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Dh	PD	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Eh	PE	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Fh	PF	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C050h	PG	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C051h	PH	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C060h	P0	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C061h	P1	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C062h	P2	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C063h	P3	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C064h	P4	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C065h	P5	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C066h	P6	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C067h	P7	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C068h	P8	Input buffer control register	ICR	8	8	2 to 3 PCLK *7

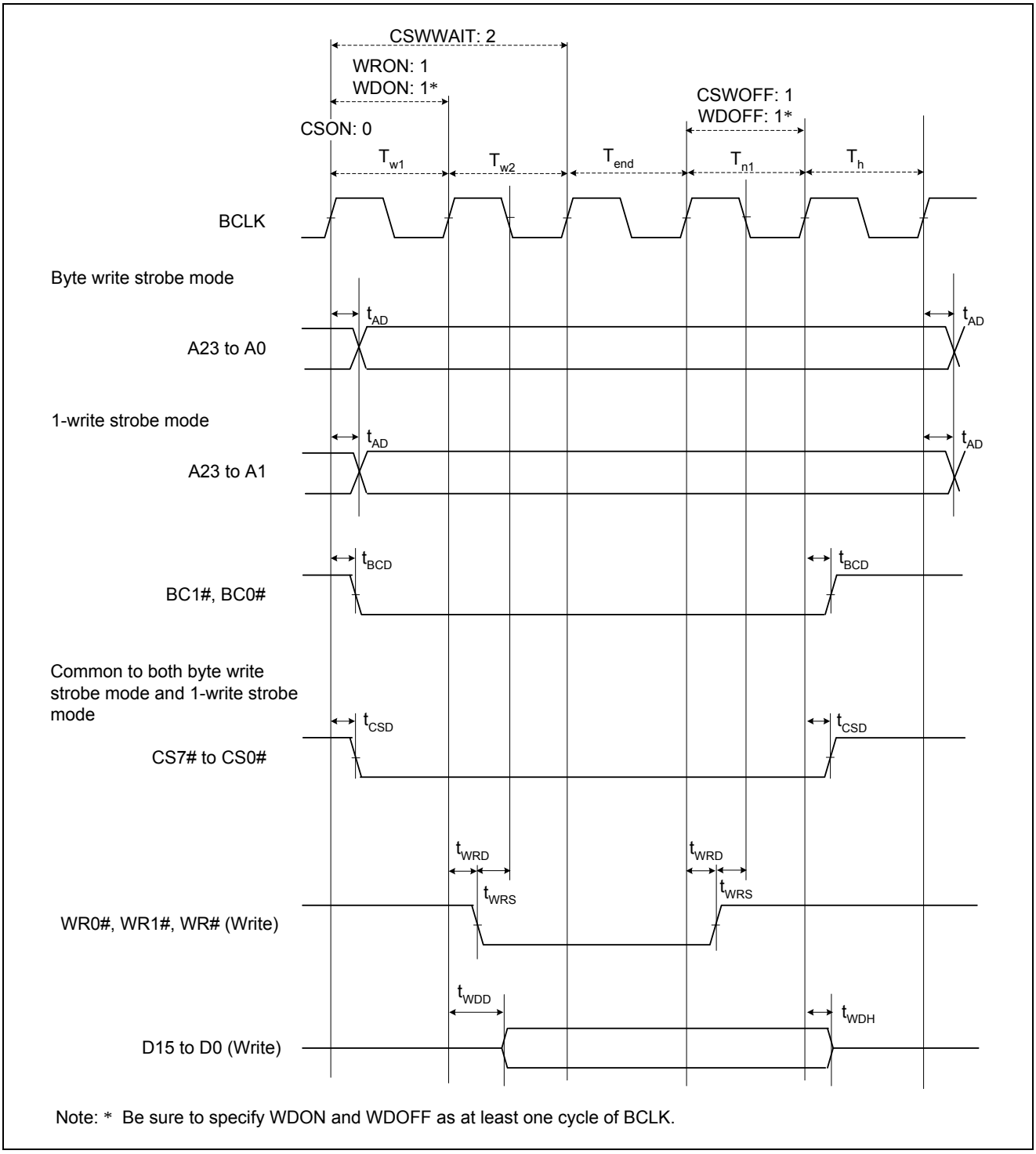
Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C329h	ICU	IRQ control register 9	IRQCR9	8	8	2 to 3 PCLK *7
0008 C32Ah	ICU	IRQ control register 10	IRQCR10	8	8	2 to 3 PCLK *7
0008 C32Bh	ICU	IRQ control register 11	IRQCR11	8	8	2 to 3 PCLK *7
0008 C32Ch	ICU	IRQ control register 12	IRQCR12	8	8	2 to 3 PCLK *7
0008 C32Dh	ICU	IRQ control register 13	IRQCR13	8	8	2 to 3 PCLK *7
0008 C32Eh	ICU	IRQ control register 14	IRQCR14	8	8	2 to 3 PCLK *7
0008 C32Fh	ICU	IRQ control register 15	IRQCR15	8	8	2 to 3 PCLK *7
0008 C340h	ICU	Software standby release IRQ enable register	SSIER	16	16	2 to 3 PCLK *7
0008 C350h	ICU	Non-maskable interrupt enable register	NMIER	8	8	2 to 3 PCLK *7
0008 C351h	ICU	NMI pin interrupt control register	NMICR	8	8	2 to 3 PCLK *7
0008 C352h	ICU	Non-maskable interrupt status register	NMISR	8	8	2 to 3 PCLK *7
0008 C353h	ICU	Non-maskable interrupt clear register	NMICLR	8	8	2 to 3 PCLK *7
007F C402h	FLASH	Flash mode register	FMODR	8	8	2 to 3 PCLK *7
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2 to 3 PCLK *7
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2 to 3 PCLK *7
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2 to 3 PCLK *7
007F C440h	FLASH	Data flash read enable register	DFLRE	16	16	2 to 3 PCLK *7
007F C450h	FLASH	Data flash programming/erasure enable register	DFLWE	16	16	2 to 3 PCLK *7
007F C454h	FLASH	FCU RAM enable register	FCURAME	16	16	2 to 3 PCLK *7
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2 to 3 PCLK *7
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2 to 3 PCLK *7
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2 to 3 PCLK *7
007F FFB4h	FLASH	Flash protection register	FPROTR	16	16	2 to 3 PCLK *7
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2 to 3 PCLK *7
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2 to 3 PCLK *7
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2 to 3 PCLK *7
007F FFCAh	FLASH	Data flash blank check control register	DFLBCCNT	16	16	2 to 3 PCLK *7
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2 to 3 PCLK *7
007F FFCEh	FLASH	Data flash blank check status register	DFLBCSTAT	16	16	2 to 3 PCLK *7
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2 to 3 PCLK *7

Notes:
1. When the same output trigger is specified for pulse output groups 2 and 3 by the PPG0.PCR setting, the PPG0.NDRH address is 000881ECh. When different output triggers are specified, the PPG0.NDRH addresses for pulse output groups 2 and 3 are 000881EEh and 000881ECh, respectively.
2. When the same output trigger is specified for pulse output groups 0 and 1 by the PPG0.PCR setting, the PPG0.NDRL address is 000881EDh. When different output triggers are specified, the PPG0.NDRL addresses for pulse output groups 0 and 1 are 000881EFh and 000881EDh, respectively.
3. When the same output trigger is specified for pulse output groups 6 and 7 by the PPG1.PCR setting, the PPG1.NDRH address is 000881FCh. When different output triggers are specified, the PPG1.NDRH addresses for pulse output groups 6 and 7 are 000881FEh and 000881FCh, respectively.
4. When the same output trigger is specified for pulse output groups 4 and 5 by the PPG1.PCR setting, the PPG1.NDRL address is 000881FDh. When different output triggers are specified, the PPG1.NDRL addresses for pulse output groups 4 and 5 are 000881FFh and 000881FDh, respectively.
5. 16-bit access to odd addresses is prohibited. When 16-bit access is required, access is at the address corresponding to TMR0 or TMR2.
6. For certain bits, functions differ according to whether the mode is serial communications or smart card interface.
7. The number of access cycles varies depending on the number of divided cycles for clock synchronization (0 to one PCLK).
8. The number of access cycles may be 5 ICLK if the register is accessed during the DMAC operation.

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input pull-up resistor current	Ports A to E			$-I_p$	10	—	300	µA	V_{CC} = 3.0 to 3.6 V, V_{in} = 0 V
Input capacitance	All input pins (except port 0, ports 14 to 17)			C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	Port 0, ports 14 to 17				—	—	30		
Supply current*3	In operation	Max.*4		I_{CC}*5	—	—	100	mA	ICLK = 100 MHz PCLK = 50 MHz BCLK = 25 MHz
		Normal*6			—	35	—		
		Increased by BGO operation*7			—	15	—		
	Sleep				—	18	52		
	All-module-clock-stop mode*8				—	14	28		
	Standby mode	Software standby mode			—	0.08	3.0		
		Deep software standby mode	RAM retained		—	15	200	µA	
			RAM power supply halted		—	0.9	26		
Analog power supply current	During A/D conversion (per unit)			AI_{CC}	—	0.8	1.2	mA	
	During D/A conversion (per unit)				—	0.3	1.0	µA	
	Idle (all units)				—	0.3	1.0		
Reference power supply current	During A/D conversion (per unit)				—	0.06	0.1	mA	
	During D/A conversion (per unit)				—	0.4	0.6		
	Idle (all units)				—	0.3	1.0	µA	
RAM standby voltage				V_{RAM}	2.5	—	—	V	
V_{CC} start voltage*9				$V_{CCSTART}$	—	—	0.8	V	
V_{CC} rising gradient*9				SV_{CC}	—	—	20	ms/V	

Notes:
1. This does not include the pins, which are multiplexed as ports 0, and 14 to 17 for 5 V tolerant.
2. This includes the multiplexed pins, but RIIC input pins for ports 14 to 17 are excluded.
3. Supply current values are with all output pins unloaded, all input pins for V_{IH} = V_{CC} and V_{IL}= 0 V, and all input pull-up resistors in the off state.
4. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
5. I_{CC} depends on f (ICLK) as follows. (ICLK : PCLK : BCLK = 8 : 4: 2)

   I_{CC} max. = 0.89 x f + 11 (max.)
   I_{CC} typ. = 0.30 x f + 5 (normal operation)
   I_{CC} max. = 0.41 x f + 11 (sleep mode)
6. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.
7. Incremented if data is written to or erased from the ROM or data flash for data storage during the program execution.
8. The values are for reference.
9. This can be applied when the RES# pin is held low at power-on.



Note: * Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 5.10 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

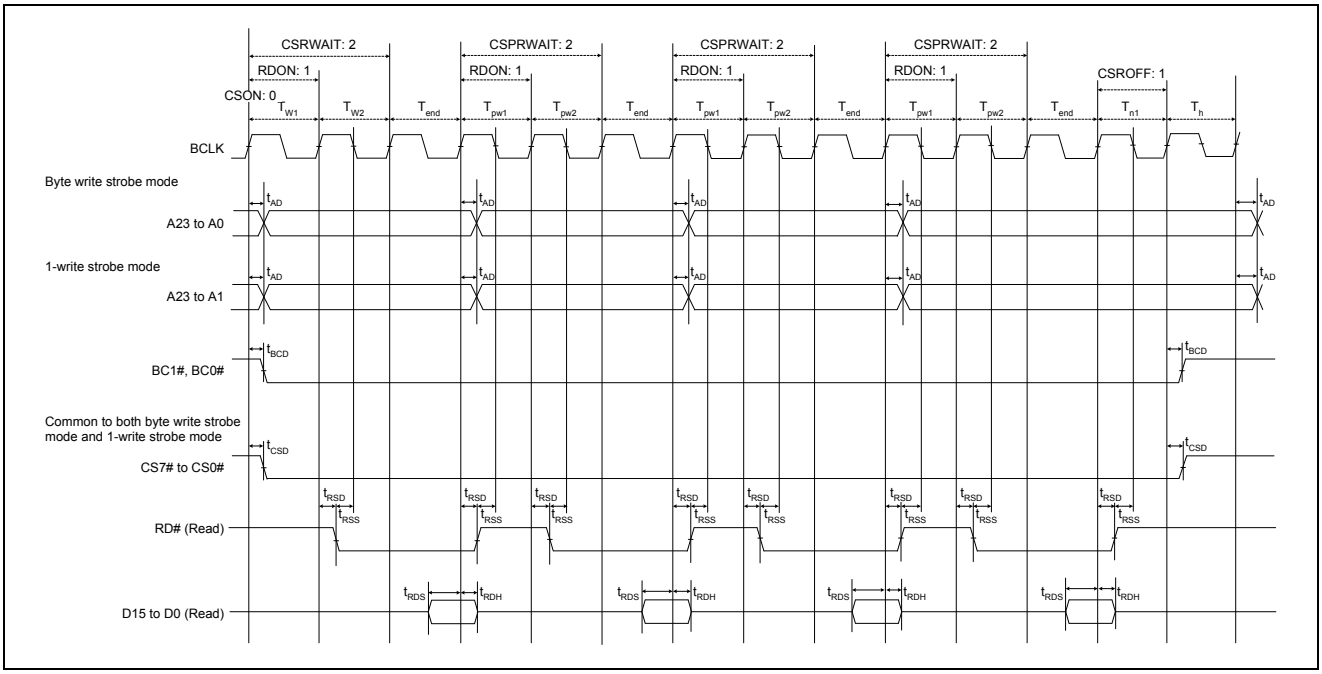


Figure 5.11 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)

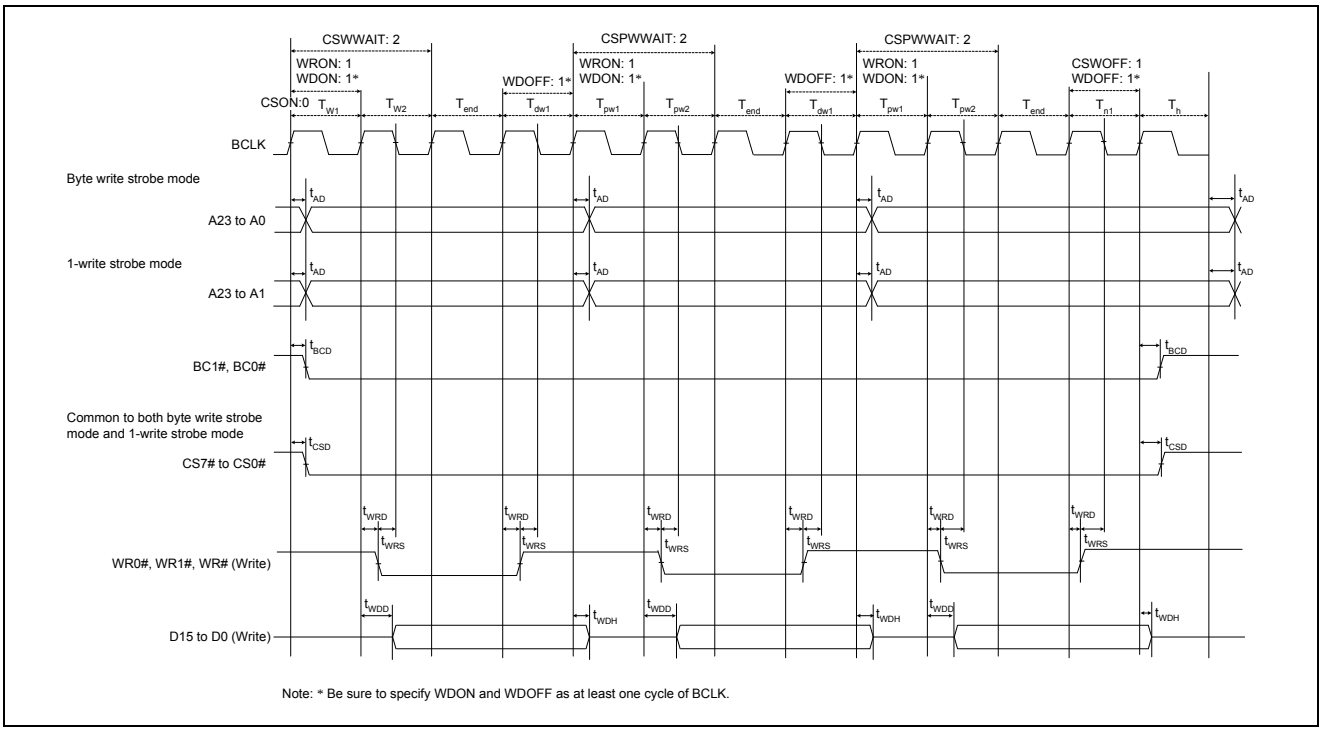


Figure 5.12 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

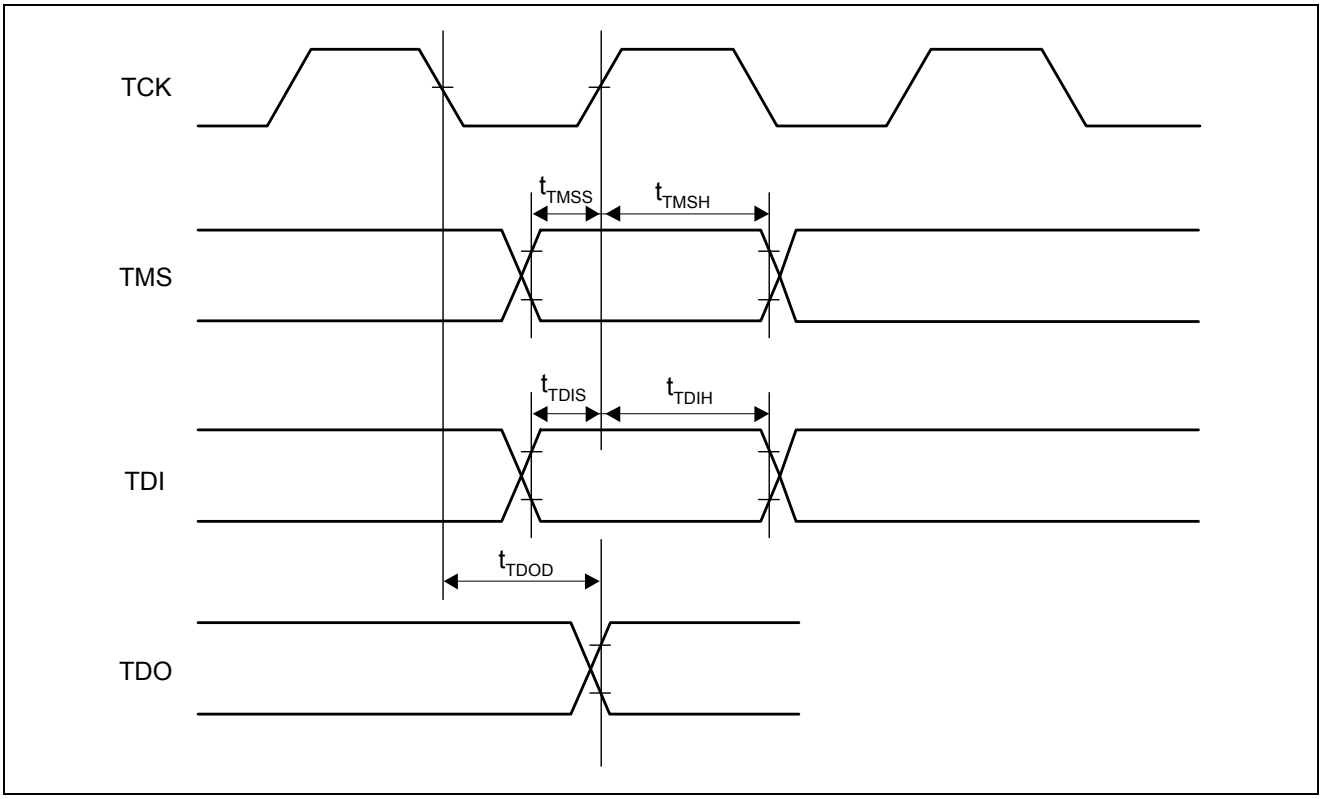


Figure 5.28 Boundary Scan Input/Output Timing

REVISION HISTORY — RX610 Group Datasheet

		Description	
Rev.	**Data**	**Page**	**Summary**
0.50	Mar. 24, 2009	–	First edition issued
1.00	Apr. 22, 2011		1. Overview
		6	Figure 1.2 Block Diagram: Ports F to H added
		7	Figure 1.3 Pin Assignment of the 176-pin LFBGA, added
		10 to 15	Table 1.3 List of Pins and Pin Functions (176-Pin LFBGA), added
			Table 1.5 Pin Functions:
		21, 25	Description on the BSCANP, PF0 to PF6, PG0 to PG7, and PH0 to PH7 pins added
			4. I/O Registers
		34 to 54	Table 4.1 List of I/O Registers (Address Order), changed
			5. Electrical Characteristics
		58	Table 5.3 Permissible Output Currents, changed
		59	Table 5.5 Clock Timing: Oscillation settling time after leaving deep software standby mode (crystal), $t_{OSC3,}$ added
		60	Figure 5.2 Oscillation Settling Timing after Software Standby Mode, changed
		61	Figure 5.3 Oscillation Settling Timing after Deep Software Standby Mode, added
		71	Table 5.8 Timing of On-Chip Peripheral Modules (3), changed
		75	Figure 5.26 Boundary Scan TCK Timing, added
		75	Figure 5.27 Boundary Scan TRST# Timing, added
		76	Figure 5.28 Boundary Scan Input/Output Timing, added
1.20	Feb.20, 2013		1. Overview
		5	Table 1.2 List of Products, product lineup added
		23, 26	Table 1.5 Pin Functions, description on bus control changed, note added
			5. I/O register
		35 to 55	Table 5.1 List of I/O Registers (Address Order), changed

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