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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	12K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 25x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l162vdt6

2.1 Device overview

Table 1. Ultra-low-power STM32L162xD device features and peripheral counts

Peripheral		STM32L162RD	STM32L162VD	STM32L162QD	STM32L162ZD
Flash (Kbytes)		384			
Data EEPROM (KBytes)		12			
RAM (Kbytes)		48			
AES		1			
FSMC		No	Multiplexed only	Yes	
Timers	32 bit	1			
	General-purpose	6			
	Basic	2			
Communication interfaces	SPI	8(3)(1)			
	I^2S	2			
	I^2C	2			
	USART	5			
	USB	1			
	SDIO	1			
GPIOs		51	83	109	115
Operation amplifiers		3			
12-bit synchronized ADC Number of channels		1 21	1 25	1 40	
12-bit DAC Number of channels		2 2			
LCD COM x SEG		1 4x32 or 8x28	1 4x44 or 8x40		
Comparators		2			
Capacitive sensing channels		23	23	33	34
Max. CPU frequency		32 MHz			
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option			

from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode. See *Table 68: Temperature sensor calibration values*.

3.11.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value (when no external voltage, VREF+, is available for ADC). The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode. See *Table 14: Embedded internal reference voltage calibration values*.

3.12 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This dual digital Interface supports the following features:

- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channels, independent or simultaneous conversions
- DMA capability for each channel (including the underrun interrupt)
- External triggers for conversion
- Input reference voltage V_{REF+}

Eight DAC trigger inputs are used in the STM32L162xD devices. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.13 Operational amplifier

The STM32L162xD devices embed three operational amplifiers with external or internal follower routing capability (or even amplifier and filter capability with external components). When one operational amplifier is selected, one external ADC channel is used to enable output measurement.

Reliable touch sensing functionality can be quickly and easily implemented using the free STM32L1xx STMTouch touch sensing firmware library.

3.17 AES

The AES Hardware Accelerator can be used to encrypt and decrypt data using the AES algorithm (compatible with FIPS PUB 197, 2001 Nov 26).

- Key scheduler
- Key derivation for decryption
- 128-bit data block processed
- 128-bit key length
- 213 clock cycles to encrypt/decrypt one 128-bit block
- Electronic codebook (ECB), cypher block chaining (CBC), and counter mode (CTR) supported by hardware.

AES data flow can be served by 2ch (D_{IN}/D_{OUT}) of the DMA2 controller

3.18 Timers and watchdogs

The ultra-low-power STM32L162xD devices include seven general-purpose timers, two basic timers, and two watchdog timers.

Table 5 compares the features of the general-purpose and basic timers.

Table 5. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3, TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM5	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM9	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.18.1 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM9, TIM10 and TIM11)

There are seven synchronizable general-purpose timers embedded in the STM32L162xD devices (see *Table 5* for differences).

Table 8. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	..	AFIO11	AFIO12	..	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4/5	TIM9/ 10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5		LCD	FSMC/ SDIO		CPRI	SYSTEM
PG5	-	-	-	-	-	-	-	-	-		-	A15		-	EVENT OUT
PG6	-	-	-	-	-	-	-	-	-		-	-		-	EVENT OUT
PG7	-	-	-	-	-	-	-	-	-		-	-		-	EVENT OUT
PG8	-	-	-	-	-	-	-	-	-		-	-		-	EVENT OUT
PG9	-	-	-	-	-	-	-	-	-		-	NE2		-	EVENT OUT
PG10	-	-	-	-	-	-	-	-	-		-	NE3		-	EVENT OUT
PG11	-	-	-	-	-	-	-	-	-		-	-		-	EVENT OUT
PG12	-	-	-	-	-	-	-	-	-		-	NE4		-	EVENT OUT
PG13	-	-	-	-	-	-	-	-	-		-	A24		-	EVENT OUT
PG14	-	-	-	-	-	-	-	-	-		-	A25		-	EVENT OUT
PG15	-	-	-	-	-	-	-	-	-		-	-		-	EVENT OUT
PH0OSC_IN	-	-	-	-	-	-	-	-	-		-	-		-	-
PH1OSC_OUT	-	-	-	-	-	-	-	-	-		-	-		-	-
PH2	-	-	-	-	-	-	-	-	-		-	A22		-	-

Table 18. Current consumption in Sleep mode

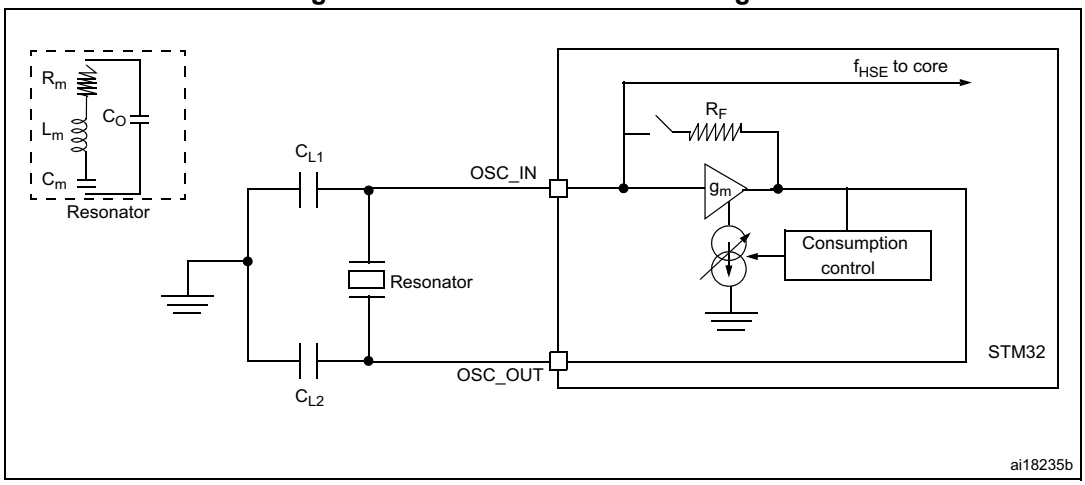
Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max (1)	Unit
$I_{DD(SLEEP)}$	Supply current in Sleep mode, code executed from RAM, Flash switched OFF	f_{HSE} = f_{HCLK} up to 16 MHz, included f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range3, Vcore=1.2 V VOS[1:0]=11	1	58	220	µA
				2	96	300	
				4	170	380	
			Range2, Vcore=1.5 V VOS[1:0]=10	4	210	500	
				8	400	700	
				16	810	1100	
			Range1, Vcore=1.8 V VOS[1:0]=01	8	485	800	
				16	955	1250	
				32	2100	2700	
		HSI clock source (16 MHz)	Range2, Vcore=1.5 V VOS[1:0]=10	16	835	1100	
			Range1, Vcore=1.8 V VOS[1:0]=01	32	2100	2700	
		MSI clock, 65 kHZ	Range3, Vcore=1.2 V VOS[1:0]=11	0.065	18.5	72	
		MSI clock, 524 kHZ		0.524	37	92	
		MSI clock, 4.2 MHZ		4.2	180	273	
	Supply current in Sleep mode, Flash switched ON	f_{HSE} = f_{HCLK} up to 16 MHz, included f_{HSE} = f_{HCLK}/2 above 16MHz (PLL ON)(2)	Range3, Vcore=1.2 V VOS[1:0]=11	1	75	250	
				2	115	300	
				4	200	380	
			Range2, Vcore=1.5 V VOS[1:0]=10	4	230	500	
				8	430	700	
				16	840	1120	
			Range1, Vcore=1.8 V VOS[1:0]=01	8	500	800	
				16	980	1300	
				32	2100	2700	
		HSI clock source (16 MHz)	Range2, Vcore=1.5 V VOS[1:0]=10	16	860	1160	
			Range1, Vcore=1.8 V VOS[1:0]=01	32	2150	2800	
		MSI clock, 65 kHZ	Range3, Vcore=1.2 V VOS[1:0]=11	0.065	33,5	90	
		MSI clock, 524 kHZ		0.524	53	110	
		MSI clock, 4.2 MHZ		4.2	200	290	

1. Guaranteed by characterization results, unless otherwise specified.

Table 23. Peripheral current consumption(1) (continued)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}= 1.8 V VOS[1:0] = 01	Range 2, V_{CORE}= 1.5 V VOS[1:0] = 10	Range 3, V_{CORE}= 1.2 V VOS[1:0] = 11	Low-power sleep and run	
APB2	SYSCFG & RI	3.5	2.9	2.4	2.9	µA/MHz (f_{HCLK})
	TIM9	9.0	7.4	5.8	7.4	
	TIM10	7.1	5.8	4.6	5.8	
	TIM11	6.5	5.3	4.3	5.3	
	ADC(2)	11.0	9.1	7.2	9.1	
	SDIO	28.4	24.2	19.1	24.2	
	SPI1	5.1	4.2	3.3	4.2	
	USART1	9.4	7.8	6.1	7.8	
AHB	GPIOA	7.3	6.1	4.8	6.1	
	GPIOB	7.5	6.1	4.8	6.1	
	GPIOC	8.2	6.8	5.3	6.8	
	GPIOD	8.7	7.1	5.7	7.1	
	GPIOE	7.6	6.2	4.9	6.2	
	GPIOF	7.7	6.3	5.0	6.3	
	GPIOG	8.4	7.0	5.4	7.0	
	GPIOH	1.8	1.3	1.1	1.3	
	CRC	0.8	0.6	0.4	0.6	
	AES	5	4	3	4	
	FLASH	26.3	19.3	18.3	-(3)	
	DMA1	19.0	16.0	12.8	16.0	
	DMA2	17.0	14.5	11.5	14.5	
All enabled		315	250	220	230.7	

Figure 16. HSE oscillator circuit diagram



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 28*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 28. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low speed external oscillator frequency	-	-	32.768	-	kHz
R_F	Feedback resistor	-	-	1.2	-	MΩ
$C^{(2)}$	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 kΩ	-	8	-	pF
I_{LSE}	LSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS}	-	-	1.1	µA
$I_{DD\ (LSE)}$	LSE oscillator current consumption	V_{DD} = 1.8 V	-	450	-	nA
		V_{DD} = 3.0 V	-	600	-	
		V_{DD} = 3.6V	-	750	-	
g_m	Oscillator transconductance	-	3	-	-	µA/V
$t_{SU(LSE)}$(4)	Startup time	V_{DD} is stabilized	-	1	-	s

1. Guaranteed by characterization results.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA with the non-standard V_{OL}/V_{OH} specifications given in *Table 50*.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $I_{VDD(\Sigma)}$ (see *Table 10*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating $I_{VSS(\Sigma)}$ (see *Table 10*).

Output voltage levels

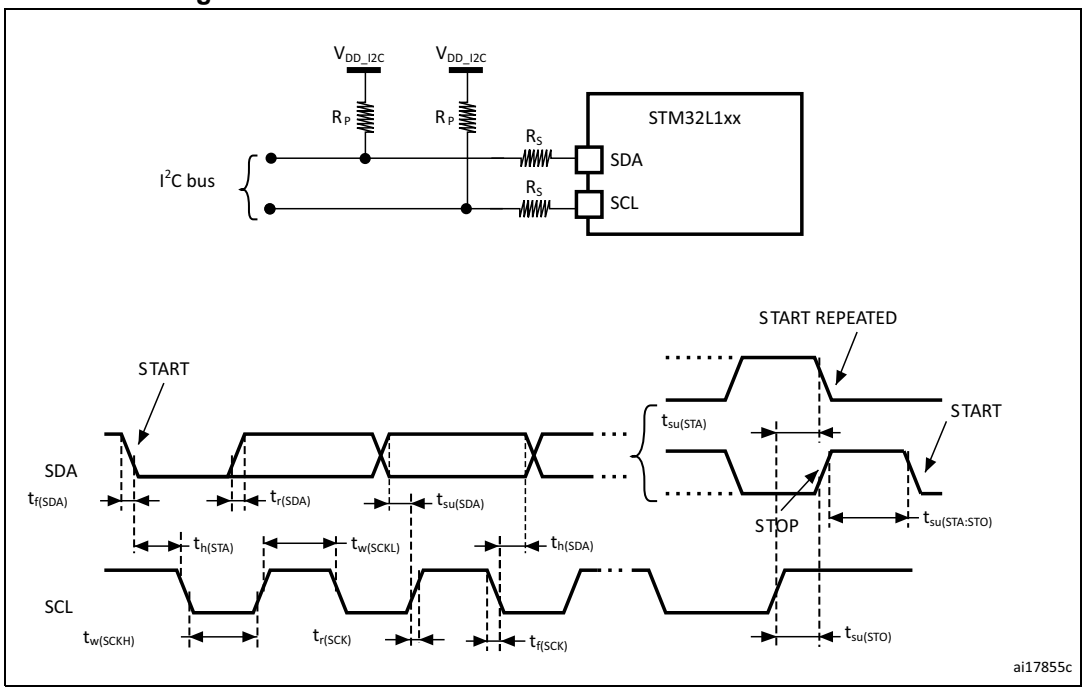
Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the conditions summarized in *Table 12*. All I/Os are CMOS and TTL compliant.

Table 50. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (1)(2)	Output low level voltage for an I/O pin	I_{IO} = 8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (2)(3)	Output high level voltage for an I/O pin		V_{DD}-0.4	-	
V_{OL} (3)(4)	Output low level voltage for an I/O pin	I_{IO} = 4 mA 1.65 V < V_{DD} < 3.6 V	-	0.45	
V_{OH} (3)(4)	Output high level voltage for an I/O pin		V_{DD}-0.45	-	
V_{OL} (1)(4)	Output low level voltage for an I/O pin	I_{IO} = 20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH} (3)(4)	Output high level voltage for an I/O pin		V_{DD}-1.3	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 10* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. Guaranteed by test in production.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 10* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed by characterization results.

Figure 28. I²C bus AC waveforms and measurement circuit



1. R_S = series protection resistor.
2. R_P = external pull-up resistor.
3. V_{DD_I2C} is the I2C bus power supply.
4. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 55. SCL frequency (f_{PCLK1}= 32 MHz, V_{DD} = V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801B
300	0x8024
200	0x8035
100	0x00A0
50	0x0140
20	0x0320

1. R_P = External pull-up resistance, f_{SCL} = I²C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed is ±2%. These variations depend on the accuracy of the external components used to design the application.

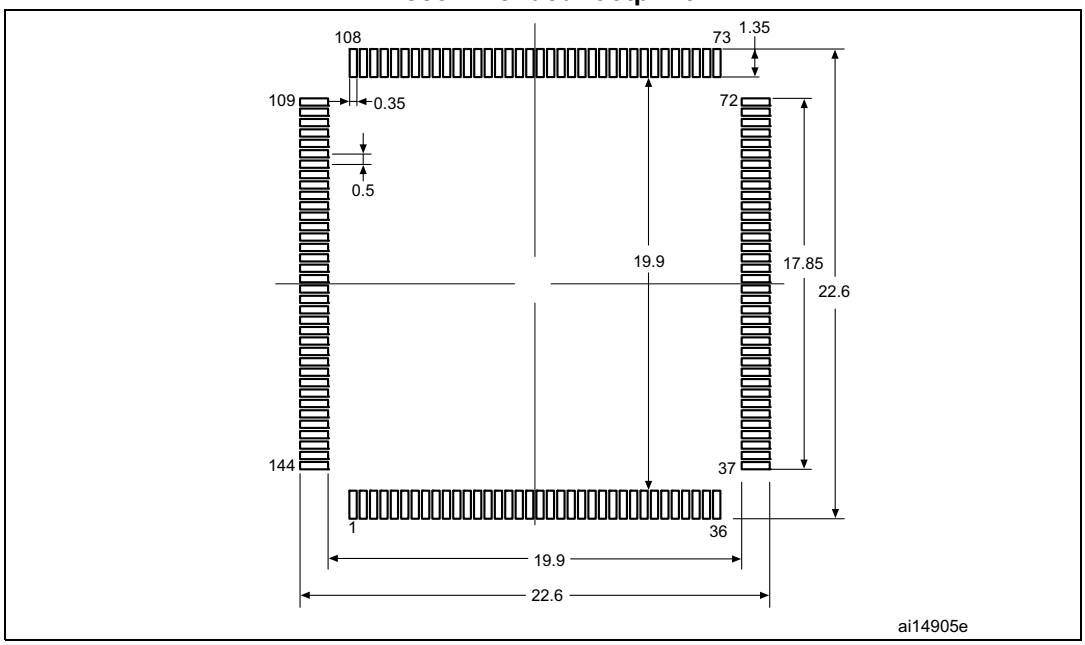
6.3.20 DAC electrical specifications

Data guaranteed by design, unless otherwise specified.

Table 66. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{REF+}	Reference supply voltage	V_{REF+} must always be below V_{DDA}	1.8	-	3.6	
V_{REF-}	Lower reference voltage	-	V_{SSA}			
$I_{DDVREF+}$(1)	Current consumption on V_{REF+} supply V_{REF+} = 3.3 V	No load, middle code (0x800)	-	130	220	µA
		No load, worst code (0x000)	-	220	350	
I_{DDA}(1)	Current consumption on V_{DDA} supply V_{DDA} = 3.3 V	No load, middle code (0x800)	-	210	320	
		No load, worst code (0xF1C)	-	320	520	
R_L(2)	Resistive load	DAC output buffer ON	5	-	-	kΩ
C_L(2)	Capacitive load		-	-	50	pF
R_O	Output impedance	DAC output buffer OFF	12	16	20	kΩ
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON	0.2	-	V_{DDA} – 0.2	V
		DAC output buffer OFF	0.5	-	V_{REF+} – 1LSB	mV
DNL(1)	Differential non linearity(3)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	1.5	3	LSB
		No R_L, $C_L \leq 50$ pF DAC output buffer OFF	-	1.5	3	
INL(1)	Integral non linearity(4)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	2	4	
		No R_L, $C_L \leq 50$ pF DAC output buffer OFF	-	2	4	
Offset(1)	Offset error at code 0x800 (5)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	±10	±25	
		No R_L, $C_L \leq 50$ pF DAC output buffer OFF	-	±5	±8	
Offset1(1)	Offset error at code 0x001(6)	No R_L, $C_L \leq 50$ pF DAC output buffer OFF	-	±1.5	±5	

Figure 41. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package recommended footprint

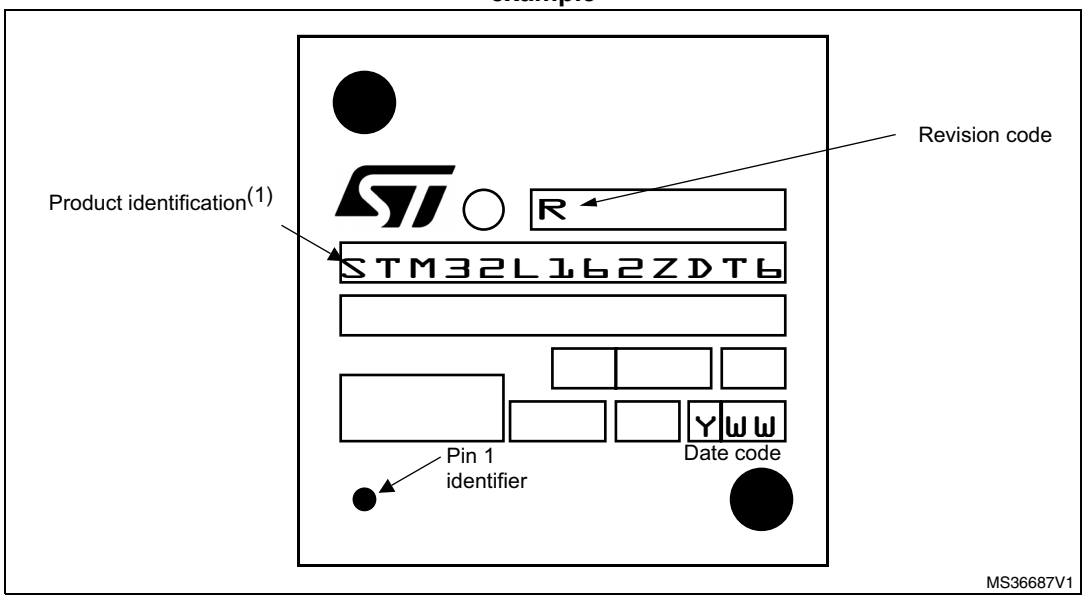


1. Dimensions are in millimeters.

Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 42. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package top view example



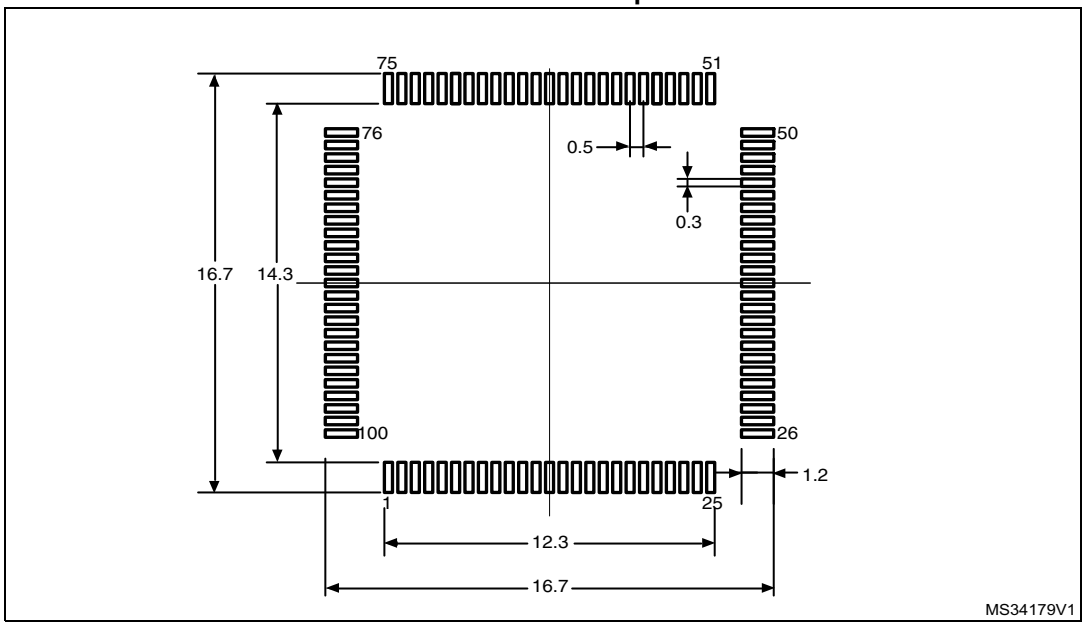
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity

Table 74. LQPF100, 14 x 14 mm, 100-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package recommended footprint

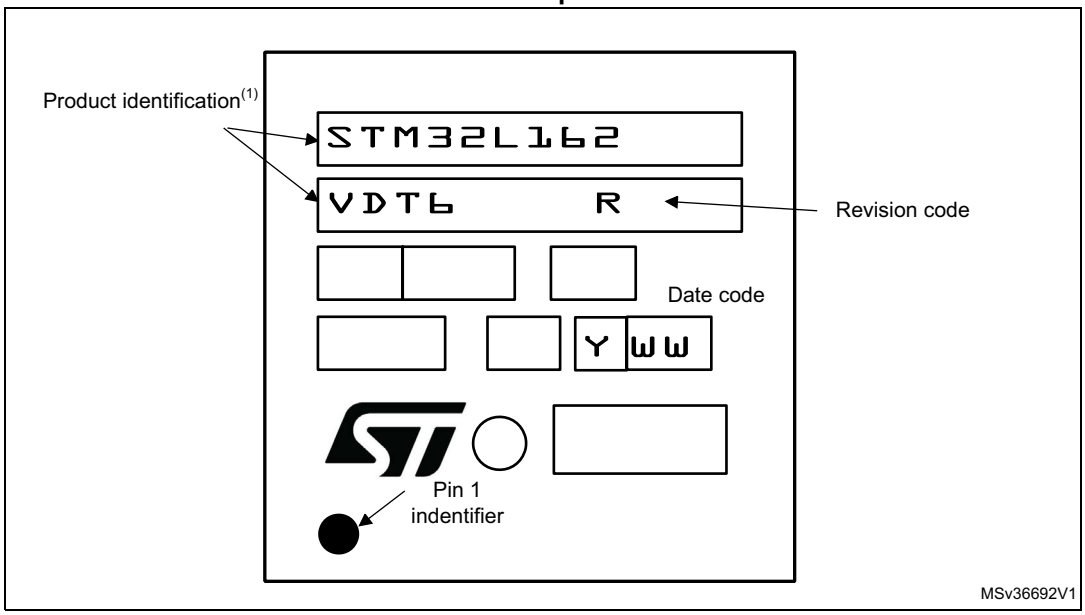


1. Dimensions are in millimeters.

Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 45. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package top view example



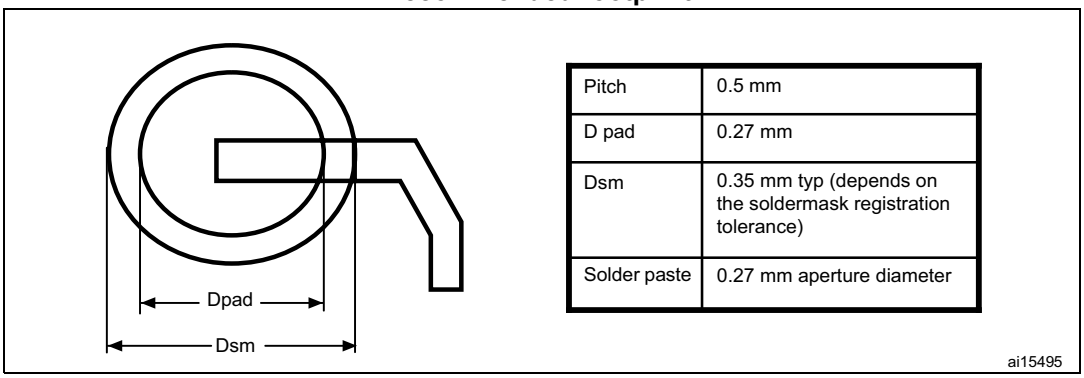
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity

Table 76. UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

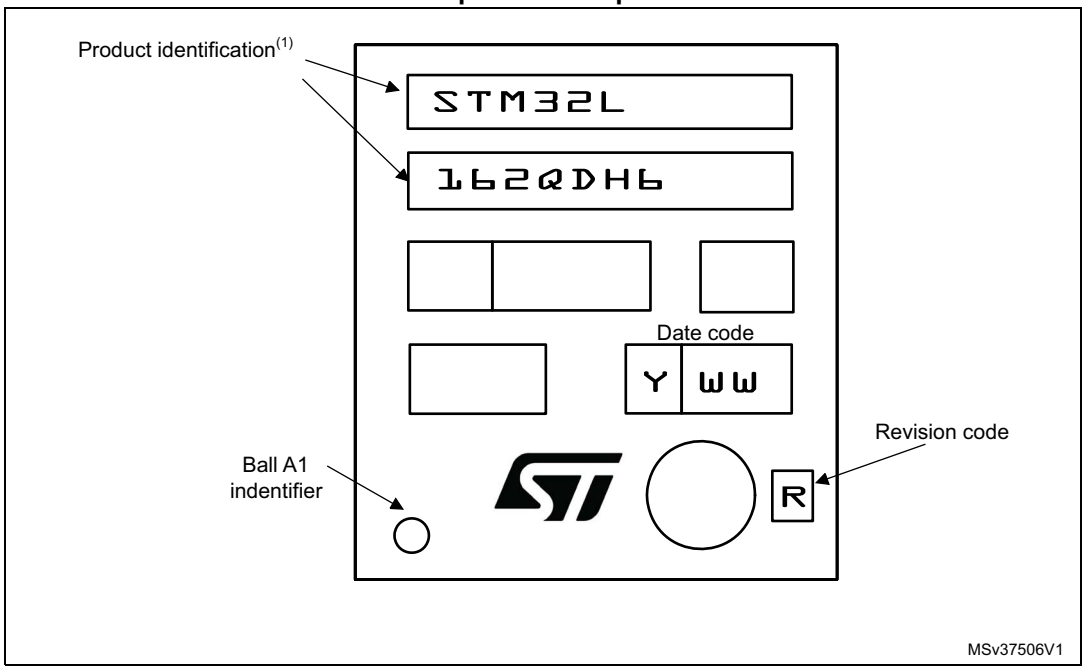
Figure 50. UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package recommended footprint



Marking of engineering samples

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

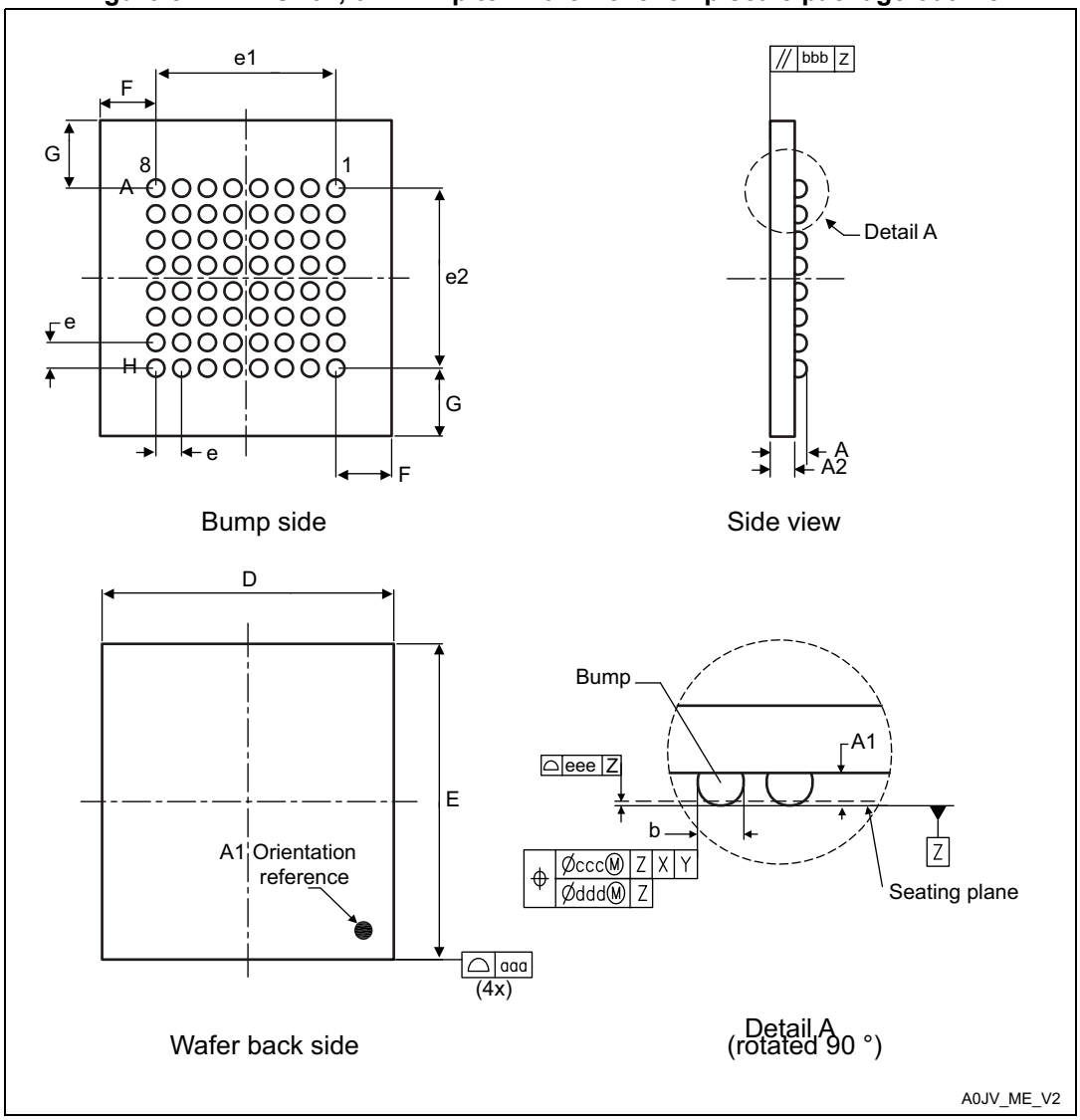
Figure 51. UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity

7.5 WLCSP64, 0.4 mm pitch wafer level chip scale package information

Figure 52. WLCSP64, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

Table 77. WLCSP64, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.540	0.570	0.600	0.0205	0.0224	0.0236
A1	-	0.190	-	-	0.0075	-
A2	-	0.380	-	-	0.0150	-

Table 81. Document revision history (continued)

Date	Revision	Changes
06-Feb-2013	4	Removed AHB1/AHB2 and corrected typo on APB1/APB2 in *Figure 1: Ultra-low-power STM32L162xC block diagram* Updated “OP amp” line in *Table 4: Functionalities depending on the working mode (from Run/active down to standby)* Added IWDG and WWDG rows in *Table 4: Functionalities depending on the working mode (from Run/active down to standby)* Added OneNAND support in *Section 3.8: FSMC (flexible static memory controller)* The comment "HSE = 16 MHz(2) (PLL ON for fHCLK above 16 MHz)" replaced by "fHSE = fHCLK up to 16 MHz included, fHSE = fHCLK/2 above 16 MHz (PLL ON)(2)” in table *Table 19: Current consumption in Sleep mode* Updated Stop mode current to 1.5 µA in *Ultra-low-power platform* Replaced BGA132 by UFBGA132 in *Table 5: Ultralow power STM32L162xD device features and peripheral counts* Replaced BGA132 by UFBGA132 in *Figure 4: STM32L15xQD STM32L162QD UFBGA132 ballout* Updated entire *Section 7: Package characteristics* Updated *Figure 34: Typical connection diagram using the ADC* and definition of symbol “R_{AIN}” in *Table 67: ADC characteristics* Removed first sentence in *Section : I2C interface characteristics*
13-June-2014	5	Updated *Table 14: Embedded internal reference voltage calibration values* and moved inside *Section 6.3.3: Embedded internal reference voltage*. Updated I_{DD} (WU from Standby) unit in *Table 22: Typical and maximum current consumptions in Standby mode* Updated*Figure 5: Pin loading conditions* Updated *Figure 6: Pin input voltage*. Updated *Figure 17: Typical application with a 32.768 kHz crystal*Updated *Figure 27: Recommended NRST pin protection* Updated *Figure 28: I2C bus AC waveforms and measurement circuit* Updated *Table 68: Temperature sensor calibration values* and moved inside *Section 6.3.22: Temperature sensor characteristics*.. Updated *Figure 11: Power supply scheme*. Updated *Table 9: Voltage characteristics* added row. Updated *Table 10: Current characteristics*. Updated *Table 12: General operating conditions*, footnote and added row. Updated *Section 6.3.4: Supply current characteristics*. Updated *Table 16: Current consumption in Run mode, code with data processing running from Flash*. Updated *Table 17: Current consumption in Run mode, code with data processing running from RAM*. Created *Section 6.3.5: Wakeup time from low-power mode*. Updated *Table 75: LQFP64, 10 x 10 mm 64-pin low-profile quad flat package mechanical data* and *Table 76: UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package mechanical data* exchange Min and Typ values inside columns.