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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-4
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	EBI/EMI, FIFO, SCI, SmartCard
Peripherals	DMA, POR, WDT
Number of I/O	39
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-BBGA
Supplier Device Package	256-BGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d6417751rba240hvu0

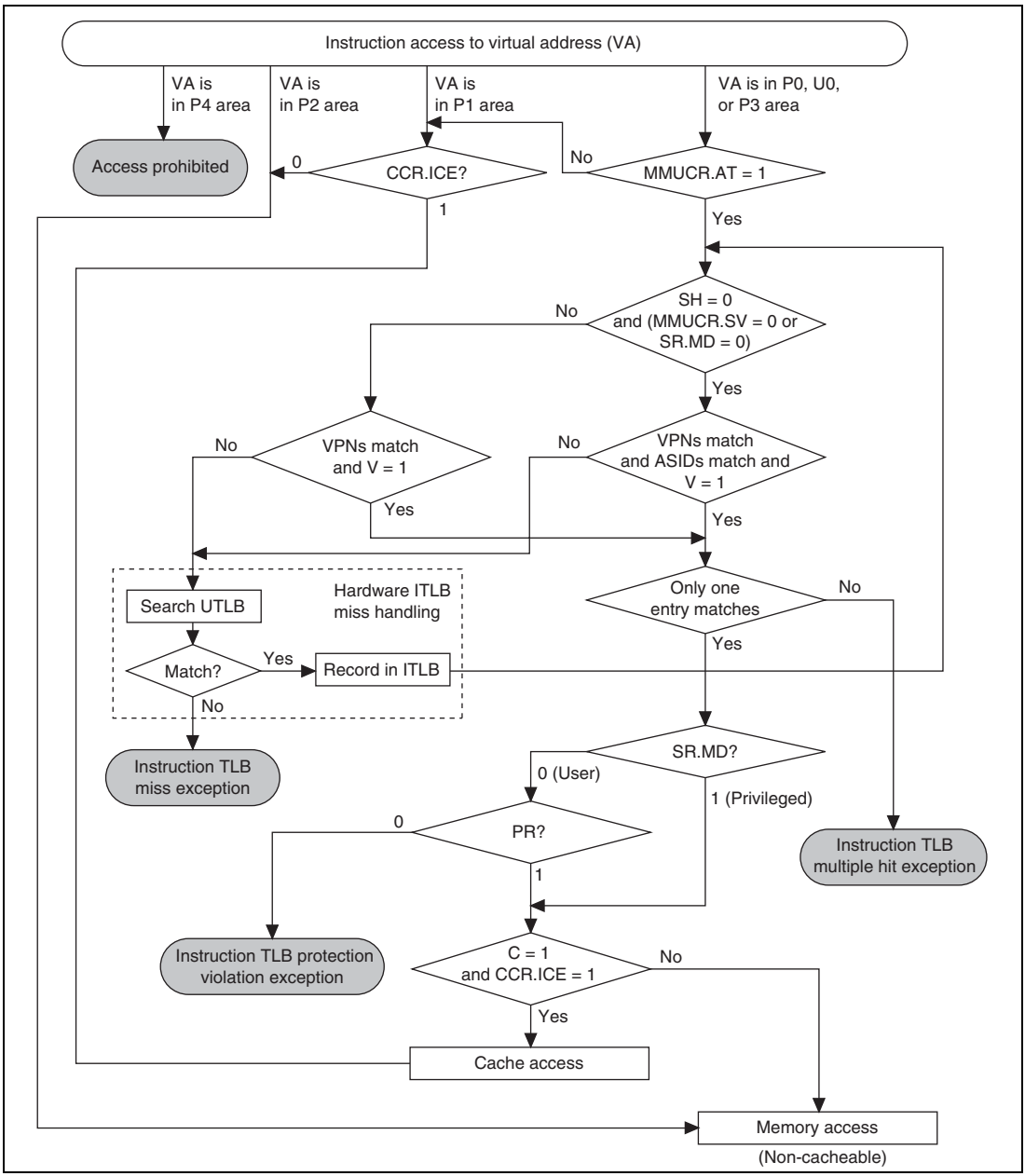


Figure 3.11 Flowchart of Memory Access Using ITLB

When a write is performed with the A bit in the address field set to 1, comparison of all the UTLB entries is carried out using the VPN specified in the data field and PTEH.ASID. The usual address comparison rules are followed, but if a UTLB miss occurs, the result is no operation, and an exception is not generated. If the comparison identifies a UTLB entry corresponding to the VPN specified in the data field, D and V specified in the data field are written to that entry. If there is more than one matching entry, a data TLB multiple hit exception results. This associative operation is simultaneously carried out on the ITLB, and if a matching entry is found in the ITLB, V is written to that entry. Even if the UTLB comparison results in no operation, a write to the ITLB side only is performed as long as there is an ITLB match. If there is a match in both the UTLB and ITLB, the UTLB information is also written to the ITLB.

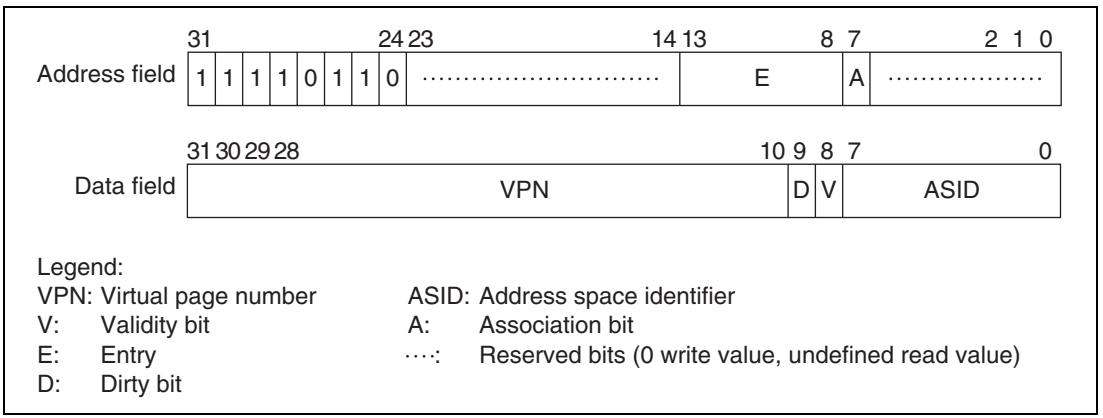


Figure 3.16 Memory-Mapped UTLB Address Array

3.7.5 UTLB Data Array 1

UTLB data array 1 is allocated to addresses H'F700 0000 to H'F77F FFFF in the P4 area. A data array access requires a 32-bit address field specification (when reading or writing) and a 32-bit data field specification (when writing). Information for selecting the entry to be accessed is specified in the address field, and PPN, V, SZ, PR, C, D, SH, and WT to be written to the data array are specified in the data field.

In the address field, bits [31:23] have the value H'F70 indicating UTLB data array 1, and the entry is selected by bits [13:8].

In the data field, PPN is indicated by bits [28:10], V by bit [8], SZ by bits [7] and [4], PR by bits [6:5], C by bit [3], D by bit [2], SH by bit [1], and WT by bit [0].

The following two kinds of operation can be used on UTLB data array 1:

1. General Pipeline

I	D	EX	NA	S
• Instruction fetch	• Instruction decode • Issue • Register read • Destination address calculation for PC-relative branch	• Operation	• Non-memory data access	• Write-back

2. General Load/Store Pipeline

I	D	EX	MA	S
• Instruction fetch	• Instruction decode • Issue • Register read	• Address calculation	• Memory data access	• Write-back

3. Special Pipeline

I	D	SX	NA	S
• Instruction fetch	• Instruction decode • Issue • Register read	• Operation	• Non-memory data access	• Write-back

4. Special Load/Store Pipeline

I	D	SX	MA	S
• Instruction fetch	• Instruction decode • Issue • Register read	• Address calculation	• Memory data access	• Write-back

5. Floating-Point Pipeline

I	D	F1	F2	FS
• Instruction fetch	• Instruction decode • Issue • Register read	• Computation 1	• Computation 2	• Computation 3 • Write-back

6. Floating-Point Extended Pipeline

I	D	F0	F1	F2	FS
• Instruction fetch	• Instruction decode • Issue • Register read	• Computation 0	• Computation 1	• Computation 2	• Computation 3 • Write-back

7. FDIV/FSQRT Pipeline

F3

Computation: Takes several cycles

Figure 8.1 Basic Pipelines

Functional Category	No.	Instruction		Instruction Group	Issue Rate	Latency	Execution Pattern	Lock		
								Stage	Start	Cycles
Single-precision floating-point instructions	182	FABS	FRn	LS	1	0	#1	—	—	—
	183	FADD	FRm,FRn	FE	1	3/4	#36	—	—	—
	184	FCMP/EQ	FRm,FRn	FE	1	2/4	#36	—	—	—
	185	FCMP/GT	FRm,FRn	FE	1	2/4	#36	—	—	—
	186	FDIV	FRm,FRn	FE	1	12/13	#37	F3	2	10
								F1	11	1
	187	FLOAT	FPUL,FRn	FE	1	3/4	#36	—	—	—
	188	FMAC	FR0,FRm,FRn	FE	1	3/4	#36	—	—	—
	189	FMUL	FRm,FRn	FE	1	3/4	#36	—	—	—
	190	FNEG	FRn	LS	1	0	#1	—	—	—
	191	FSQRT	FRn	FE	1	11/12	#37	F3	2	9
								F1	10	1
	192	FSUB	FRm,FRn	FE	1	3/4	#36	—	—	—
	193	FTRC	FRm,FPUL	FE	1	3/4	#36	—	—	—
	194	FMOV	DRm,DRn	LS	1	0	#1	—	—	—
	195	FMOV	@Rm,DRn	LS	1	2	#2	—	—	—
	196	FMOV	@Rm+,DRn	LS	1	1/2	#2	—	—	—
	197	FMOV	@(R0,Rm),DRn	LS	1	2	#2	—	—	—
	198	FMOV	DRm,@Rn	LS	1	1	#2	—	—	—
	199	FMOV	DRm,@-Rn	LS	1	1/1	#2	—	—	—
	200	FMOV	DRm,@(R0,Rn)	LS	1	1	#2	—	—	—
Double-precision floating-point instructions	201	FABS	DRn	LS	1	0	#1	—	—	—
	202	FADD	DRm,DRn	FE	1	(7, 8)/9	#39	F1	2	6
	203	FCMP/EQ	DRm,DRn	CO	2	3/5	#40	F1	2	2
	204	FCMP/GT	DRm,DRn	CO	2	3/5	#40	F1	2	2
	205	FCNVDS	DRm,FPUL	FE	1	4/5	#38	F1	2	2
	206	FCNVSD	FPUL,DRn	FE	1	(3, 4)/5	#38	F1	2	2
	207	FDIV	DRm,DRn	FE	1	(24, 25)/26	#41	F3	2	23
								F1	22	3
								F1	2	2
	208	FLOAT	FPUL,DRn	FE	1	(3, 4)/5	#38	F1	2	2
	209	FMUL	DRm,DRn	FE	1	(7, 8)/9	#39	F1	2	6

Bit 0—Module Stop 5 (MSTP5): Specifies stopping of the clock supply to the user break controller (UBC) among the on-chip peripheral modules. See section 20.6, User Break Controller Stop Function for how to set the clock supply.

Bit 0: MSTP5	Description	
0	UBC operating	(Initial value)
1	Clock supply to UBC stopped	

9.2.5 Clock Stop Register 00 (CLKSTP00)

Clock stop register 00 (CLKSTP00) is a 32-bit readable/writable register that controls the operating clock for peripheral modules.

The clock supply is restarted by writing 1 to the corresponding bit in the CLKSTPCLR00 register. Writing 0 to CLKSTP00 will not change the bit value.

CLKSTP00 is initialized to H'00000000 by a reset. It is not initialized in standby mode.

Bit:	31	30	29	...	11	10	9	8
	—	—	—	...	—	—	—	—
Initial value:	0	0	0	...	0	0	0	0
R/W:	R	R	R	...	R	R	R	R

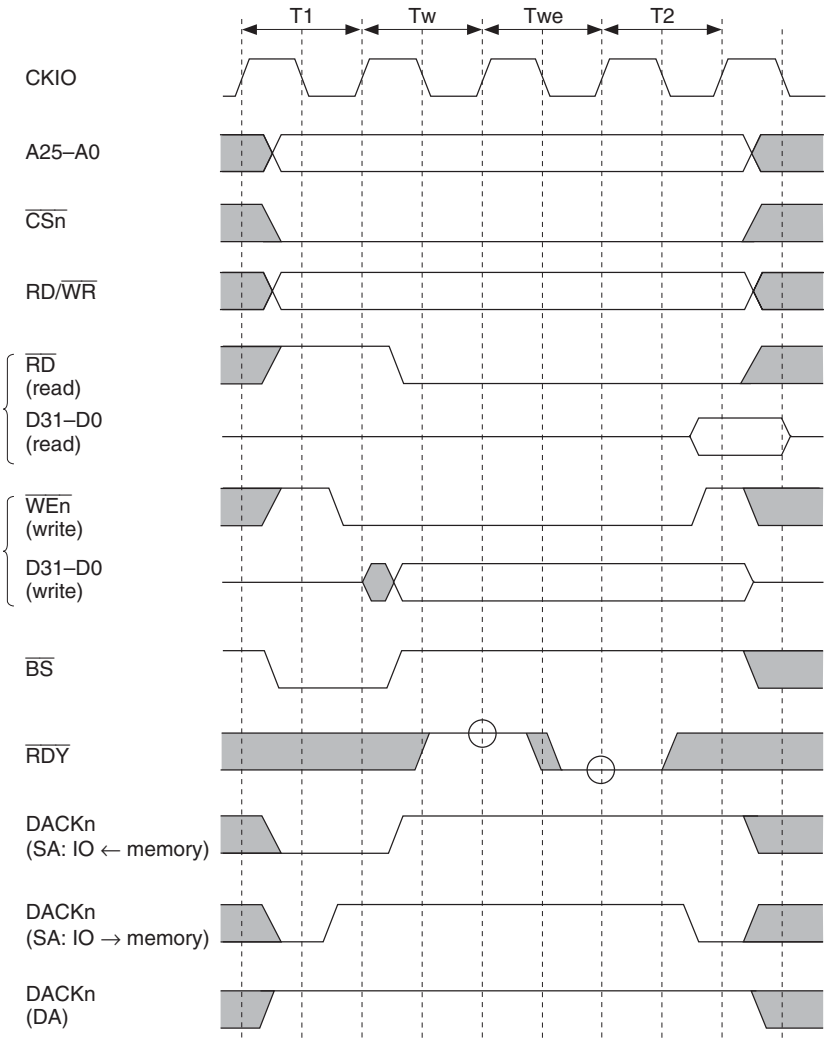
Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	CSTP2	CSTP1	CSTP0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bits 31 to 3—Reserved: These bits are always read as 0, and should only be written with 0.

Bit 2—Clock Stop 2 (CSTP2): Specifies stopping of the peripheral clock supply to the PCI bus controller (PCIC). For details see section 22, PCI Controller (PCIC).

Bit 2: CSTP2	Description	
0	Peripheral clock is supplied to PCIC	(Initial value)
1	Peripheral clock supply to PCIC is stopped	

When software wait insertion is specified by WCR2, the external wait input $\overline{\text{RDY}}$ signal is also sampled. $\overline{\text{RDY}}$ signal sampling is shown in figure 13.11. A single-cycle wait is specified as a software wait. Sampling is performed at the transition from the Tw state to the T2 state; therefore, the $\overline{\text{RDY}}$ signal has no effect if asserted in the T1 cycle or the first Tw cycle. The $\overline{\text{RDY}}$ signal is sampled on the rising edge of the clock.



Note: For DACKn, an example is shown where CHCRn.AL (access level) = 0 for the DMAC.

Figure 13.11 SRAM Interface Wait State Timing (Wait State Insertion by $\overline{\text{RDY}}$ Signal)

13.3.9 Byte Control SRAM Interface

The byte control SRAM interface is a memory interface that outputs a byte select strobe ($\overline{\text{WEn}}$) in both read and write bus cycles. It has 16 bit data pins, and can be connected to SRAM which has an upper byte select strobe and lower byte select strobe function such as UB and LB.

Areas 1 and 4 can be designated as byte control SRAM interface. However, when these areas are set to MPX mode, MPX mode has priority.

The byte control SRAM interface write timing is the same as for the normal SRAM interface.

In read operations, the $\overline{\text{WEn}}$ pin timing is different. In a read access, only the $\overline{\text{WE}}$ signal for the byte being read is asserted. Assertion is synchronized with the fall of the CKIO clock, as for the $\overline{\text{WE}}$ signal, while negation is synchronized with the rise of the CKIO clock, using the same timing as the $\overline{\text{RD}}$ signal.

32-byte transfer is performed consecutively for a total of 32 bytes according to the set bus width. The first access is performed on the data for which there was an access request. The remaining accesses are performed in wrap-around fashion on the data at the 32-byte boundary. The bus is not released during this period.

Figure 13.64 shows an example of byte control SRAM connection to this LSI, and figures 13.65 to 13.67 show examples of byte control SRAM read cycles.

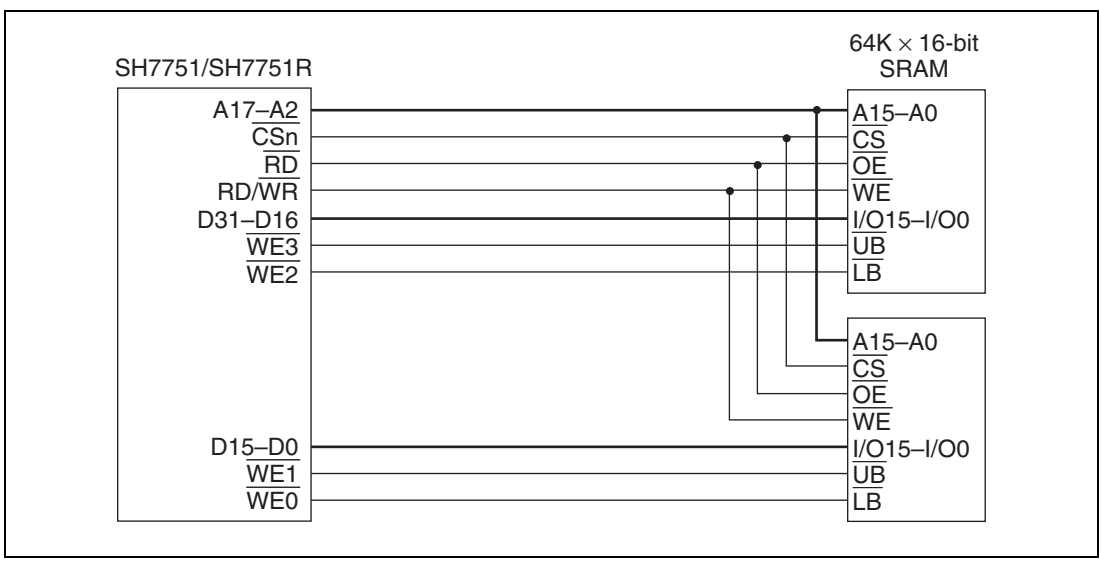


Figure 13.64 Example of 32-Bit Data Width Byte Control SRAM

Bit 19—$\overline{\text{DREQ}}$ Select (DS): Specifies either low level detection or falling edge detection as the sampling method for the $\overline{\text{DREQ}}$ pin used in external request mode.

In normal DMA mode, this bit is valid only in CHCR0 and CHCR1. In DDT mode, it is valid in CHCR0–CHCR3.

Bit 19: DS	Description	
0	Low level detection	(Initial value)
1	Falling edge detection	

Notes: Level detection burst mode when TM = 1 and DS = 0
Edge detection burst mode when TM = 1 and DS = 1

Bit 18—Request Check Level (RL): Selects whether the DRAK signal (that notifies an external device of the acceptance of $\overline{\text{DREQ}}$) is an active-high or active-low output.

In normal DMA mode, this bit is valid only in CHCR0 and CHCR1. It is invalid in DDT mode.

Bit 18: RL	Description	
0	DRAK is an active-high output	(Initial value)
1	DRAK is an active-low output	

Bit 17—Acknowledge Mode (AM): In dual address mode, selects whether DACK is output in the data read cycle or write cycle. In single address mode, DACK is always output regardless of the setting of this bit.

In normal DMA mode, this bit is valid only in CHCR0 and CHCR1. In DDT mode, it is valid in CHCR1–CHCR3. (DDT mode: TDACK)

Bit 17: AM	Description	
0	DACK is output in read cycle	(Initial value)
1	DACK is output in write cycle	

Section 15 Serial Communication Interface (SCI)

15.1 Overview

This LSI is equipped with a single-channel serial communication interface (SCI) and a single-channel serial communication interface with built-in FIFO registers (SCI with FIFO: SCIF).

The SCI can handle both asynchronous and synchronous serial communication.

The SCI supports a smart card interface. This is a serial communication function supporting a subset of the ISO/IEC 7816-3 (identification cards) standard. For details, see section 17, Smart Card Interface.

The SCIF is a dedicated asynchronous communication serial interface with built-in 16-stage FIFO registers for both transmission and reception. For details, see section 16, Serial Communication Interface with FIFO (SCIF).

15.1.1 Features

SCI features are listed below.

- Choice of synchronous or asynchronous serial communication mode
  - — Asynchronous mode

    Serial data communication is executed using an asynchronous system in which synchronization is achieved character by character. Serial data communication can be carried out with standard asynchronous communication chips such as a Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communication Interface Adapter (ACIA). A multiprocessor communication function is also provided that enables serial data communication with a number of processors.

    There is a choice of 12 serial data transfer formats.

Data length:	7 or 8 bits
Stop bit length:	1 or 2 bits
Parity:	Even/odd/none
Multiprocessor bit:	1 or 0
Receive error detection:	Parity, overrun, and framing errors
Break detection:	A break can be detected by reading the RxD pin level directly from the serial port register (SCSPTR1) when a framing error occurs.

Bit 4—Framing Error (FER): Indicates that a framing error occurred during reception in asynchronous mode, causing abnormal termination.

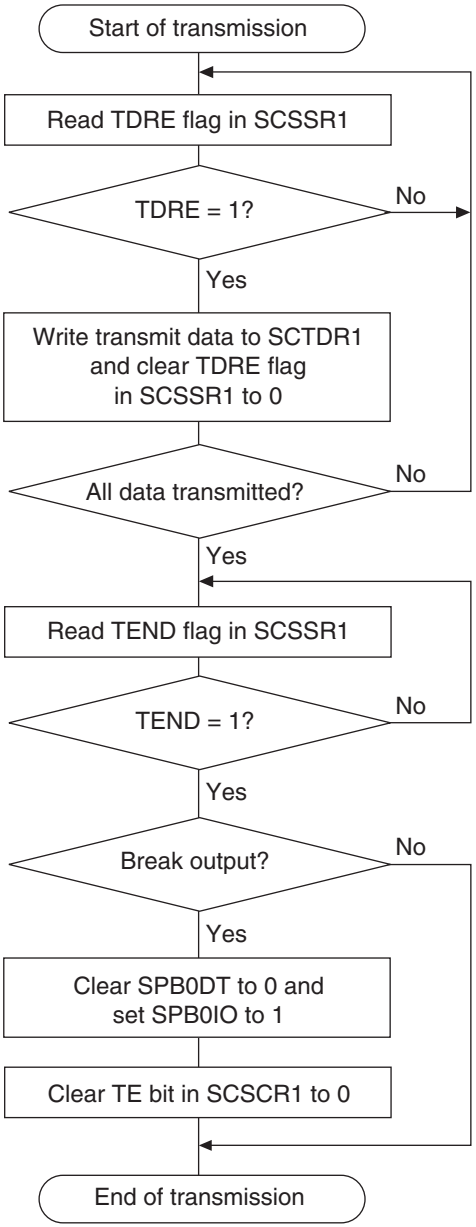
Bit 4: FER	Description
0	Reception in progress, or reception has ended normally*1 (Initial value) [Clearing conditions] • Power-on reset, manual reset, standby mode, or module standby • When 0 is written to FER after reading FER = 1
1	A framing error occurred during reception [Setting condition] When the SCI checks whether the stop bit at the end of the receive data is 1 when reception ends, and the stop bit is 0*2

Notes: 1. The FER flag is not affected and retains its previous state when the RE bit in SCSCR1 is cleared to 0.
2. In 2-stop-bit mode, only the first stop bit is checked for a value of 1; the second stop bit is not checked. If a framing error occurs, the receive data is transferred to SCRDR1 but the RDRF flag is not set. Serial reception cannot be continued while the FER flag is set to 1.

Bit 3—Parity Error (PER): Indicates that a parity error occurred during reception with parity addition in asynchronous mode, causing abnormal termination.

Bit 3: PER	Description
0	Reception in progress, or reception has ended normally*1 (Initial value) [Clearing conditions] • Power-on reset, manual reset, standby mode, or module standby • When 0 is written to PER after reading PER = 1
1	A parity error occurred during reception*2 [Setting condition] When, in reception, the number of 1-bits in the receive data plus the parity bit does not match the parity setting (even or odd) specified by the O/$\overline{E}$ bit in SCSMR1

Notes: 1. The PER flag is not affected and retains its previous state when the RE bit in SCSCR1 is cleared to 0.
2. If a parity error occurs, the receive data is transferred to SCRDR1 but the RDRF flag is not set. Serial reception cannot be continued while the PER flag is set to 1.



1. SCI status check and transmit data write: Read SCSSR1 and check that the TDRE flag is set to 1, then write transmit data to SCTDR1 and clear the TDRE flag to 0.
2. Serial transmission continuation procedure: To continue serial transmission, read 1 from the TDRE flag to confirm that writing is possible, then write data to SCTDR1, and then clear the TDRE flag to 0. (Checking and clearing of the TDRE flag is automatic when the direct memory access controller (DMAC) is activated by a transmit-data-empty interrupt (TXI) request, and data is written to SCTDR1.)
3. Break output at the end of serial transmission: To output a break in serial transmission, clear the SPB0DT bit to 0 and set the SPB0IO bit to 1 in SCSPTR, then clear the TE bit in SCSCR1 to 0.

Figure 15.8 Sample Serial Transmission Flowchart

16.2.7 Serial Status Register (SCFSR2)

Bit:	15	14	13	12	11	10	9	8
	PER3	PER2	PER1	PER0	FER3	FER2	FER1	FER0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	7	6	5	4	3	2	1	0
	ER	TEND	TDFE	BRK	FER	PER	RDF	DR
Initial value:	0	1	1	0	0	0	0	0
R/W:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/(W)*	R/(W)*

Note: * Only 0 can be written, to clear the flag.

SCFSR2 is a 16-bit register. The lower 8 bits consist of status flags that indicate the operating status of the SCIF, and the upper 8 bits indicate the number of receive errors in the data in the receive FIFO register.

SCFSR2 can be read or written to by the CPU at all times. However, 1 cannot be written to flags ER, TEND, TDFE, BRK, RDF, and DR. Also note that in order to clear these flags they must be read as 1 beforehand. The FER flag and PER flag are read-only flags and cannot be modified.

SCFSR2 is initialized to H'0060 by a power-on reset or manual reset. It is not initialized in standby mode or in the module standby state.

Bits 15 to 12—Number of Parity Errors (PER3–PER0): These bits indicate the number of data bytes in which a parity error occurred in the receive data stored in SCFRDR2.

After the ER bit in SCFSR2 is set, the value indicated by bits 15 to 12 is the number of data bytes in which a parity error occurred.

If all 16 bytes of receive data in SCFRDR2 have parity errors, the value indicated by bits PER3 to PER0 will be 0.

Bits 11 to 8—Number of Framing Errors (FER3–FER0): These bits indicate the number of data bytes in which a framing error occurred in the receive data stored in SCFRDR2.

After the ER bit in SCFSR2 is set, the value indicated by bits 11 to 8 is the number of data bytes in which a framing error occurred.

Inversion specified by the SINV bit applies only to the data bits, D7 to D0. For parity bit inversion, the O/$\overline{E}$ bit in SCSMR1 is set to odd parity mode. (This applies to both transmission and reception).

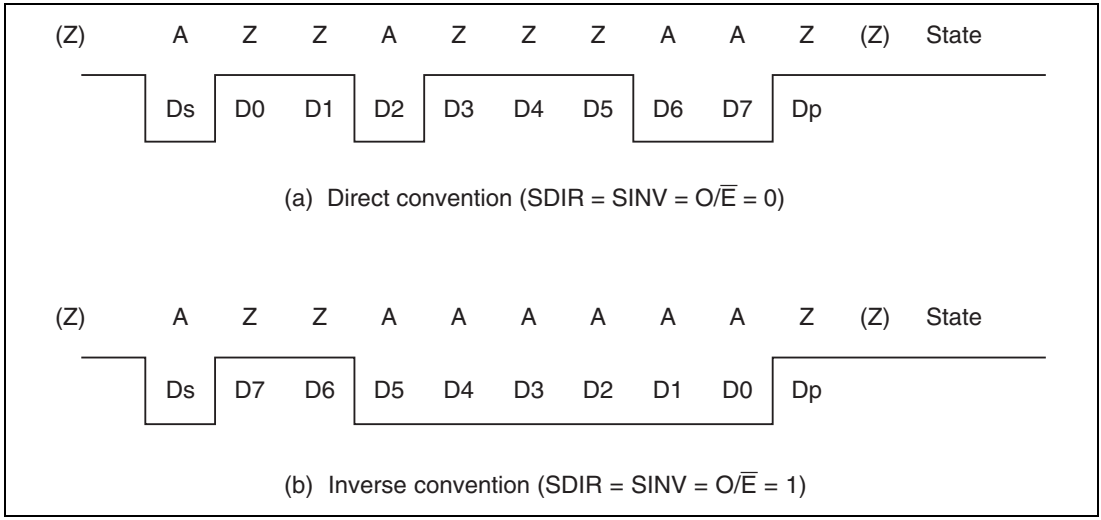


Figure 17.5 Sample Start Character Waveforms

17.3.5 Clock

Only an internal clock generated by the on-chip baud rate generator can be used as the transmit/receive clock for the smart card interface. The bit rate is set with the bit rate register (SCBRR1) and the CKS1 and CKS0 bits in the serial mode register (SCSMR1). The equation for calculating the bit rate is shown below. Table 17.5 shows some sample bit rates.

If clock output is selected with CKE0 set to 1, a clock with a frequency of 372 times the bit rate is output from the SCK pin.

$$B = \frac{Pck}{1488 \times 2^{2n-1} \times (N+1)} \times 10^6$$

Where: N = Value set in SCBRR1 ($0 \leq N \leq 255$)
B = Bit rate (bits/s)
Pck = Peripheral module operating frequency (MHz)
n = 0 to 3 (See table 17.4)

21.2 Register Descriptions

21.2.1 Instruction Register (SDIR)

The instruction register (SDIR) is a 16-bit register that can only be read by the CPU. In the initial state, bypass mode is set. The value (command) is set from the serial input pin (TDI). SDIR is initialized by the $\overline{\text{TRST}}$ pin or in the TAP Test-Logic-Reset state. When this register is written to from the H-UDI, writing is possible regardless of the CPU mode. Operation is undefined if a reserved command is set in this register.

Bit:	15	14	13	12	11	10	9	8
	TI7	TI6	TI5	TI4	TI3	TI2	TI1	TI0
Initial value:	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R

Bits 15 to 8—Test Instruction Bits (TI7–TI0)

Bit 15: TI7	Bit 14: TI6	Bit 13: TI5	Bit 12: TI4	Bit 11: TI3	Bit 10: TI2	Bit 9: TI1	Bit 8: TI0	Description
0	0	0	0	0	0	0	0	EXTEST
0	0	0	0	0	1	0	0	SAMPLE/PRELOAD
0	1	1	0	—	—	—	—	H-UDI reset negate
0	1	1	1	—	—	—	—	H-UDI reset assert
1	0	1	—	—	—	—	—	H-UDI interrupt
1	1	1	1	1	1	1	1	Bypass mode (Initial value)
Other than above								Reserved

Bits 7 to 0—Reserved: These bits are always read as 1, and should only be written with 1.

Bit 3—Special Cycle Control (SPC): Shows whether special cycles are supported when the PCIC is operating as a target.

Bit 3: SPC	Description	
0	Ignore special cycle	(Initial value)
1	Monitor special cycle (not supported)	

Bit 2—PCI Bus Master Control (BUM): Controls the bus master operation.

Bit 2: BUM	Description	
0	Disable bus master operation	(Initial value)
1	Enable bus master operation	

Bit 1—Memory Space Control (MES): Controls the access to the memory space when the PCIC is operating as a target. When this bit is 0, all memory transfers to the PCIC are terminated by master abort.

Bit 1: MES	Description	
0	Disable access to memory space	(Initial value)
1	Enable access to memory space	

Bit 0—I/O Space Control (IOS): Controls the access to the I/O space when the PCIC is operating as a target. When this bit is 0, all I/O transfers to the PCIC are terminated by master abort.

Bit 0: IOS	Description	
0	Disable access to I/O space	(Initial value)
1	Enable access to I/O space	

23.3.3 Bus Timing

Table 23.21 Bus Timing (1)

		HD6417751 RBP240 (V) HD6417751 RBG240 (V) HD6417751 RBA240HV		HD6417751 RBP200 (V) HD6417751 RBG200 (V) HD6417751 RBA240HV*2		HD6417751 RF240 (V)		HD6417751 RF200 (V)			
		*1		*1		*1		*1			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Address delay time	t_{AD}	1.5	5.3	1.5	5.3	1.5	6	1.5	6	ns	
$\overline{BS}$ delay time	t_{BSD}	1.5	5.3	1.5	5.3	1.5	6	1.5	6	ns	
$\overline{CS}$ delay time	t_{CSD}	1.5	5.3	1.5	5.3	1.5	6	1.5	6	ns	
$\overline{RW}$ delay time	t_{RWD}	1.5	5.3	1.5	5.3	1.5	6	1.5	6	ns	
$\overline{RD}$ delay time	t_{RSD}	1.5	5.3	1.5	5.3	1.5	6	1.5	6	ns	
Read data setup time	t_{RDS}	2.0	—	2.5	—	3.5	—	3.5	—	ns	
Read data hold time	t_{RDH}	1.5	—	1.5	—	1.5	—	1.5	—	ns	
$\overline{WE}$ delay time (falling edge)	t_{WEDF}	—	5.3	—	5.3	—	6	—	6	ns	Relative to CKIO falling edge
$\overline{WE}$ delay time	t_{WED1}	1.5	5.3	1.5	5.3	1.5	6	1.5	6	ns	
Write data delay time	t_{WDD}	1.5	5.3	1.5	5.3	1.5	6	1.5	6	ns	
$\overline{RDY}$ setup time	t_{RDYS}	2.0	—	2.5	—	3.5	—	3.5	—	ns	
$\overline{RDY}$ hold time	t_{RDYH}	1.5	—	1.5	—	1.5	—	1.5	—	ns	
$\overline{RAS}$ delay time	t_{RASD}	1.5	5.3	1.5	5.3	1.5	6	1.5	6	ns	
$\overline{CAS}$ delay time 1	t_{CASD1}	1.5	5.3	1.5	5.3	1.5	6	1.5	6	ns	DRAM
$\overline{CAS}$ delay time 2	t_{CASD2}	1.5	5.3	1.5	5.3	1.5	6	1.5	6	ns	SDRAM
CKE delay time	t_{CKED}	1.5	5.3	1.5	5.3	1.5	6	1.5	6	ns	SDRAM
DQM delay time	t_{DQMD}	1.5	5.3	1.5	5.3	1.5	6	1.5	6	ns	SDRAM
$\overline{FRAME}$ delay time	t_{FMD}	1.5	5.3	1.5	5.3	1.5	6	1.5	6	ns	MPX
$\overline{IOIS16}$ setup time	t_{IO16S}	2.0	—	2.5	—	3.5	—	3.5	—	ns	PCMCIA
$\overline{IOIS16}$ hold time	t_{IO16H}	1.5	—	1.5	—	1.5	—	1.5	—	ns	PCMCIA
$\overline{ICIOWR}$ delay time (falling edge)	t_{ICWSDF}	1.5	5.3	1.5	5.3	1.5	6	1.5	6	ns	PCMCIA
$\overline{ICIORD}$ delay time	t_{ICRSD}	1.5	5.3	1.5	5.3	1.5	6	1.5	6	ns	PCMCIA

Pin Name	I/O	Reset (Power On) Host	Reset (Power On) Non-Host	Reset (Manual) Host	Reset (Manual) Non-Host	Standby Host	Standby Non-Host	Reset (Software) Host	Reset (Software) Non-Host	Hard-ware Standby	Notes
$\overline{\text{PCIREQ3}}$/ MD10	I/O	I*[17]	I*[17]	Z*[10]	Z*[10] (IO*[11,16])	I*[10]	Z*[10] (IO*[10,16])	PI	PZ (IO*[10,16])	Z	Values in paren-thesis are when using PORT
PCIREQ1/ GNTIN	I	PI	PI	I*[10]	I*[10]	I*[10]	I*[10]	PI	PI	Z	
$\overline{\text{PCIGNT4}}$–$\overline{\text{PCIGNT2}}$	O	Z	Z	O	Z (K)	K	Z (K)	Z	Z (K)	Z	Values in paren-thesis are when using PORT
$\overline{\text{PCIGNT1}}$/ $\overline{\text{REQOUT}}$	O	Z	Z	O	O	K	K	Z	H	Z	
PCICLK	I	I	I	I	I	I	I	I	I	Z	
$\overline{\text{PCIRST}}$	O	L	L	K	K	K	K	L	L	Z	
IDSEL	I	PI	I	PI	I	PI	I	PI	I	Z	
$\overline{\text{INTA}}$	O	PZ	PZ	ODK *[10]	ODK *[10]	ODK *[10]	ODK *[10]	PZ	PZ	Z	

Appendix I Version Registers

The configuration of the registers related to the product version is shown below.

Table I.1 Register Configuration

Name	Abbreviation	Read/Write	Initial value	P4 Address	Area 7 Address	Access Size
Processor version register	PVR	R	*	H'FF000030	H'1F000030	32
Product register	PRR	R	*	H'FF000044	H'1F000044	32

Note: * Refer to table below.

PVR and PRR Initial Values

Product Name	PVR	PRR
SH7751	H'041100xx	H'xxxxxxxx
SH7751R	H'040500xx	H'0000011x

Legend: x: Undefined

1. Processor Version Register (PVR) Initial Value Example for SH7751R

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Version information															
Initial value:	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Version information								—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	—	—	—	—	—	—	—	—