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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.209", 5.30mm Width)
Supplier Device Package	8-SOIJ
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12c508a-04e-sm

TABLE 3-1: PIC12C5XX PINOUT DESCRIPTION

Name	DIP Pin #	SOIC Pin #	I/O/P Type	Buffer Type	Description
GP0	7	7	I/O	TTL/ST	Bi-directional I/O port/ serial programming data. Can be software programmed for internal weak pull-up and wake-up from SLEEP on pin change. This buffer is a Schmitt Trigger input when used in serial programming mode.
GP1	6	6	I/O	TTL/ST	Bi-directional I/O port/ serial programming clock. Can be software programmed for internal weak pull-up and wake-up from SLEEP on pin change. This buffer is a Schmitt Trigger input when used in serial programming mode.
GP2/T0CKI	5	5	I/O	ST	Bi-directional I/O port. Can be configured as T0CKI.
GP3/$\overline{MCLR}$/VPP	4	4	I	TTL/ST	Input port/master clear (reset) input/programming voltage input. When configured as $\overline{MCLR}$, this pin is an active low reset to the device. Voltage on $\overline{MCLR}$/VPP must not exceed VDD during normal device operation or the device will enter programming mode. Can be software programmed for internal weak pull-up and wake-up from SLEEP on pin change. Weak pull-up always on if configured as $\overline{MCLR}$. ST when in $\overline{MCLR}$ mode.
GP4/OSC2	3	3	I/O	TTL	Bi-directional I/O port/oscillator crystal output. Connections to crystal or resonator in crystal oscillator mode (XT and LP modes only, GPIO in other modes).
GP5/OSC1/CLKIN	2	2	I/O	TTL/ST	Bidirectional IO port/oscillator crystal input/external clock source input (GPIO in Internal RC mode only, OSC1 in all other oscillator modes). TTL input when GPIO, ST input in external RC oscillator mode.
VDD	1	1	P	—	Positive supply for logic and I/O pins
VSS	8	8	P	—	Ground reference for logic and I/O pins

Legend: I = input, O = output, I/O = input/output, P = power, — = not used, TTL = TTL input, ST = Schmitt Trigger input

4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1).

The special registers can be classified into two sets. The special function registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

TABLE 4-1: SPECIAL FUNCTION REGISTER (SFR) SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets[2]
N/A	TRIS	—	—							`--11 1111`	`--11 1111`
N/A	OPTION	Contains control bits to configure Timer0, Timer0/WDT prescaler, wake-up on change, and weak pull-ups								`1111 1111`	`1111 1111`
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								`xxxx xxxx`	`uuuu uuuu`
01h	TMR0	8-bit real-time clock/counter								`xxxx xxxx`	`uuuu uuuu`
02h[1]	PCL	Low order 8 bits of PC								`1111 1111`	`1111 1111`
03h	STATUS	GPWUF	—	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	`0001 1xxx`	`q00q quuu`[3]
04h	FSR (PIC12C508/ PIC12C508A/ PIC12C518)	Indirect data memory address pointer								`111x xxxx`	`111u uuuu`
04h	FSR (PIC12C509/ PIC12C509A/ PIC12CR509A/ PIC12CE519)	Indirect data memory address pointer								`110x xxxx`	`11uu uuuu`
05h	OSCCAL (PIC12C508/ PIC12C509)	CAL3	CAL2	CAL1	CAL0	—	—	—	—	`0111 ----`	`uuuu ----`
05h	OSCCAL (PIC12C508A/ PIC12C509A/ PIC12CE518/ PIC12CE519/ PIC12CR509A)	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	—	`1000 00--`	`uuuu uu--`
06h	GPIO (PIC12C508/ PIC12C509/ PIC12C508A/ PIC12C509A/ PIC12CR509A)	—	—	GP5	GP4	GP3	GP2	GP1	GP0	`--xx xxxx`	`--uu uuuu`
06h	GPIO (PIC12CE518/ PIC12CE519)	SCL	SDA	GP5	GP4	GP3	GP2	GP1	GP0	`11xx xxxx`	`11uu uuuu`

Legend: Shaded boxes = unimplemented or unused, – = unimplemented, read as '0' (if applicable)
x = unknown, u = unchanged, q = see the tables in Section 8.7 for possible values.

Note 1: The upper byte of the Program Counter is not directly accessible. See Section 4.6 for an explanation of how to access these bits.

2: Other (non power-up) resets include external reset through $\overline{MCLR}$, watchdog timer and wake-up on pin change reset.

3: If reset was due to wake-up on pin change then bit 7 = 1. All other resets will cause bit 7 = 0.

4.6 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

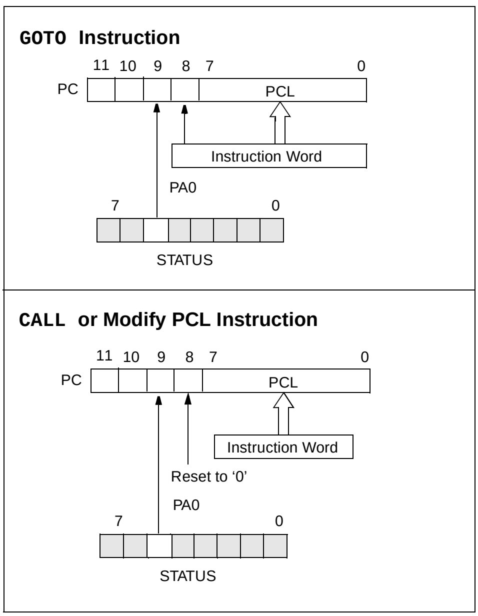
For a `GOTO` instruction, bits 8:0 of the PC are provided by the `GOTO` instruction word. The PC Latch (PCL) is mapped to PC<7:0>. Bit 5 of the STATUS register provides page information to bit 9 of the PC (Figure 4-8).

For a `CALL` instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-8).

Instructions where the PCL is the destination, or Modify PCL instructions, include `MOVWF PC`, `ADDWF PC`, and `BSF PC,5`.

> **Note:** Because PC<8> is cleared in the `CALL` instruction, or any Modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-8: LOADING OF PC BRANCH INSTRUCTIONS - PIC12C5XX



4.6.1 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page i.e., the oscillator calibration instruction. After executing MOVLW XX, the PC will roll over to location 00h, and begin executing user code.

The STATUS register page preselect bits are cleared upon a RESET, which means that page 0 is pre-selected.

Therefore, upon a RESET, a `GOTO` instruction will automatically cause the program to jump to page 0 until the value of the page bits is altered.

4.7 Stack

PIC12C5XX devices have a 12-bit wide L.I.F.O. hardware push/pop stack.

A `CALL` instruction will *push* the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential `CALL`'s are executed, only the most recent two return addresses are stored.

A `RETLW` instruction will *pop* the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential `RETLW`'s are executed, the stack will be filled with the address previously stored in level 2. Note that the W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

Upon any reset, the contents of the stack remain unchanged, however the program counter (PCL) will also be reset to 0.

> **Note 1:** There are no STATUS bits to indicate stack overflows or stack underflow conditions.
>
> **Note 2:** There are no instructions mnemonics called PUSH or POP. These are actions that occur from the execution of the `CALL` and `RETLW` instructions.

FIGURE 6-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE

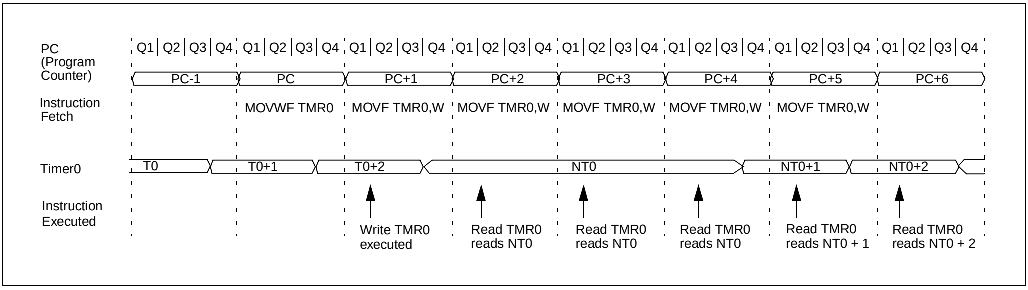


FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

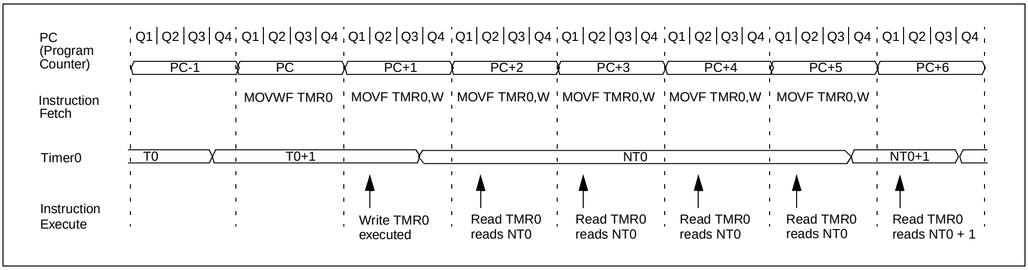


TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
01h	TMR0	Timer0 - 8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
N/A	OPTION	$\overline{\text{GPWU}}$	$\overline{\text{GPPU}}$	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
N/A	TRIS	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--11 1111	--11 1111

Legend: Shaded cells not used by Timer0, - = unimplemented, x = unknown, u = unchanged,

FIGURE 7-3: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

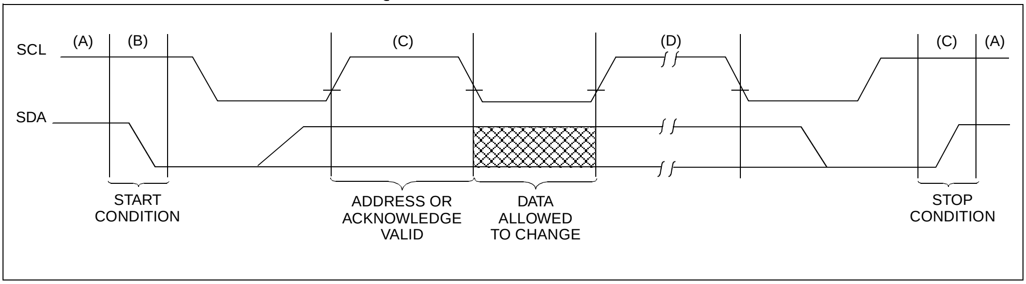
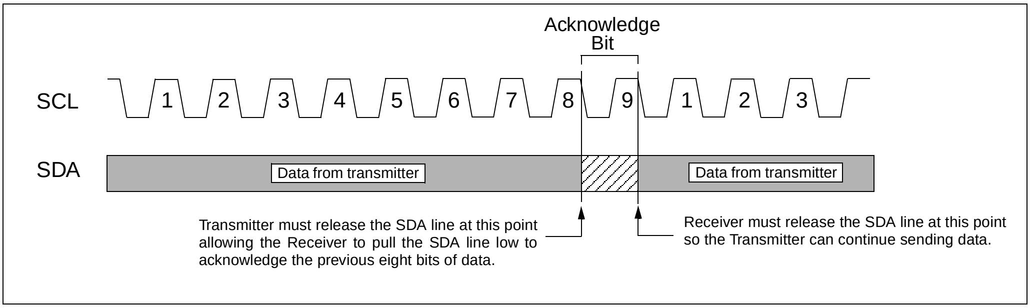


FIGURE 7-4: ACKNOWLEDGE TIMING

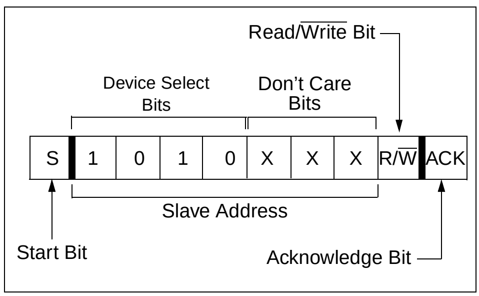


7.2 Device Addressing

After generating a START condition, the bus master transmits a control byte consisting of a slave address and a Read/$\overline{\text{Write}}$ bit that indicates what type of operation is to be performed. The slave address consists of a 4-bit device code (1010) followed by three don't care bits.

The last bit of the control byte determines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. (Figure 7-5). The bus is monitored for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 7-5: CONTROL BYTE FORMAT



7.5 READ OPERATIONS

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

7.5.1 CURRENT ADDRESS READ

It contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the device discontinues transmission (Figure 7-8).

7.5.2 RANDOM READ

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the device as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. It will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the device discontinues transmission (Figure 7-9). After this command, the internal address counter will point to the address location following the one that was just read.

7.5.3 SEQUENTIAL READ

Sequential reads are initiated in the same way as a random read except that after the device transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the device to transmit the next sequentially addressed 8-bit word (Figure 7-10).

To provide sequential reads, it contains an internal address pointer which is incremented by one at the completion of each read operation. This address pointer allows the entire memory contents to be serially read during one operation.

FIGURE 7-8: CURRENT ADDRESS READ

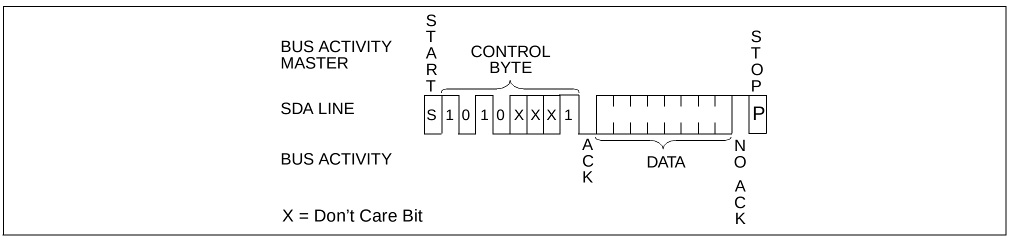


FIGURE 7-9: RANDOM READ

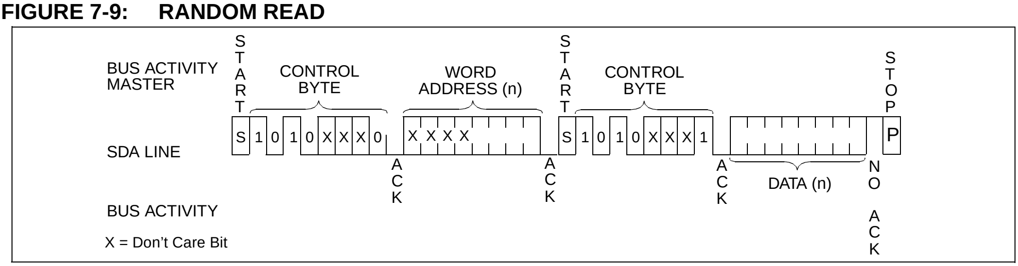
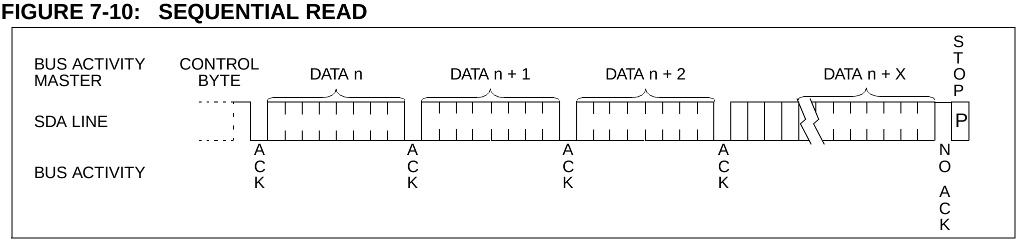


FIGURE 7-10: SEQUENTIAL READ



8.2 Oscillator Configurations

8.2.1 OSCILLATOR TYPES

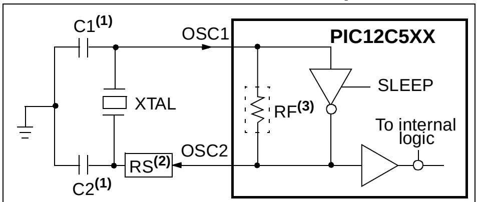
The PIC12C5XX can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

- LP: Low Power Crystal
- XT: Crystal/Resonator
- INTRC: Internal 4 MHz Oscillator
- EXTRC: External Resistor/Capacitor

8.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT or LP modes, a crystal or ceramic resonator is connected to the GP5/OSC1/CLKIN and GP4/OSC2 pins to establish oscillation (Figure 8-2). The PIC12C5XX oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT or LP modes, the device can have an external clock source drive the GP5/OSC1/CLKIN pin (Figure 8-3).

FIGURE 8-2: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (XT OR LP OSC CONFIGURATION)



Note 1: See Capacitor Selection tables for recommended values of C1 and C2.
2: A series resistor (RS) may be required for AT strip cut crystals.
3: RF approximate value = 10 MΩ.

FIGURE 8-3: EXTERNAL CLOCK INPUT OPERATION (XT OR LP OSC CONFIGURATION)

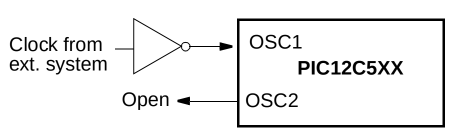


TABLE 8-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS - PIC12C5XX

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
XT	4.0 MHz	30 pF	30 pF

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 8-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - PIC12C5XX

Osc Type	Resonator Freq	Cap.Range C1	Cap. Range C2
LP	32 kHz(1)	15 pF	15 pF
XT	200 kHz 1 MHz 4 MHz	47-68 pF 15 pF 15 pF	47-68 pF 15 pF 15 pF

Note 1: For $V_{DD} > 4.5V$, $C1 = C2 \approx 30$ pF is recommended.

These values are for design guidance only. Rs may be required to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

TABLE 8-3: RESET CONDITIONS FOR REGISTERS

Register	Address	Power-on Reset	$\overline{MCLR}$ Reset WDT time-out Wake-up on Pin Change
W (PIC12C508/509)	—	qqqq xxxx (1)	qqqq uuuu (1)
W (PIC12C508A/509A/ PIC12CE518/519/ PIC12CE509A)	—	qqqq qqxx (1)	qqqq qquu (1)
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu
PC	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	q00q quuu (2,3)
FSR (PIC12C508/ PIC12C508A/ PIC12CE518)	04h	111x xxxx	111u uuuu
FSR (PIC12C509/ PIC12C509A/ PIC12CE519/ PIC12CR509A)	04h	110x xxxx	11uu uuuu
OSCCAL (PIC12C508/509)	05h	0111 ----	uuuu ----
OSCCAL (PIC12C508A/509A/ PIC12CE518/512/ PIC12CR509A)	05h	1000 00--	uuuu uu--
GPIO (PIC12C508/PIC12C509/ PIC12C508A/ PIC12C509A/ PIC12CR509A)	06h	--xx xxxx	--uu uuuu
GPIO (PIC12CE518/ PIC12CE519)	06h	11xx xxxx	11uu uuuu
OPTION	—	1111 1111	1111 1111
TRIS	—	--11 1111	--11 1111

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as ‘0’, q = value depends on condition.
Note 1: Bits <7:2> of W register contain oscillator calibration values due to MOVLW XX instruction at top of memory.
Note 2: See Table 8-7 for reset value for specific conditions
Note 3: If reset was due to wake-up on pin change, then bit 7 = 1. All other resets will cause bit 7 = 0.

TABLE 8-4: RESET CONDITION FOR SPECIAL REGISTERS

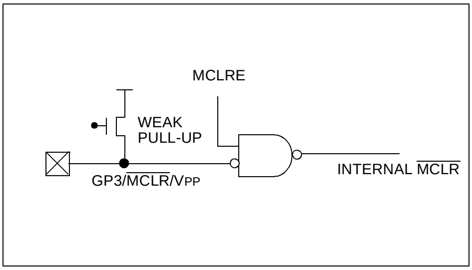
	STATUS Addr: 03h	PCL Addr: 02h
Power on reset	0001 1xxx	1111 1111
$\overline{MCLR}$ reset during normal operation	000u uuuu	1111 1111
$\overline{MCLR}$ reset during SLEEP	0001 0uuu	1111 1111
WDT reset during SLEEP	0000 0uuu	1111 1111
WDT reset normal operation	0000 uuuu	1111 1111
Wake-up from SLEEP on pin change	1001 0uuu	1111 1111

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as ‘0’.

8.3.1 $\overline{\text{MCLR}}$ ENABLE

This configuration bit when unprogrammed (left in the '1' state) enables the external $\overline{\text{MCLR}}$ function. When programmed, the $\overline{\text{MCLR}}$ function is tied to the internal V_{DD}, and the pin is assigned to be a GPIO. See Figure 8-7. When pin GP3/$\overline{\text{MCLR}}$/V_{PP} is configured as $\overline{\text{MCLR}}$, the internal pull-up is always on.

FIGURE 8-7: $\overline{\text{MCLR}}$ SELECT



8.4 Power-On Reset (POR)

The PIC12C5XX family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip reset for most power-up situations.

The on-chip POR circuit holds the chip in reset until V_{DD} has reached a high enough level for proper operation. To take advantage of the internal POR, program the GP3/$\overline{\text{MCLR}}$/V_{PP} pin as $\overline{\text{MCLR}}$ and tie through a resistor to V_{DD} or program the pin as GP3. An internal weak pull-up resistor is implemented using a transistor. Refer to Table 11-1 for the pull-up resistor ranges. This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for V_{DD} is specified. See Electrical Specifications for details.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, ...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating parameters are met.

A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 8-8.

The Power-On Reset circuit and the Device Reset Timer (Section 8.5) circuit are closely related. On power-up, the reset latch is set and the DRT is reset. The DRT timer begins counting once it detects $\overline{\text{MCLR}}$ to be high. After the time-out period, which is typically 18 ms, it will reset the reset latch and thus end the on-chip reset signal.

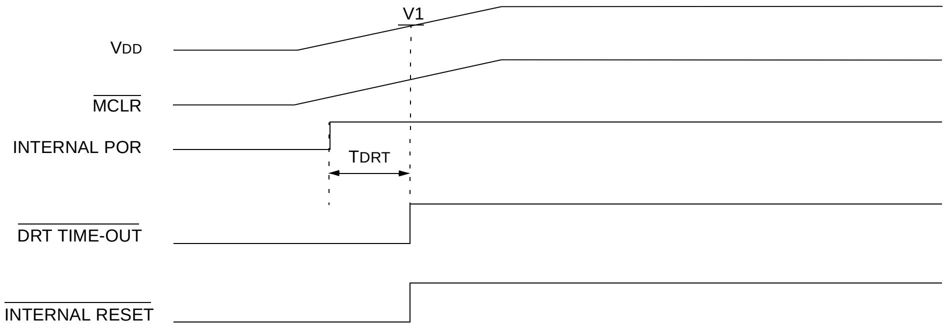
A power-up example where $\overline{\text{MCLR}}$ is held low is shown in Figure 8-9. V_{DD} is allowed to rise and stabilize before bringing $\overline{\text{MCLR}}$ high. The chip will actually come out of reset T_{DRT} msec after $\overline{\text{MCLR}}$ goes high.

In Figure 8-10, the on-chip Power-On Reset feature is being used ($\overline{\text{MCLR}}$ and V_{DD} are tied together or the pin is programmed to be GP3.). The V_{DD} is stable before the start-up timer times out and there is no problem in getting a proper reset. However, Figure 8-11 depicts a problem situation where V_{DD} rises too slowly. The time between when the DRT senses that $\overline{\text{MCLR}}$ is high and when $\overline{\text{MCLR}}$ (and V_{DD}) actually reach their full value, is too long. In this situation, when the start-up timer times out, V_{DD} has not reached the V_{DD} (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 8-10).

Note:	When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be meet to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For additional information refer to Application Notes "*Power-Up Considerations*" - AN522 and "*Power-up Trouble Shooting*" - AN607.

FIGURE 8-11: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO V_{DD}): SLOW V_{DD} RISE TIME



When V_{DD} rises slowly, the T_{DRT} time-out expires long before V_{DD} has reached its final value. In this example, the chip will reset properly if, and only if, $V1 \geq V_{DD}$ min.

8.5 Device Reset Timer (DRT)

In the PIC12C5XX, DRT runs from RESET and varies based on oscillator selection (see Table 8-5.)

The DRT operates on an internal RC oscillator. The processor is kept in RESET as long as the DRT is active. The DRT delay allows V_{DD} to rise above V_{DD} min., and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the device in a RESET condition for approximately 18 ms after $\overline{MCLR}$ has reached a logic high ($V_{IH}\overline{MCLR}$) level. Thus, programming GP3/$\overline{MCLR}$/V_{PP} as $\overline{MCLR}$ and using an external RC network connected to the $\overline{MCLR}$ input is not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications, as well as allowing the use of the GP3/$\overline{MCLR}$/V_{PP} pin as a general purpose input.

The Device Reset time delay will vary from chip to chip due to V_{DD}, temperature, and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out. This is particularly important for applications using the WDT to wake from SLEEP mode automatically.

8.6 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the external RC oscillator of the GP5/OSC1/CLKIN pin and the internal 4 MHz oscillator. That means that the WDT will run even if the main processor clock has been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT reset or wake-up reset generates a device RESET.

The $\overline{TO}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer reset.

The WDT can be permanently disabled by programming the configuration bit WDTE as a ’0’ (Section 8.1). Refer to the PIC12C5XX Programming Specifications to determine how to access the configuration word.

TABLE 8-5: DRT (DEVICE RESET TIMER PERIOD)

Oscillator Configuration	POR Reset	Subsequent Resets
IntRC & ExtRC	18 ms (typical)	300 µs (typical)
XT & LP	18 ms (typical)	18 ms (typical)

8.7 Time-Out Sequence, Power Down, and Wake-up from SLEEP Status Bits ($\overline{\text{TO}}$/$\overline{\text{PD}}$/GPWUF)

The $\overline{\text{TO}}$, $\overline{\text{PD}}$, and GPWUF bits in the STATUS register can be tested to determine if a RESET condition has been caused by a power-up condition, a $\overline{\text{MCLR}}$ or Watchdog Timer (WDT) reset.

TABLE 8-7: $\overline{\text{TO}}$/$\overline{\text{PD}}$/GPWUF STATUS AFTER RESET

GPWUF	$\overline{\text{TO}}$	$\overline{\text{PD}}$	RESET caused by
0	0	0	WDT wake-up from SLEEP
0	0	u	WDT time-out (not from SLEEP)
0	1	0	$\overline{\text{MCLR}}$ wake-up from SLEEP
0	1	1	Power-up
0	u	u	$\overline{\text{MCLR}}$ not during SLEEP
1	1	0	Wake-up from SLEEP on pin change

Legend: u = unchanged

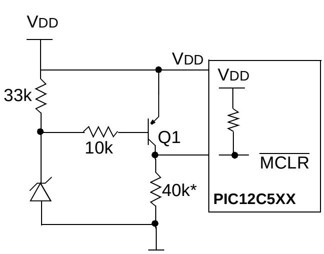
Note 1: The $\overline{\text{TO}}$, $\overline{\text{PD}}$, and GPWUF bits maintain their status (u) until a reset occurs. A low-pulse on the $\overline{\text{MCLR}}$ input does not change the $\overline{\text{TO}}$, $\overline{\text{PD}}$, and GPWUF status bits.

8.8 Reset on Brown-Out

A brown-out is a condition where device power (V_{DD}) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

To reset PIC12C5XX devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 8-13 , Figure 8-14 and Figure 8-15

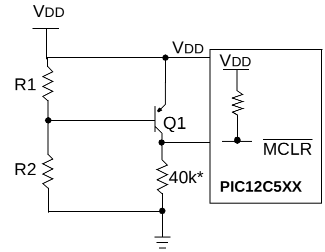
FIGURE 8-13: BROWN-OUT PROTECTION CIRCUIT 1



This circuit will activate reset when V_{DD} goes below Vz + 0.7V (where Vz = Zener voltage).

*Refer to Figure 8-7 and Table 11-1 for internal weak pull-up on $\overline{\text{MCLR}}$.

FIGURE 8-14: BROWN-OUT PROTECTION CIRCUIT 2

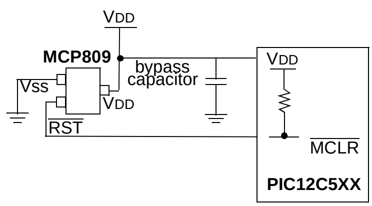


This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when V_{DD} is below a certain level such that:

$$V_{DD} \bullet \frac{R1}{R1 + R2} = 0.7V$$

*Refer to Figure 8-7 and Table 11-1 for internal weak pull-up on $\overline{\text{MCLR}}$.

FIGURE 8-15: BROWN-OUT PROTECTION CIRCUIT 3



This brown-out protection circuit employs Microchip Technology's MCP809 microcontroller supervisor. The MCP8XX and MCP1XX family of supervisors provide push-pull and open collector outputs with both high and low active reset pins. There are 7 different trip point selections to accomodate 5V and 3V systems.

TABLE 9-2: INSTRUCTION SET SUMMARY

Mnemonic, Operands		Description	Cycles	12-Bit Opcode MSb LSb	Status Affected	Notes
ADDWF	**f,d**	Add W and f	1	`0001 11df ffff`	C,DC,Z	1,2,4
ANDWF	**f,d**	AND W with f	1	`0001 01df ffff`	Z	2,4
CLRF	**f**	Clear f	1	`0000 011f ffff`	Z	4
CLRW	**–**	Clear W	1	`0000 0100 0000`	Z	
COMF	**f, d**	Complement f	1	`0010 01df ffff`	Z	
DECF	**f, d**	Decrement f	1	`0000 11df ffff`	Z	2,4
DECFSZ	**f, d**	Decrement f, Skip if 0	1(2)	`0010 11df ffff`	None	2,4
INCF	**f, d**	Increment f	1	`0010 10df ffff`	Z	2,4
INCFSZ	**f, d**	Increment f, Skip if 0	1(2)	`0011 11df ffff`	None	2,4
IORWF	**f, d**	Inclusive OR W with f	1	`0001 00df ffff`	Z	2,4
MOVF	**f, d**	Move f	1	`0010 00df ffff`	Z	2,4
MOVWF	**f**	Move W to f	1	`0000 001f ffff`	None	1,4
NOP	**–**	No Operation	1	`0000 0000 0000`	None	
RLF	**f, d**	Rotate left f through Carry	1	`0011 01df ffff`	C	2,4
RRF	**f, d**	Rotate right f through Carry	1	`0011 00df ffff`	C	2,4
SUBWF	**f, d**	Subtract W from f	1	`0000 10df ffff`	C,DC,Z	1,2,4
SWAPF	**f, d**	Swap f	1	`0011 10df ffff`	None	2,4
XORWF	**f, d**	Exclusive OR W with f	1	`0001 10df ffff`	Z	2,4
BIT-ORIENTED FILE REGISTER OPERATIONS						
BCF	**f, b**	Bit Clear f	1	`0100 bbbf ffff`	None	2,4
BSF	**f, b**	Bit Set f	1	`0101 bbbf ffff`	None	2,4
BTFSC	**f, b**	Bit Test f, Skip if Clear	1 (2)	`0110 bbbf ffff`	None	
BTFSS	**f, b**	Bit Test f, Skip if Set	1 (2)	`0111 bbbf ffff`	None	
LITERAL AND CONTROL OPERATIONS						
ANDLW	**k**	AND literal with W	1	`1110 kkkk kkkk`	Z	
CALL	**k**	Call subroutine	2	`1001 kkkk kkkk`	None	1
CLRWDT	**k**	Clear Watchdog Timer	1	`0000 0000 0100`	$\overline{TO}$, $\overline{PD}$	
GOTO	**k**	Unconditional branch	2	`101k kkkk kkkk`	None	
IORLW	**k**	Inclusive OR Literal with W	1	`1101 kkkk kkkk`	Z	
MOVLW	**k**	Move Literal to W	1	`1100 kkkk kkkk`	None	
OPTION	**–**	Load OPTION register	1	`0000 0000 0010`	None	
RETLW	**k**	Return, place Literal in W	2	`1000 kkkk kkkk`	None	
SLEEP	**–**	Go into standby mode	1	`0000 0000 0011`	$\overline{TO}$, $\overline{PD}$	
TRIS	**f**	Load TRIS register	1	`0000 0000 0fff`	None	3
XORLW	**k**	Exclusive OR Literal to W	1	`1111 kkkk kkkk`	Z	

Note 1: The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for `GOTO`. (Section 4.6)

2: When an I/O register is modified as a function of itself (e.g. `MOVF GPIO, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

3: The instruction `TRIS f`, where f = 6 causes the contents of the W register to be written to the tristate latches of GPIO. A '1' forces the pin to a hi-impedance state and disables the output buffers.

4: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared (if assigned to TMR0).

ADDWF — Add W and f

Syntax:	[*label*] ADDWF f,d
Operands:	$0 \leq f \leq 31$ $d \in [0,1]$
Operation:	(W) + (f) → (dest)
Status Affected:	C, DC, Z
Encoding:	`0001` `11df` `ffff`
Description:	Add the contents of the W register and register 'f'. If 'd' is 0 the result is stored in the W register. If '1' the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example:	`ADDWF FSR, 0`

Before Instruction
W = 0x17
FSR = 0xC2

After Instruction
W = 0xD9
FSR = 0xC2

ANDLW — And literal with W

Syntax:	[*label*] ANDLW k
Operands:	$0 \leq k \leq 255$
Operation:	(W).AND. (k) → (W)
Status Affected:	Z
Encoding:	`1110` `kkkk` `kkkk`
Description:	The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.
Words:	1
Cycles:	1
Example:	`ANDLW 0x5F`

Before Instruction
W = 0xA3

After Instruction
W = 0x03

ANDWF — AND W with f

Syntax:	[*label*] ANDWF f,d
Operands:	$0 \leq f \leq 31$ $d \in [0,1]$
Operation:	(W) .AND. (f) → (dest)
Status Affected:	Z
Encoding:	`0001` `01df` `ffff`
Description:	The contents of the W register are AND'ed with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example:	`ANDWF FSR, 1`

Before Instruction
W = 0x17
FSR = 0xC2

After Instruction
W = 0x17
FSR = 0x02

BCF — Bit Clear f

Syntax:	[*label*] BCF f,b
Operands:	$0 \leq f \leq 31$ $0 \leq b \leq 7$
Operation:	0 → (f<b>)
Status Affected:	None
Encoding:	`0100` `bbbf` `ffff`
Description:	Bit 'b' in register 'f' is cleared.
Words:	1
Cycles:	1
Example:	`BCF FLAG_REG, 7`

Before Instruction
FLAG_REG = 0xC7

After Instruction
FLAG_REG = 0x47

10.10 MPLAB Integrated Development Environment Software

The MPLAB IDE Software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a windows based application which contains:

- A full featured editor
- Three operating modes
  - editor
  - emulator
  - simulator
- A project manager
- Customizable tool bar and key mapping
- A status bar with project information
- Extensive on-line help

MPLAB allows you to:

- Edit your source files (either assembly or ‘C’)
- One touch assemble (or compile) and download to PICmicro® tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file

The ability to use MPLAB with Microchip’s simulator allows a consistent platform and the ability to easily switch from the low cost simulator to the full featured emulator with minimal retraining due to development tools.

10.11 Assembler (MPASM)

The MPASM Universal Macro Assembler is a PC-hosted symbolic assembler. It supports all microcontroller series including the PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX, and PIC17CXX families.

MPASM offers full featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from MPLAB-ICE, Microchip’s Universal Emulator System.

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro assembly capability.
- Produces all the files (Object, Listing, Symbol, and special) required for symbolic debug with Microchip’s emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a rich directive language to support programming of the PICmicro®. Directives are helpful in making the development of your assemble source code shorter and more maintainable.

10.12 Software Simulator (MPLAB-SIM)

The MPLAB-SIM Software Simulator allows code development in a PC host environment. It allows the user to simulate the PICmicro® series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in; single step, execute until break, or in a trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C17 and MPASM. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

10.13 MPLAB-C17 Compiler

The MPLAB-C17 Code Development System is a complete ANSI ‘C’ compiler and integrated development environment for Microchip’s PIC17CXXX family of microcontrollers. The compiler provides powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compiler provides symbol information that is compatible with the MPLAB IDE memory display.

10.14 Fuzzy Logic Development System (*fuzzy*TECH-MP)

*fuzzy*TECH-MP fuzzy logic development tool is available in two versions - a low cost introductory version, MP Explorer, for designers to gain a comprehensive working knowledge of fuzzy logic system design; and a full-featured version, *fuzzy*TECH-MP, Edition for implementing more complex systems.

Both versions include Microchip’s *fuzzy*LAB™ demonstration board for hands-on experience with fuzzy logic systems implementation.

10.15 SEEVAL® Evaluation and Programming System

The SEEVAL SEEPROM Designer’s Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials™ and secure serials. The Total Endurance™ Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

12.0 DC AND AC CHARACTERISTICS - PIC12C508/PIC12C509

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean – 3σ) respectively, where σ is standard deviation.

FIGURE 12-1: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE (VDD = 2.5V)

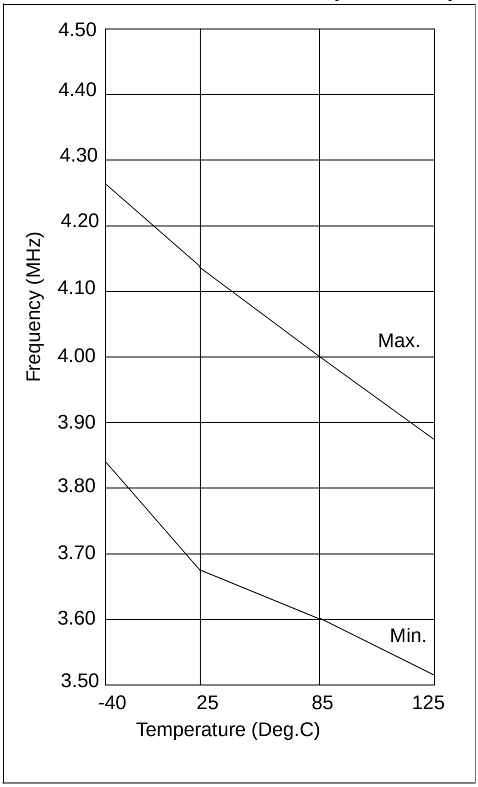


FIGURE 12-2: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE (VDD = 5.0V)

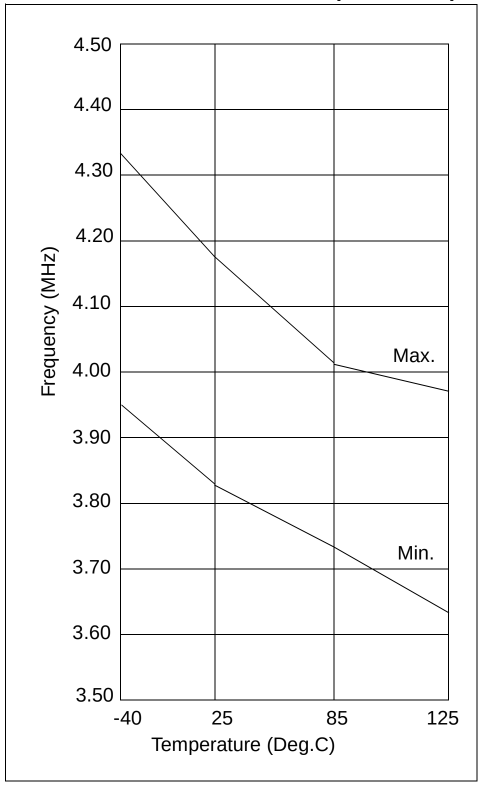


TABLE 13-8: EEPROM MEMORY BUS TIMING REQUIREMENTS - PIC12CE5XX ONLY.

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C, Vcc = 3.0V to 5.5V (commercial) –40°C ≤ TA ≤ +85°C, Vcc = 3.0V to 5.5V (industrial) –40°C ≤ TA ≤ +125°C, Vcc = 4.5V to 5.5V (extended) Operating Voltage VDD range is described in Section 13.1				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Clock frequency	FCLK	— — —	100 100 400	kHz	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 3.0V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Clock high time	THIGH	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 3.0V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Clock low time	TLOW	4700 4700 1300	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 3.0V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
SDA and SCL rise time (Note 1)	TR	— — —	1000 1000 300	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 3.0V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
SDA and SCL fall time	TF	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 3.0V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
START condition setup time	TSU:STA	4700 4700 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 3.0V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Data input hold time	THD:DAT	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250 250 100	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 3.0V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
STOP condition setup time	TSU:STO	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 3.0V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Output valid from clock (Note 2)	TAA	— — —	3500 3500 900	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 3.0V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Bus free time: Time the bus must be free before a new transmission can start	TBUF	4700 4700 1300	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 3.0V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Output fall time from VIH minimum to VIL maximum	TOF	20+0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	ns	(Notes 1, 3)
Write cycle time	TWC	—	4	ms	
Endurance		1M	—	cycles	25°C, VCC = 5.0V, Block Mode (Note 4)

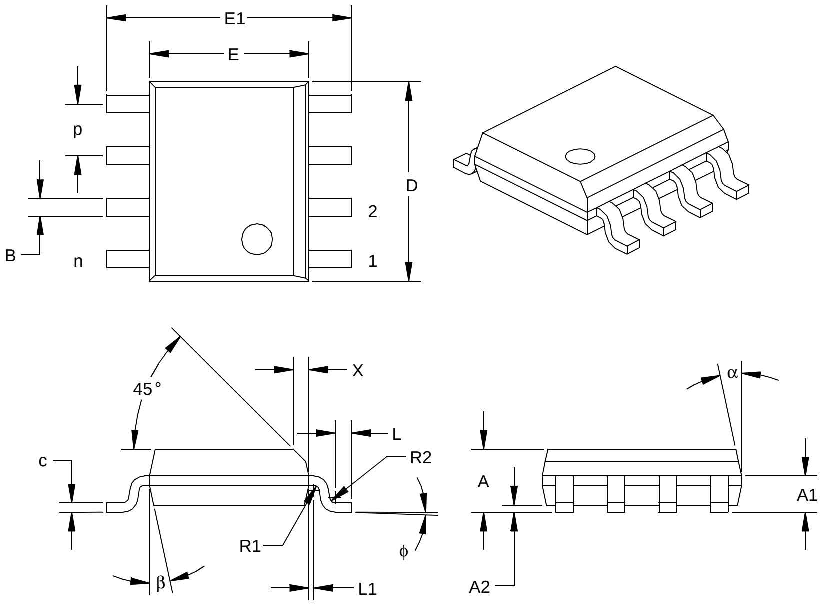
Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on Microchip's website.

Package Type: K04-057 8-Lead Plastic Small Outline (SN) – Narrow, 150 mil



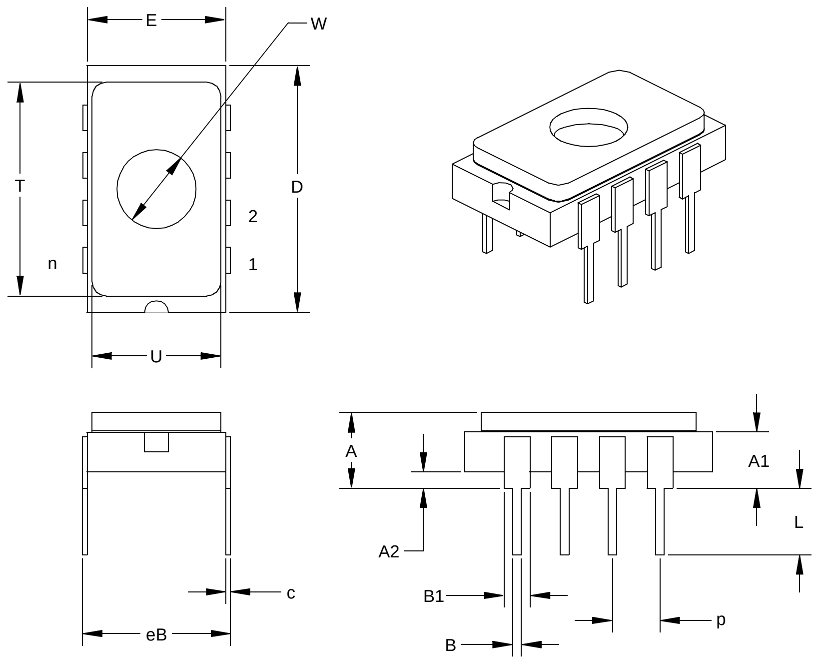
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.050			1.27	
Number of Pins	n		8			8	
Overall Pack. Height	A	0.054	0.061	0.069	1.37	1.56	1.75
Shoulder Height	A1	0.027	0.035	0.044	0.69	0.90	1.11
Standoff	A2	0.004	0.007	0.010	0.10	0.18	0.25
Molded Package Length	D‡	0.189	0.193	0.196	4.80	4.89	4.98
Molded Package Width	E‡	0.150	0.154	0.157	3.81	3.90	3.99
Outside Dimension	E1	0.229	0.237	0.244	5.82	6.01	6.20
Chamfer Distance	X	0.010	0.015	0.020	0.25	0.38	0.51
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	φ	0	4	8	0	4	8
Radius Centerline	L1	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.009	0.010	0.19	0.22	0.25
Lower Lead Width	B†	0.014	0.017	0.020	0.36	0.43	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter.

† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

Package Type: K04-084 8-Lead Ceramic Side Brazed Dual In-line with Window (JW) – 300 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		8			8	
Pitch	p	0.098	0.100	0.102	2.49	2.54	2.59
Lower Lead Width	B	0.016	0.018	0.020	0.41	0.46	0.51
Upper Lead Width	B1	0.050	0.055	0.060	1.27	1.40	1.52
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.145	0.165	0.185	3.68	4.19	4.70
Top of Body to Seating Plane	A1	0.103	0.123	0.143	2.62	3.12	3.63
Base to Seating Plane	A2	0.025	0.035	0.045	0.64	0.89	1.14
Tip to Seating Plane	L	0.130	0.140	0.150	3.30	3.56	3.81
Package Length	D	0.510	0.520	0.530	12.95	13.21	13.46
Package Width	E	0.280	0.290	0.300	7.11	7.37	7.62
Overall Row Spacing	eB	0.310	0.338	0.365	7.87	8.57	9.27
Window Diameter	W	0.161	0.166	0.171	4.09	4.22	4.34
Lid Length	T	0.440	0.450	0.460	11.18	11.43	11.68
Lid Width	U	0.260	0.270	0.280	6.60	6.86	7.11

* Controlling Parameter.

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Device: **PIC12C5XX** Literature Number: **DS40139E**

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this data sheet easy to follow? If not, why?

4. What additions to the data sheet do you think would enhance the structure and subject?

5. What deletions from the data sheet could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

8. How would you improve our software, systems, and silicon products?

PIC12C5XX Product Identification System

PART NO. -XX X /XX XXX

Pattern:	Special Requirements		
Package:	SN	=	150 mil SOIC
	SM	=	208 mil SOIC
	P	=	300 mil PDIP
	JW	=	300 mil Windowed Ceramic Side Brazed
Temperature Range:	-	=	0°C to +70°C
	I	=	-40°C to +85°C
	E	=	-40°C to +125°C
Frequency Range:	04	=	4 MHz
Device	PIC12C508		
	PIC12C509		
	PIC12C508T (Tape & reel for SOIC only)		
	PIC12C509T (Tape & reel for SOIC only)		
	PIC12C508A		
	PIC12C509A		
	PIC12C508AT (Tape & reel for SOIC only)		
	PIC12C509AT (Tape & reel for SOIC only)		
	PIC12LC508A		
	PIC12LC509A		
	PIC12LC508AT (Tape & reel for SOIC only)		
	PIC12LC509AT (Tape & reel for SOIC only)		
	PIC12CR509A		
	PIC12CR509AT (Tape & reel for SOIC only)		
	PIC12LCR509A		
	PIC12LCR509AT (Tape & reel for SOIC only)		
	PIC12CE518		
	PIC12CE518T (Tape & reel for SOIC only)		
	PIC12CE519		
	PIC12CE519T (Tape & reel for SOIC only)		
	PIC12LCE518		
	PIC12LCE518T (Tape & reel for SOIC only)		
	PIC12LCE519		
	PIC12LCE519T (Tape & reel for SOIC only)		

Examples

a) PIC12C508A-04/P Commercial Temp., PDIP Package, 4 MHz, normal V_{DD} limits

b) PIC12C508A-04I/SM Industrial Temp., SOIC package, 4 MHz, normal V_{DD} limits

c) PIC12C509-04I/P Industrial Temp., PDIP package, 4 MHz, normal V_{DD} limits

Please contact your local sales office for exact ordering procedures.

Sales and Support:

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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