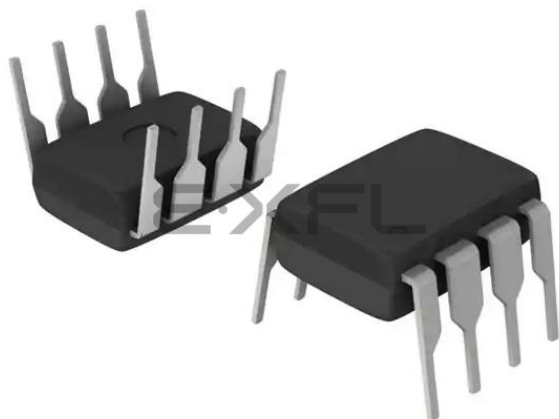




Welcome to E-XFL.COM

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12c508a-04i-p

PIC12C5XX

FIGURE 3-1: PIC12C5XX BLOCK DIAGRAM

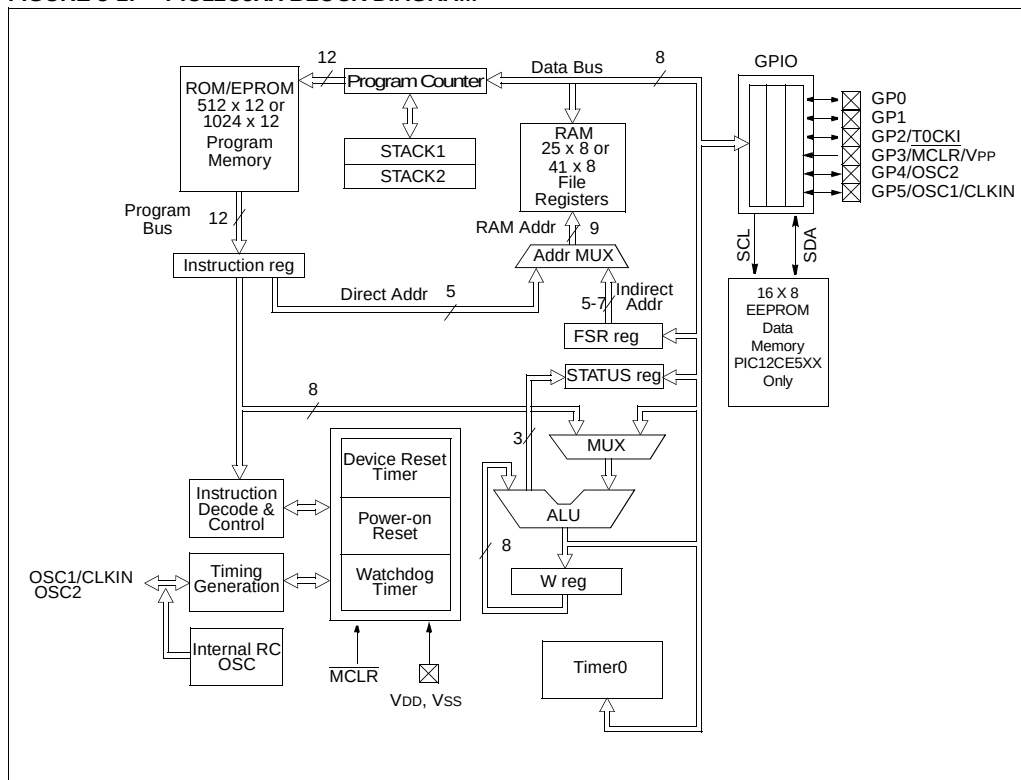


FIGURE 6-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE

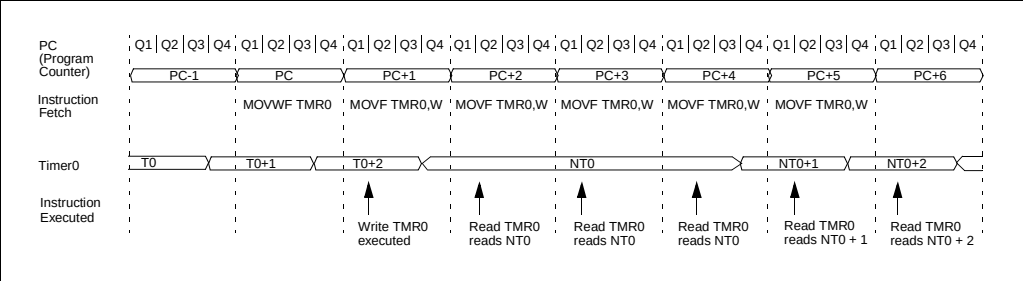


FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

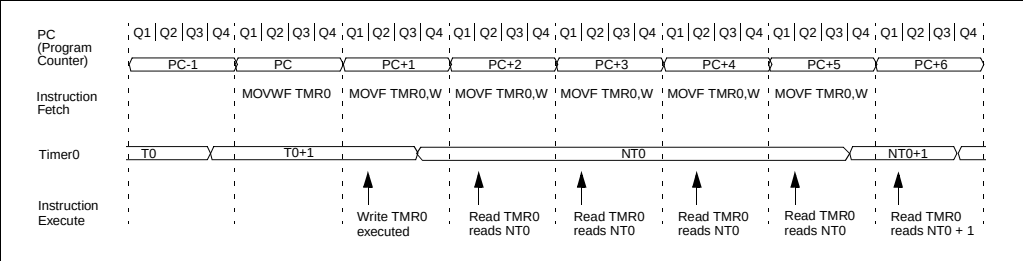


TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
01h	TMR0	Timer0 - 8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
N/A	OPTION	GPWU	GPPU	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
N/A	TRIS	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--11 1111	--11 1111

Legend: Shaded cells not used by Timer0, - = unimplemented, x = unknown, u = unchanged,

7.0.2 SERIAL CLOCK

This SCL input is used to synchronize the data transfer from and to the device.

7.1 BUS CHARACTERISTICS

The following **bus protocol** is to be used with the EEPROM data memory.

- Data transfer may be initiated only when the bus is not busy.

During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 7-3).

7.1.1 BUS NOT BUSY (A)

Both data and clock lines remain HIGH.

7.1.2 START DATA TRANSFER (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

7.1.3 STOP DATA TRANSFER (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

7.1.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

7.1.5 ACKNOWLEDGE

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: Acknowledge bits are not generated if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition (Figure 7-4).

7.5 READ OPERATIONS

Read operations are initiated in the same way as write operations with the exception that the R/W bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

7.5.1 CURRENT ADDRESS READ

It contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n , the next current address read operation would access data from address $n + 1$. Upon receipt of the slave address with the $R/\bar{W}$ bit set to one, the device issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the device discontinues transmission (Figure 7-8).

7.5.2 RANDOM READ

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the

device as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the $R/\bar{W}$ bit set to a one. It will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the device discontinues transmission (Figure 7-9). After this command, the internal address counter will point to the address location following the one that was just read.

7.5.3 SEQUENTIAL READ

Sequential reads are initiated in the same way as a random read except that after the device transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the device to transmit the next sequentially addressed 8-bit word (Figure 7-10).

To provide sequential reads, it contains an internal address pointer which is incremented by one at the completion of each read operation. This address pointer allows the entire memory contents to be serially read during one operation.

FIGURE 7-8: CURRENT ADDRESS READ

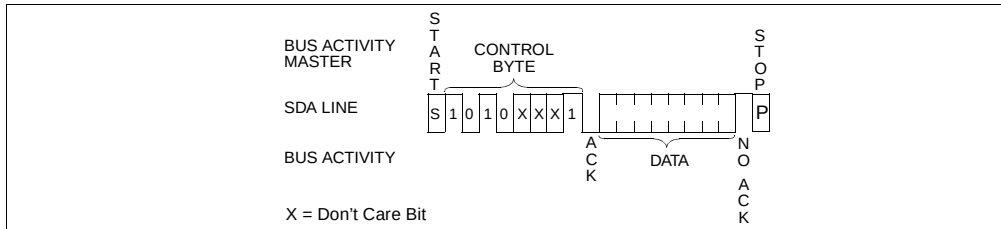


FIGURE 7-9: RANDOM READ

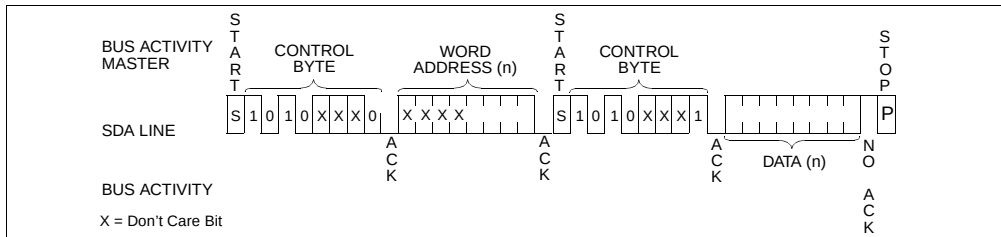


FIGURE 7-10: SEQUENTIAL READ

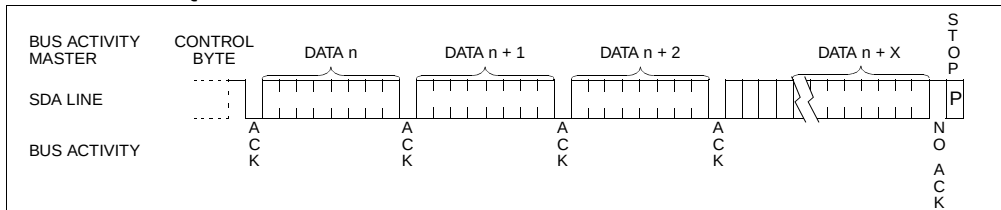
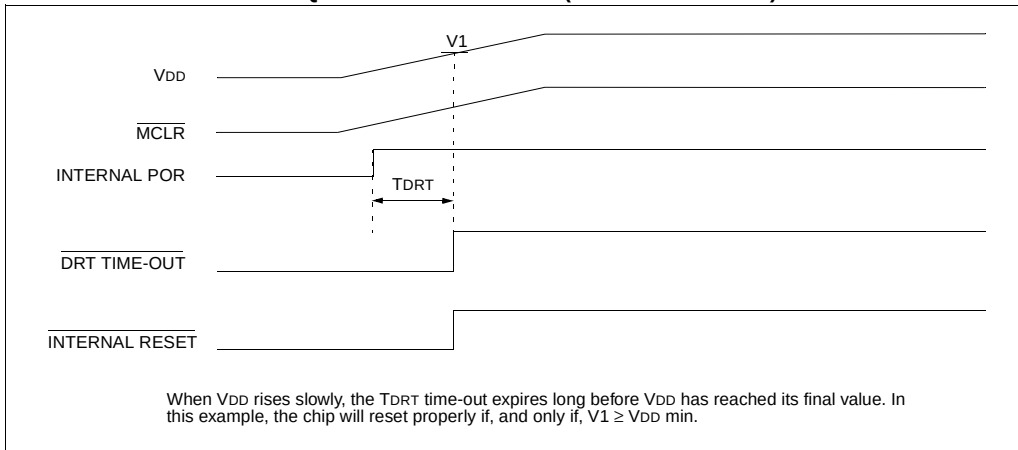


FIGURE 8-11: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD}): SLOW V_{DD} RISE TIME



8.5 Device Reset Timer (DRT)

In the PIC12C5XX, DRT runs from RESET and varies based on oscillator selection (see Table 8-5.)

The DRT operates on an internal RC oscillator. The processor is kept in RESET as long as the DRT is active. The DRT delay allows V_{DD} to rise above $V_{DD \text{ min.}}$, and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the device in a RESET condition for approximately 18 ms after $\overline{\text{MCLR}}$ has reached a logic high ($V_{IH\overline{\text{MCLR}}}$) level. Thus, programming GP3/ $\overline{\text{MCLR}}$ / V_{PP} as $\overline{\text{MCLR}}$ and using an external RC network connected to the $\overline{\text{MCLR}}$ input is not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications, as well as allowing the use of the GP3/ $\overline{\text{MCLR}}$ / V_{PP} pin as a general purpose input.

The Device Reset time delay will vary from chip to chip due to V_{DD} , temperature, and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out. This is particularly important for applications using the WDT to wake from SLEEP mode automatically.

8.6 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the external RC oscillator of the GP5/OSC1/CLKIN pin and the internal 4 MHz oscillator. That means that the WDT will run even if the main processor clock has been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT reset or wake-up reset generates a device RESET.

The $\overline{\text{TO}}$ bit ($\text{STATUS}<4>$) will be cleared upon a Watchdog Timer reset.

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Section 8.1). Refer to the PIC12C5XX Programming Specifications to determine how to access the configuration word.

TABLE 8-5: DRT (DEVICE RESET TIMER PERIOD)

Oscillator Configuration	POR Reset	Subsequent Resets
IntRC & ExtRC	18 ms (typical)	300 μ s (typical)
XT & LP	18 ms (typical)	18 ms (typical)

PIC12C5XX

8.7 Time-Out Sequence, Power Down, and Wake-up from SLEEP Status Bits (TO/PD/GPWUF)

The $\overline{TO}$, $\overline{PD}$, and GPWUF bits in the STATUS register can be tested to determine if a RESET condition has been caused by a power-up condition, a $\overline{MCLR}$ or Watchdog Timer (WDT) reset.

TABLE 8-7: $\overline{TO}/\overline{PD}/\overline{GPWUF}$ STATUS AFTER RESET

GPWUF	$\overline{TO}$	$\overline{PD}$	RESET caused by
0	0	0	WDT wake-up from SLEEP
0	0	u	WDT time-out (not from SLEEP)
0	1	0	$\overline{MCLR}$ wake-up from SLEEP
0	1	1	Power-up
0	u	u	$\overline{MCLR}$ not during SLEEP
1	1	0	Wake-up from SLEEP on pin change

Legend: u = unchanged

Note 1: The $\overline{TO}$, $\overline{PD}$, and GPWUF bits maintain their status (u) until a reset occurs. A low-pulse on the $\overline{MCLR}$ input does not change the $\overline{TO}$, $\overline{PD}$, and GPWUF status bits.

8.8 Reset on Brown-Out

A brown-out is a condition where device power (V_{DD}) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

To reset PIC12C5XX devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 8-13, Figure 8-14 and Figure 8-15

FIGURE 8-13: BROWN-OUT PROTECTION CIRCUIT 1

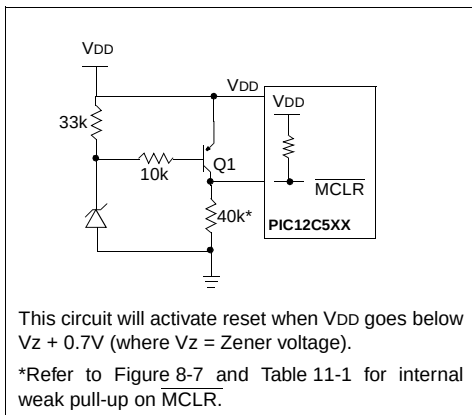


FIGURE 8-14: BROWN-OUT PROTECTION CIRCUIT 2

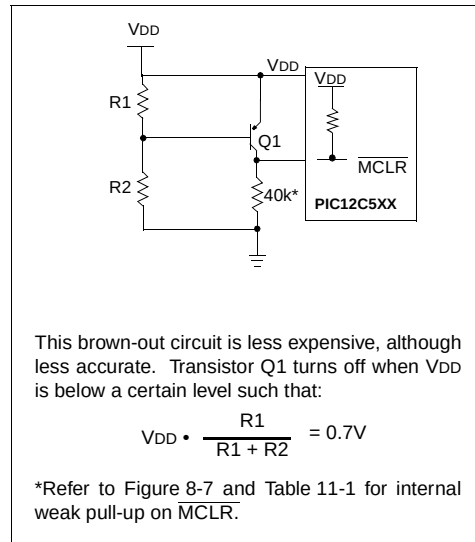
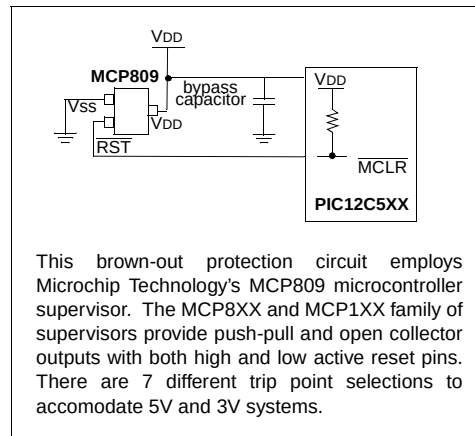


FIGURE 8-15: BROWN-OUT PROTECTION CIRCUIT 3



9.0 INSTRUCTION SET SUMMARY

Each PIC12C5XX instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type, and one or more operands which further specify the operation of the instruction. The PIC12C5XX instruction set summary in Table 9-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 9-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 9-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0 (store result in W) d = 1 (store result in file register 'f') Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
WDT	Watchdog Timer Counter
T $\bar{O}$	Time-Out bit
P $\bar{D}$	Power-Down bit
dest	Destination, either the W register or the specified register file location
[]	Options
()	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
<i>italics</i>	User defined term (font is courier)

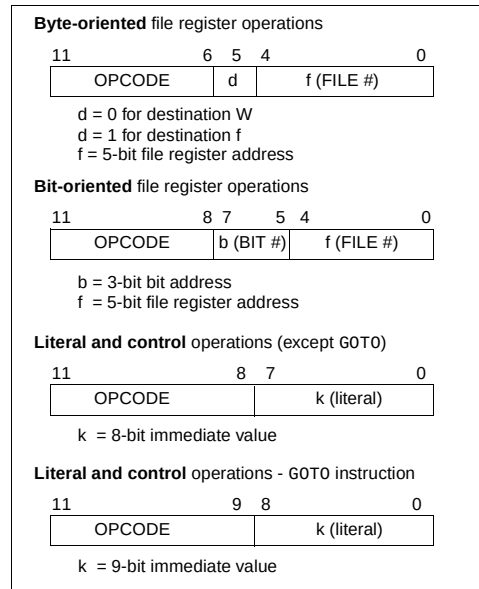
All instructions are executed within a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μ s. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μ s.

Figure 9-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

FIGURE 9-1: GENERAL FORMAT FOR INSTRUCTIONS



10.6 SIMICE Entry-Level Hardware Simulator

SIMICE is an entry-level hardware development system designed to operate in a PC-based environment with Microchip's simulator MPLAB™-SIM. Both SIMICE and MPLAB-SIM run under Microchip Technology's MPLAB Integrated Development Environment (IDE) software. Specifically, SIMICE provides hardware simulation for Microchip's PIC12C5XX, PIC12CE5XX, and PIC16C5X families of PICmicro® 8-bit microcontrollers. SIMICE works in conjunction with MPLAB-SIM to provide non-real-time I/O port emulation. SIMICE enables a developer to run simulator code for driving the target system. In addition, the target system can provide input to the simulator code. This capability allows for simple and interactive debugging without having to manually generate MPLAB-SIM stimulus files. SIMICE is a valuable debugging tool for entry-level system development.

10.7 PICDEM-1 Low-Cost PICmicro® Demonstration Board

The PICDEM-1 is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The users can program the sample microcontrollers provided with the PICDEM-1 board, on a PRO MATE II or PICSTART-Plus programmer, and easily test firmware. The user can also connect the PICDEM-1 board to the MPLAB-ICE emulator and download the firmware to the emulator for testing. Additional prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push-button switches and eight LEDs connected to PORTB.

10.8 PICDEM-2 Low-Cost PIC16CXX Demonstration Board

The PICDEM-2 is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-2 board, on a PRO MATE II programmer or PICSTART-Plus, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-2 board to test firmware. Additional prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push-button switches, a potentiometer for simulated analog input, a Serial EEPROM to demonstrate usage of the I²C bus and separate headers for connection to an LCD module and a keypad.

10.9 PICDEM-3 Low-Cost PIC16CXXX Demonstration Board

The PICDEM-3 is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with a LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-3 board, on a PRO MATE II programmer or PICSTART Plus with an adapter socket, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-3 board to test firmware. Additional prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include an RS-232 interface, push-button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM-3 board is an LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM-3 provides an additional RS-232 interface and Windows 3.1 software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

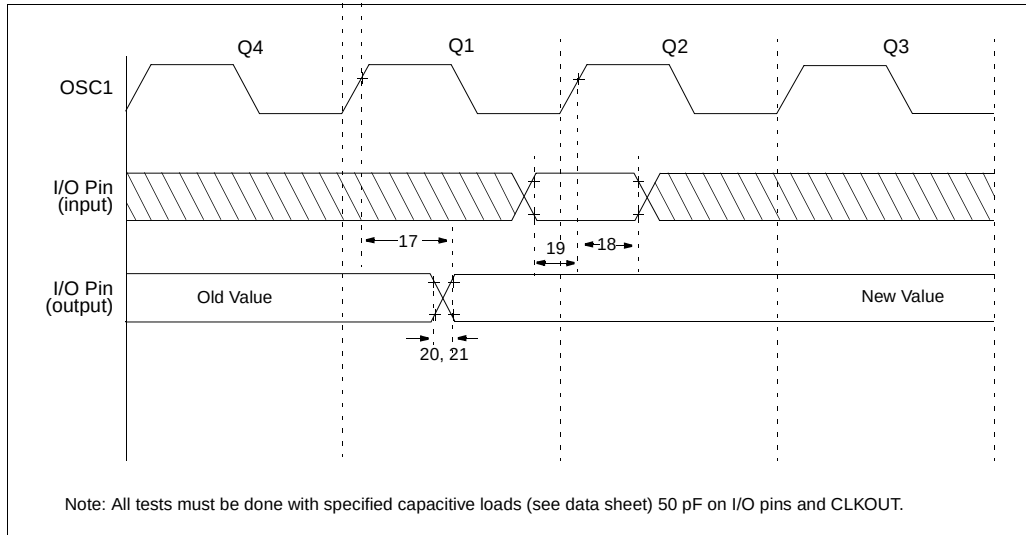
TABLE 11-3: CALIBRATED INTERNAL RC FREQUENCIES - PIC12C508/C509

AC Characteristics		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial), $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial), $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)					
		Operating Voltage V_{DD} range is described in Section 10.1					
Parameter No.	Sym	Characteristic	Min*	Typ ⁽¹⁾	Max*	Units	Conditions
		Internal Calibrated RC Frequency	3.58	4.00	4.32	MHz	$V_{DD} = 5.0\text{V}$
		Internal Calibrated RC Frequency	3.50	—	4.26	MHz	$V_{DD} = 2.5\text{V}$

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 11-3: I/O TIMING - PIC12C508/C509



13.1 DC CHARACTERISTICS: PIC12C508A/509A (Commercial, Industrial, Extended) PIC12CE518/519 (Commercial, Industrial, Extended) PIC12CR509A (Commercial, Industrial, Extended)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) −40°C ≤ TA ≤ +85°C (industrial) −40°C ≤ TA ≤ +125°C (extended)					
Parm No.	Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
D001	Supply Voltage	VDD	3.0		5.5	V	FOSC = DC to 4 MHz (Commercial/Industrial, Extended)
D002	RAM Data Retention Voltage ⁽²⁾	VDR		1.5*		V	Device in SLEEP mode
D003	VDD Start Voltage to ensure Power-on Reset	VPOR		VSS		V	See section on Power-on Reset for details
D004	VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See section on Power-on Reset for details
D010	Supply Current ⁽³⁾	IDD	—	0.8	1.4	mA	XT and EXTRC options (Note 4) FOSC = 4 MHz, VDD = 5.5V
D010C			—	0.8	1.4	mA	INTRC Option FOSC = 4 MHz, VDD = 5.5V
D010A			—	19	27	μA	LP OPTION, Commercial Temperature FOSC = 32 kHz, VDD = 3.0V, WDT disabled
			—	19	35	μA	LP OPTION, Industrial Temperature FOSC = 32 kHz, VDD = 3.0V, WDT disabled
			—	30	55	μA	LP OPTION, Extended Temperature FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D020 D021 D021B	Power-Down Current ⁽⁵⁾	IPD	—	0.25	4	μA	VDD = 3.0V, Commercial WDT disabled
—			0.25	5	μA	VDD = 3.0V, Industrial WDT disabled	
—			2	12	μA	VDD = 3.0V, Extended WDT disabled	
D022	Power-Down Current	ΔIWD	—	2.2	5	μA	VDD = 3.0V, Commercial
			—	2.2	6	μA	VDD = 3.0V, Industrial
			—	4	11	μA	VDD = 3.0V, Extended
	Supply Current ⁽³⁾ During read/write to EEPROM peripheral	ΔIEE	—	0.1	0.2	mA	FOSC = 4 MHz, Vdd = 5.5V, SCL = 400kHz

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kOhm.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

PIC12C5XX

13.3 DC CHARACTERISTICS:

PIC12C508A/509A (Commercial, Industrial, Extended)
PIC12C518/519 (Commercial, Industrial, Extended)
PIC12CR509A (Commercial, Industrial, Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise specified)					
		Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)					
		Operating voltage V_{DD} range as described in DC spec Section 13.1 and Section 13.2.					
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D030	Input Low Voltage I/O ports with TTL buffer	V_{IL}	V_{SS}	-	0.8V	V	For $4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$ otherwise Note 1 Note 1
D031	with Schmitt Trigger buffer		V_{SS}	-	$0.15V_{DD}$	V	
D032	MCLR, GP2/T0CKI (in EXTRC mode)		V_{SS}	-	$0.2V_{DD}$	V	
D033	OSC1 (in EXTRC mode)		V_{SS}	-	$0.2V_{DD}$	V	
D033	OSC1 (in XT and LP)		V_{SS}	-	$0.3V_{DD}$	V	
D040	Input High Voltage I/O ports with TTL buffer	V_{IH}	$0.25V_{DD} + 0.8\text{V}$	-	V_{DD}	V	$4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$ otherwise For entire V_{DD} range Note 1
D040A			2.0V	-	V_{DD}	V	
D041	with Schmitt Trigger buffer		$0.8V_{DD}$	-	V_{DD}	V	
D042	MCLR, GP2/T0CKI		$0.8V_{DD}$	-	V_{DD}	V	
D042A	OSC1 (XT and LP)		$0.7V_{DD}$	-	V_{DD}	V	
D043	OSC1 (in EXTRC mode)		$0.9V_{DD}$	-	V_{DD}	V	
D070	GPIO weak pull-up current (Note 4) MCLR pull-up current	I_{PUR} -	30 -	250 -	400 30	μA μA	$V_{DD} = 5\text{V}, V_{PIN} = V_{SS}$ $V_{DD} = 5\text{V}, V_{PIN} = V_{SS}$
D060	Input Leakage Current (Notes 2, 3) I/O ports	I_{IL}	-	-	± 1	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, Pin at hi-impedance
D061	T0CKI		-	-	± 5	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$
D063	OSC1		-	-	± 5	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, XT and LP osc configuration
D080	Output Low Voltage I/O ports	V_{OL}	-	-	0.6	V	$I_{OL} = 8.5\text{ mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+85^{\circ}\text{C}$
D080A			-	-	0.6	V	$I_{OL} = 7.0\text{ mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+125^{\circ}\text{C}$
D090	Output High Voltage I/O ports (Note 3)	V_{OH}	$V_{DD} - 0.7$	-	-	V	$I_{OH} = -3.0\text{ mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+85^{\circ}\text{C}$
D090A			$V_{DD} - 0.7$	-	-	V	$I_{OH} = -2.5\text{ mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+125^{\circ}\text{C}$
D100	Capacitive Loading Specs on Output Pins OSC2 pin	C_{OSC2}	-	-	15	pF	In XT and LP modes when external clock is used to drive OSC1.
D101	All I/O pins	C_{IO}	-	-	50	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C5XX be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: This spec. applies when GP3/MCLR is configured as MCLR. The leakage current of the MCLR circuit is higher than the standard I/O logic.

PIC12C5XX

TABLE 13-1: PULL-UP RESISTOR RANGES* - PIC12C508A, PIC12C509A, PIC12CR509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519

V _{DD} (Volts)	Temperature (°C)	Min	Typ	Max	Units
GP0/GP1					
2.5	–40	38K	42K	63K	Ω
	25	42K	48K	63K	Ω
	85	42K	49K	63K	Ω
	125	50K	55K	63K	Ω
5.5	–40	15K	17K	20K	Ω
	25	18K	20K	23K	Ω
	85	19K	22K	25K	Ω
	125	22K	24K	28K	Ω
GP3					
2.5	–40	285K	346K	417K	Ω
	25	343K	414K	532K	Ω
	85	368K	457K	532K	Ω
	125	431K	504K	593K	Ω
5.5	–40	247K	292K	360K	Ω
	25	288K	341K	437K	Ω
	85	306K	371K	448K	Ω
	125	351K	407K	500K	Ω

* These parameters are characterized but not tested.

PIC12C5XX

FIGURE 13-3: I/O TIMING - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519

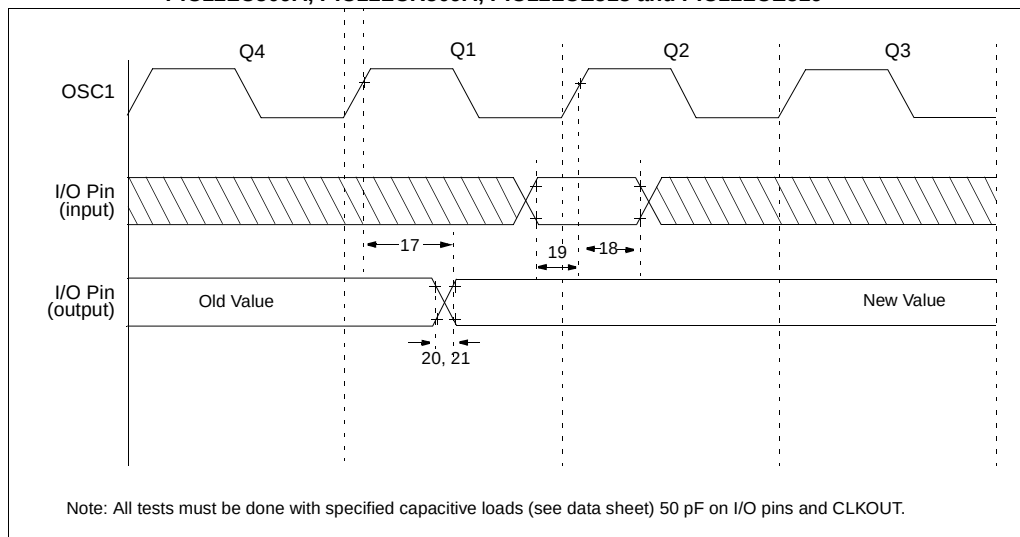


TABLE 13-4: TIMING REQUIREMENTS - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519

AC Characteristics		Standard Operating Conditions (unless otherwise specified)				
		Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)				
		Operating Voltage V_{DD} range is described in Section 13.1				
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units
17	TosH2ioV	OSC1 $\uparrow$ (Q1 cycle) to Port out valid ⁽³⁾	—	—	100*	ns
18	TosH2ioI	OSC1 $\uparrow$ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1 $\uparrow$ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time ^(2, 3)	—	10	25**	ns
21	TioF	Port output fall time ^(2, 3)	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in EXTRC mode.

3: See Figure 13-1 for loading conditions.

FIGURE 13-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519

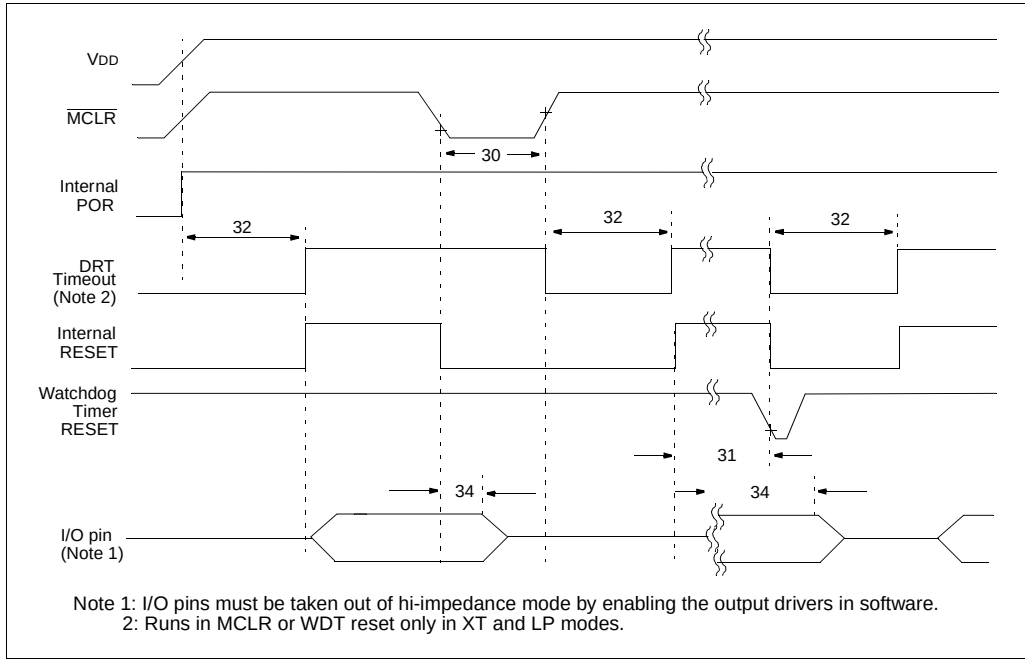


TABLE 13-5: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519

AC Characteristics Standard Operating Conditions (unless otherwise specified)							
Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)							
Operating Voltage VDD range is described in Section 13.1							
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
30	TmCL	MCLR Pulse Width (low)	2000*	—	—	ns	VDD = 5 V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9*	18*	30*	ms	VDD = 5 V (Commercial)
32	TDRT	Device Reset Timer Period ⁽²⁾	9*	18*	30*	ms	VDD = 5 V (Commercial)
34	Tioz	I/O Hi-impedance from MCLR Low	—	—	2000*	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 2: See Table 13-6.

PIC12C5XX

TABLE 14-1: DYNAMIC I_{DD} (TYPICAL) - WDT ENABLED, 25°C

Oscillator	Frequency	V _{DD} = 3.0V	V _{DD} = 5.5V
External RC	4 MHz	240 μA*	800 μA*
Internal RC	4 MHz	320 μA	800 μA
XT	4 MHz	300 μA	800 μA
LP	32 KHz	19 μA	50 μA

*Does not include current through external R&C.

FIGURE 14-3: TYPICAL I_{DD} VS. V_{DD}
(WDT DIS, 25°C, FREQUENCY
= 4MHz)

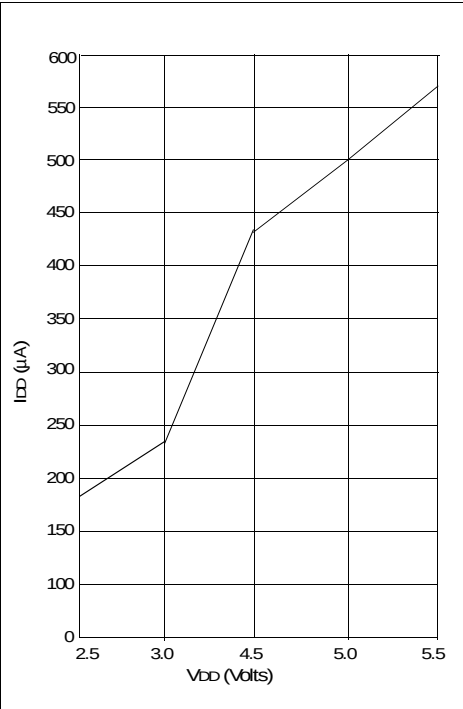


FIGURE 14-4: TYPICAL I_{DD} VS. FREQUENCY
(WDT DIS, 25°C, V_{DD} = 5.5V)

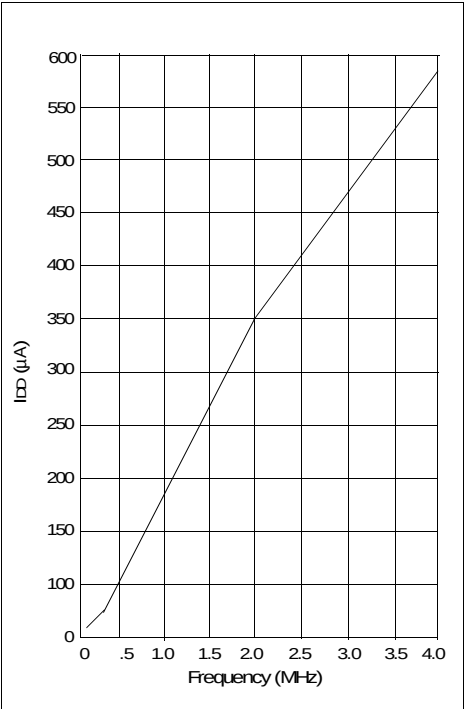


FIGURE 14-5: WDT TIMER TIME-OUT PERIOD vs. V_{DD}

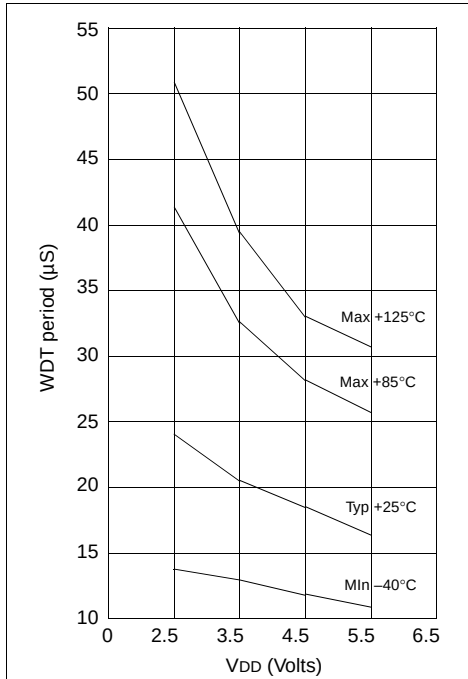


FIGURE 14-7: I_{OH} vs. V_{OH} , $V_{DD} = 2.5$ V

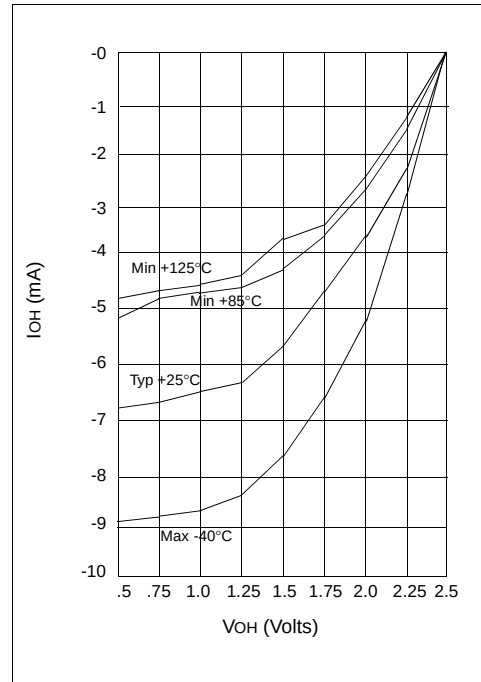


FIGURE 14-6: SHORT DRT PERIOD VS. V_{DD}

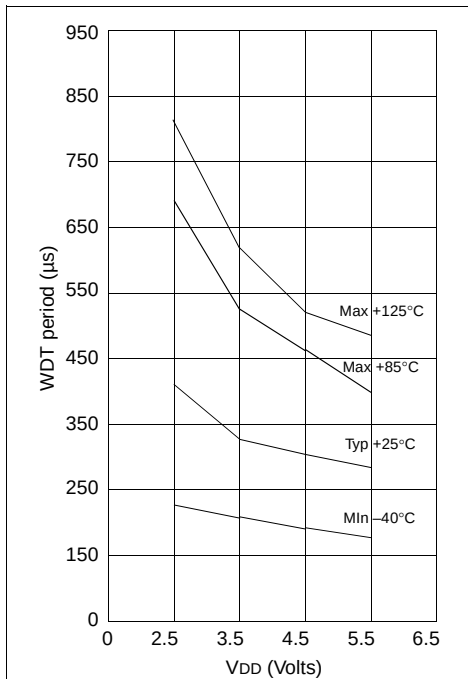
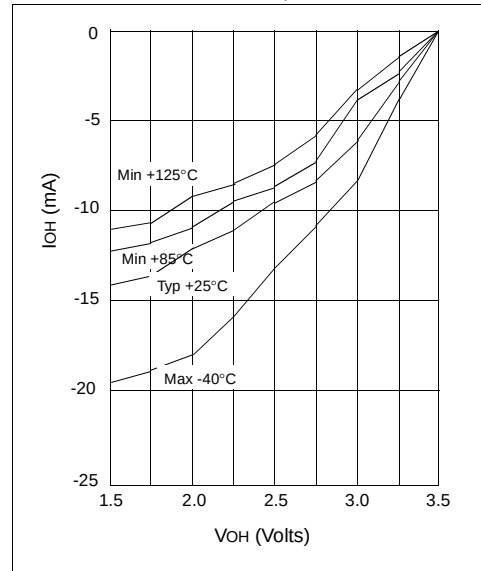


FIGURE 14-8: I_{OH} vs. V_{OH} , $V_{DD} = 3.5$ V



15.0 PACKAGING INFORMATION

15.1 Package Marking Information

8-Lead PDIP (300 mil)



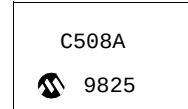
Example



8-Lead SOIC (150 mil)



Example



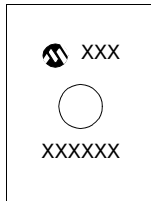
8-Lead SOIC (208 mil)



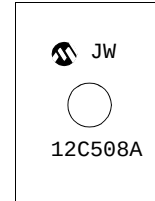
Example



8-Lead Windowed Ceramic Side Brazed (300 mil)



Example



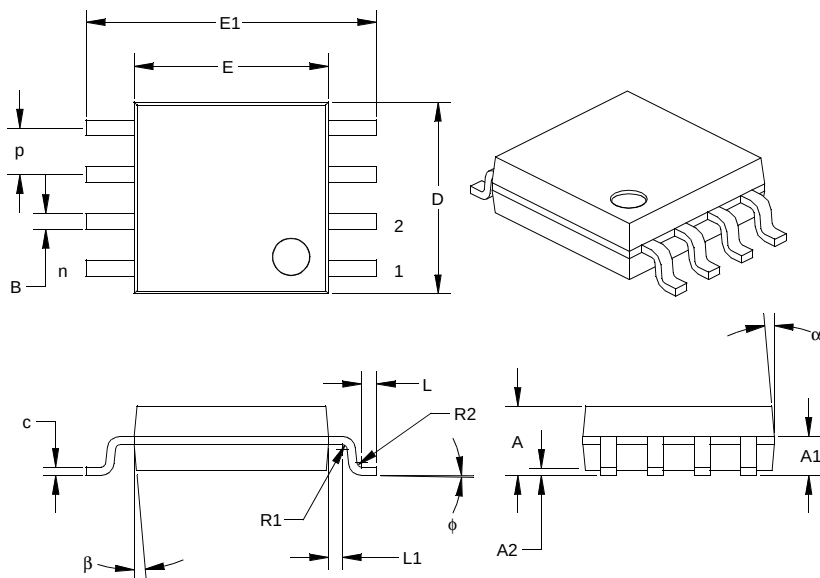
Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured
		O = Outside Vendor
		C = 5" Line
		S = 6" Line
		H = 8" Line
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

PIC12C5XX

Package Type: K04-056 8-Lead Plastic Small Outline (SM) – Medium, 208 mil



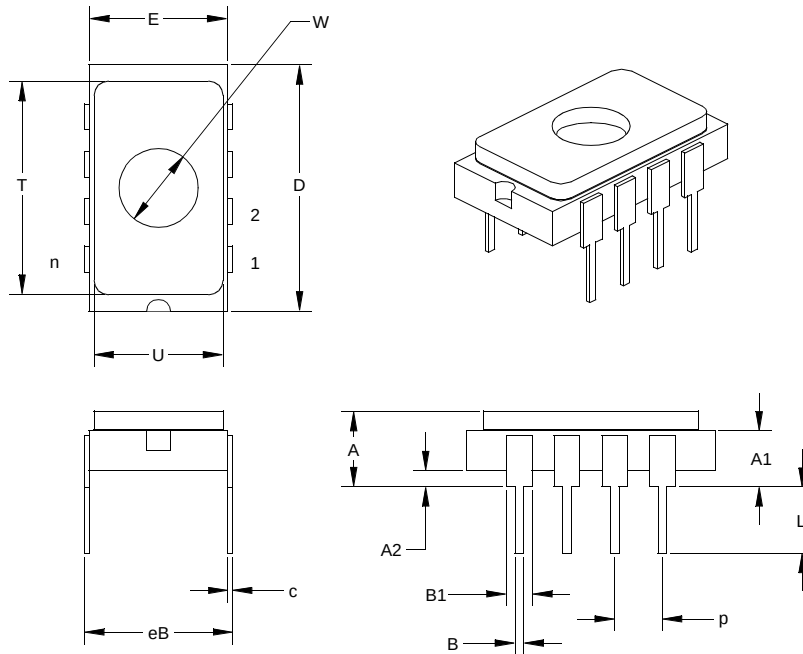
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.050			1.27	
Number of Pins	n		8			8	
Overall Pack. Height	A	0.070	0.074	0.079	1.78	1.89	2.00
Shoulder Height	A1	0.037	0.042	0.048	0.94	1.08	1.21
Standoff	A2	0.002	0.005	0.009	0.05	0.14	0.22
Molded Package Length	D [†]	0.200	0.205	0.210	5.08	5.21	5.33
Molded Package Width	E [‡]	0.203	0.208	0.213	5.16	5.28	5.41
Outside Dimension	E1	0.300	0.313	0.325	7.62	7.94	8.26
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	phi	0	4	8	0	4	8
Radius Centerline	L1	0.010	0.015	0.020	0.25	0.38	0.51
Lead Thickness	c	0.008	0.009	0.010	0.19	0.22	0.25
Lower Lead Width	B [†]	0.014	0.017	0.020	0.36	0.43	0.51
Mold Draft Angle Top	alpha	0	12	15	0	12	15
Mold Draft Angle Bottom	beta	0	12	15	0	12	15

* Controlling Parameter.

† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

Package Type: K04-084 8-Lead Ceramic Side Brazed Dual In-line with Window (JW) – 300 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		8			8	
Pitch	p	0.098	0.100	0.102	2.49	2.54	2.59
Lower Lead Width	B	0.016	0.018	0.020	0.41	0.46	0.51
Upper Lead Width	B1	0.050	0.055	0.060	1.27	1.40	1.52
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.145	0.165	0.185	3.68	4.19	4.70
Top of Body to Seating Plane	A1	0.103	0.123	0.143	2.62	3.12	3.63
Base to Seating Plane	A2	0.025	0.035	0.045	0.64	0.89	1.14
Tip to Seating Plane	L	0.130	0.140	0.150	3.30	3.56	3.81
Package Length	D	0.510	0.520	0.530	12.95	13.21	13.46
Package Width	E	0.280	0.290	0.300	7.11	7.37	7.62
Overall Row Spacing	eB	0.310	0.338	0.365	7.87	8.57	9.27
Window Diameter	W	0.161	0.166	0.171	4.09	4.22	4.34
Lid Length	T	0.440	0.450	0.460	11.18	11.43	11.68
Lid Width	U	0.260	0.270	0.280	6.60	6.86	7.11

* Controlling Parameter.

