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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.209", 5.30mm Width)
Supplier Device Package	8-SOIJ
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12c508a-04i-sm

PIC12C5XX

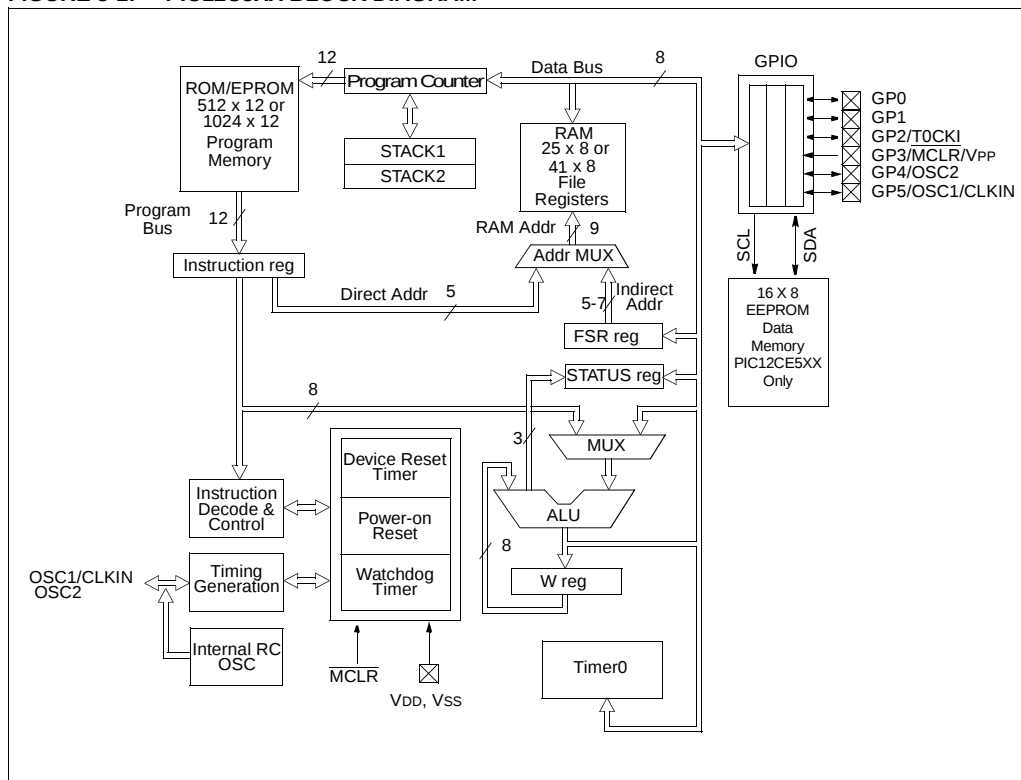
NOTES:

PIC12C5XX

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PIC12C5XX

FIGURE 3-1: PIC12C5XX BLOCK DIAGRAM



6.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (T_{osc}) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

6.1.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-4). Therefore, it is necessary for T0CKI to be high for at least $2T_{osc}$ (and a small RC delay of 20 ns) and low for at least $2T_{osc}$ (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least $4T_{osc}$ (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

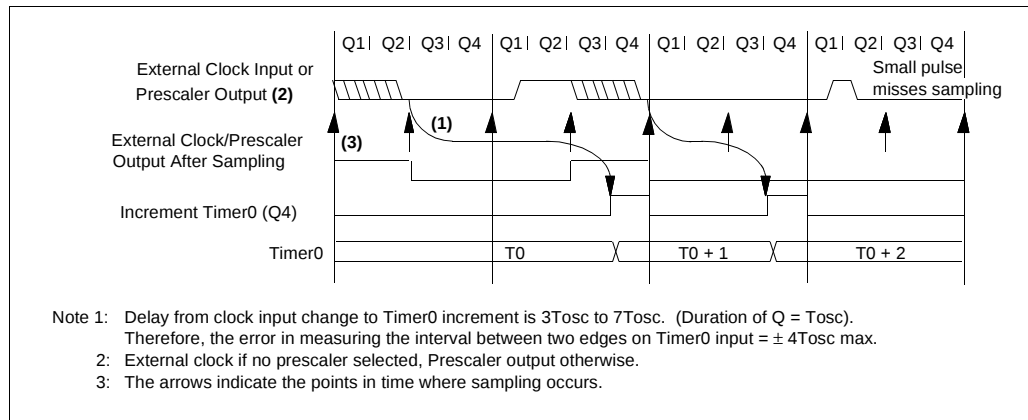
6.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 6-4 shows the delay from the external clock edge to the timer incrementing.

6.1.3 OPTION REGISTER EFFECT ON GP2 TRIS

If the option register is set to read TIMER0 from the pin, the port is forced to an input regardless of the TRIS register setting.

FIGURE 6-4: TIMER0 TIMING WITH EXTERNAL CLOCK



7.0.2 SERIAL CLOCK

This SCL input is used to synchronize the data transfer from and to the device.

7.1 BUS CHARACTERISTICS

The following **bus protocol** is to be used with the EEPROM data memory.

- Data transfer may be initiated only when the bus is not busy.

During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 7-3).

7.1.1 BUS NOT BUSY (A)

Both data and clock lines remain HIGH.

7.1.2 START DATA TRANSFER (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

7.1.3 STOP DATA TRANSFER (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

7.1.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

7.1.5 ACKNOWLEDGE

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: Acknowledge bits are not generated if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition (Figure 7-4).

7.3 WRITE OPERATIONS

7.3.1 BYTE WRITE

Following the start signal from the master, the device code (4 bits), the don't care bits (3 bits), and the R/W bit (which is a logic low) are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer. Only the lower four address bits are used by the device, and the upper four bits are don't cares. The address byte is acknowledgeable and the master device will then transmit the data word to be written into the addressed memory location. The memory acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time will not generate acknowledge signals (Figure 7-7). After a byte write command, the internal address counter will not be incremented and will point to the same address location that was just written. If a stop bit is transmitted to the device at any point in the write command sequence before the entire sequence is complete, then the command will abort and no data will be written. If more than 8 data bits are transmitted before the stop bit is sent, then the device will clear the previously loaded byte and begin loading the data buffer again. If more than one data byte is transmitted to the device and a stop bit is sent before a full eight data bits have been transmitted, then the write command will abort and no data will be written. The EEPROM memory employs a VCC threshold detector circuit which disables the internal erase/write logic if the VCC is below minimum VDD.

Byte write operations must be preceded and immediately followed by a bus not busy bus cycle where both SDA and SCL are held high.

7.4 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/W = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the start bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-6 for flow diagram.

FIGURE 7-6: ACKNOWLEDGE POLLING FLOW

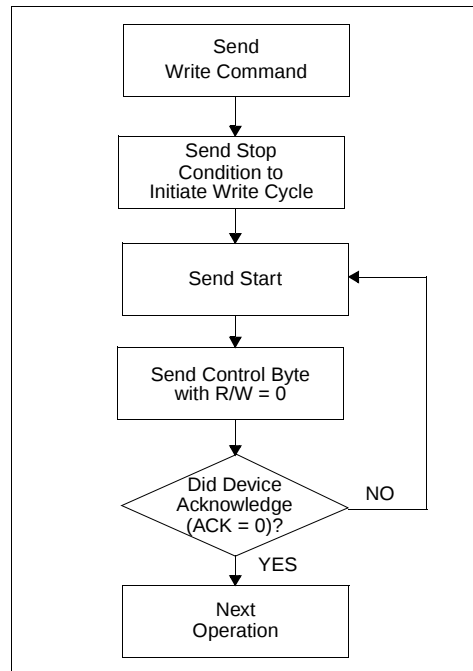


FIGURE 7-7: BYTE WRITE

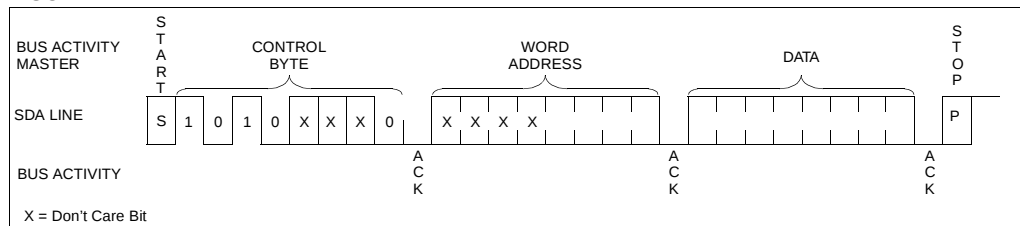


FIGURE 8-8: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

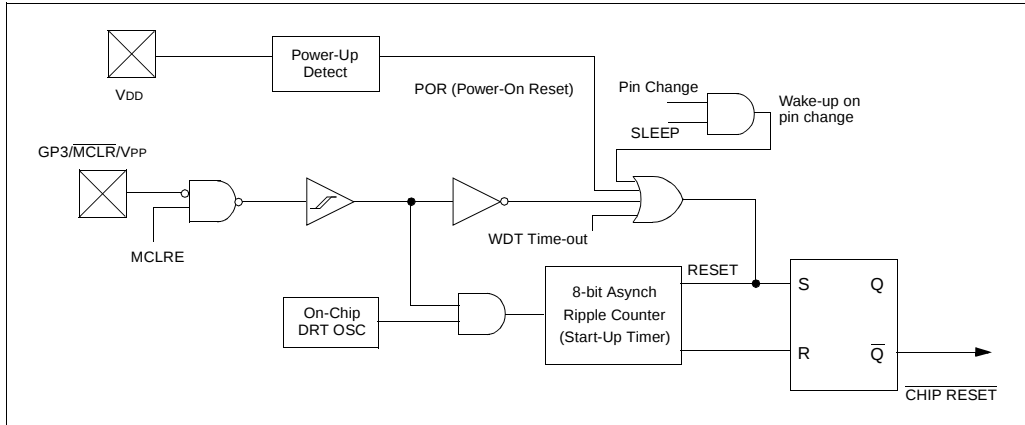


FIGURE 8-9: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ PULLED LOW)

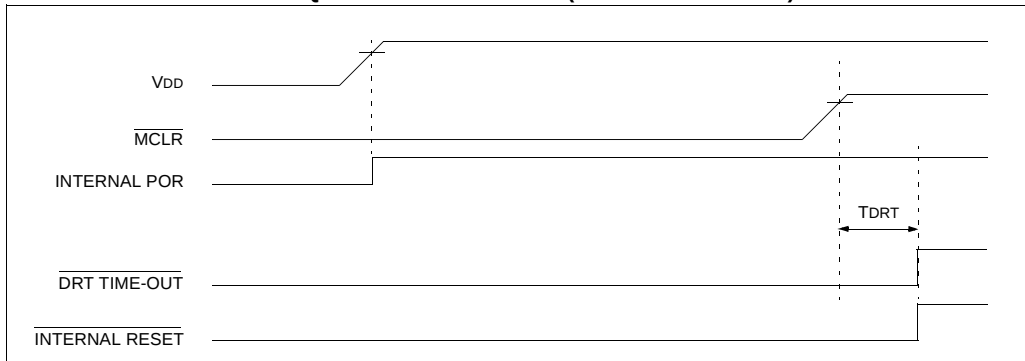
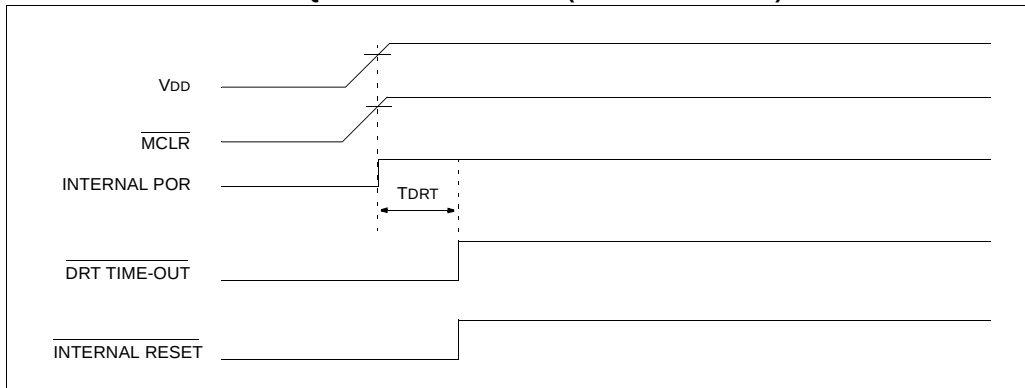


FIGURE 8-10: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD}): FAST V_{DD} RISE TIME



CALL Subroutine Call

Syntax: [label] CALL k

Operands: $0 \leq k \leq 255$

Operation: (PC) + 1 → Top of Stack;
 $k \rightarrow PC<7:0>$;
 (STATUS<6:5>) → PC<10:9>;
 $0 \rightarrow PC<8>$

Status Affected: None

Encoding:

1001	kkkk	kkkk
------	------	------

Description: Subroutine call. First, return address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two cycle instruction.

Words: 1

Cycles: 2

Example: HERE CALL THERE

Before Instruction
 PC = address (HERE)

After Instruction
 PC = address (THERE)
 TOS = address (HERE + 1)

CLRF Clear f

Syntax: [label] CLRF f

Operands: $0 \leq f \leq 31$

Operation: $00h \rightarrow (f)$;
 $1 \rightarrow Z$

Status Affected: Z

Encoding:

0000	011f	ffff
------	------	------

Description: The contents of register 'f' are cleared and the Z bit is set.

Words: 1

Cycles: 1

Example: CLRF FLAG_REG

Before Instruction
 FLAG_REG = 0x5A

After Instruction
 FLAG_REG = 0x00
 Z = 1

CLRW Clear W

Syntax: [label] CLRW

Operands: None

Operation: $00h \rightarrow (W)$;
 $1 \rightarrow Z$

Status Affected: Z

Encoding:

0000	0100	0000
------	------	------

Description: The W register is cleared. Zero bit (Z) is set.

Words: 1

Cycles: 1

Example: CLRW

Before Instruction
 W = 0x5A

After Instruction
 W = 0x00
 Z = 1

CLRWDTClear Watchdog Timer

Syntax: [label] CLRWDTClear Watchdog Timer

Operands: None

Operation: $00h \rightarrow WDT$;
 $0 \rightarrow WDT$ prescaler (if assigned);
 $1 \rightarrow \overline{TO}$;
 $1 \rightarrow \overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

0000	0000	0100
------	------	------

Description: The CLRWDTClear Watchdog Timer instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

Words: 1

Cycles: 1

Example: CLRWDTClear Watchdog Timer

Before Instruction
 WDT counter = ?

After Instruction
 WDT counter = 0x00
 WDT prescale = 0
 $\overline{TO}$ = 1
 $\overline{PD}$ = 1

10.10 MPLAB Integrated Development Environment Software

The MPLAB IDE Software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a windows based application which contains:

- A full featured editor
- Three operating modes
 - editor
 - emulator
 - simulator
- A project manager
- Customizable tool bar and key mapping
- A status bar with project information
- Extensive on-line help

MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PICmicro[®] tools (automatically updates all project information)
- Debug using:
 - source files
 - absolute listing file

The ability to use MPLAB with Microchip's simulator allows a consistent platform and the ability to easily switch from the low cost simulator to the full featured emulator with minimal retraining due to development tools.

10.11 Assembler (MPASM)

The MPASM Universal Macro Assembler is a PC-hosted symbolic assembler. It supports all microcontroller series including the PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX, and PIC17CXX families.

MPASM offers full featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from MPLAB-ICE, Microchip's Universal Emulator System.

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro assembly capability.
- Produces all the files (Object, Listing, Symbol, and special) required for symbolic debug with Microchip's emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a rich directive language to support programming of the PICmicro[®]. Directives are helpful in making the development of your assemble source code shorter and more maintainable.

10.12 Software Simulator (MPLAB-SIM)

The MPLAB-SIM Software Simulator allows code development in a PC host environment. It allows the user to simulate the PICmicro[®] series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in; single step, execute until break, or in a trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C17 and MPASM. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

10.13 MPLAB-C17 Compiler

The MPLAB-C17 Code Development System is a complete ANSI 'C' compiler and integrated development environment for Microchip's PIC17CXXX family of microcontrollers. The compiler provides powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compiler provides symbol information that is compatible with the MPLAB IDE memory display.

10.14 Fuzzy Logic Development System (fuzzyTECH-MP)

fuzzyTECH-MP fuzzy logic development tool is available in two versions - a low cost introductory version, MP Explorer, for designers to gain a comprehensive working knowledge of fuzzy logic system design; and a full-featured version, *fuzzyTECH-MP*, Edition for implementing more complex systems.

Both versions include Microchip's *fuzzyLAB™* demonstration board for hands-on experience with fuzzy logic systems implementation.

10.15 SEEVAL[®] Evaluation and Programming System

The SEEVAL SEEPROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials™ and secure serials. The Total Endurance™ Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

NOTES:

11.1 DC CHARACTERISTICS: PIC12C508/509 (Commercial, Industrial, Extended)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)					
Parm No.	Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
D001	Supply Voltage	V _{DD}	2.5 3.0		5.5 5.5	V V	Fosc = DC to 4 MHz (Commercial/ Industrial) Fosc = DC to 4 MHz (Extended)
D002	RAM Data Retention Voltage ⁽²⁾	V _{DR}		1.5*		V	Device in SLEEP mode
D003	V _{DD} Start Voltage to ensure Power-on Reset	V _{POR}		V _{SS}		V	See section on Power-on Reset for details
D004	V _{DD} Rise Rate to ensure Power-on Reset	S _{VDD}	0.05 *			V/ms	See section on Power-on Reset for details
D010 D010C D010A	Supply Current ⁽³⁾	I _{DD}	—	.78 1.1 10 14 14	2.4 2.4 27 35 35	mA mA μA μA μA	XT and EXTRC options ⁽⁴⁾ Fosc = 4 MHz, V _{DD} = 5.5V INTRC Option Fosc = 4 MHz, V _{DD} = 5.5V LP OPTION, Commercial Temperature Fosc = 32 kHz, V _{DD} = 3.0V, WDT disabled LP OPTION, Industrial Temperature Fosc = 32 kHz, V _{DD} = 3.0V, WDT disabled LP OPTION, Extended Temperature Fosc = 32 kHz, V _{DD} = 3.0V, WDT disabled
D020 D021 D021B	Power-Down Current ⁽⁵⁾	I _{PD}	— — —	0.25 0.25 2	4 5 18	μA μA μA	V _{DD} = 3.0V, Commercial WDT disabled V _{DD} = 3.0V, Industrial WDT disabled V _{DD} = 3.0V, Extended WDT disabled
D022		ΔI _{WDT}	— — —	3.75 3.75 3.75	8 9 14	μA μA μA	V _{DD} = 3.0V, Commercial V _{DD} = 3.0V, Industrial V _{DD} = 3.0V, Extended

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all I_{DD} measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V_{SS}, T0CKI = V_{DD}, MCLR = V_{DD}; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through R_{ext}. The current through the resistor can be estimated by the formula: I_R = V_{DD}/2R_{ext} (mA) with R_{ext} in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD} or V_{SS}.

TABLE 11-5: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC12C508/C509

AC Characteristics Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) Operating Voltage V_{DD} range is described in Section 11.1							
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
30	TmCL	MCLR Pulse Width (low)	2000*	—	—	ns	$V_{DD} = 5\text{ V}$
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9*	18*	30*	ms	$V_{DD} = 5\text{ V}$ (Commercial)
32	TDRT	Device Reset Timer Period ⁽²⁾	9*	18*	30*	ms	$V_{DD} = 5\text{ V}$ (Commercial)
34	Tioz	I/O Hi-impedance from MCLR Low	—	—	2000*	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 2: See Table 11-6.

TABLE 11-6: DRT (DEVICE RESET TIMER PERIOD - PIC12C508/C509)

Oscillator Configuration	POR Reset	Subsequent Resets
IntRC & ExtRC	18 ms (typical)	300 μs (typical)
XT & LP	18 ms (typical)	18 ms (typical)

12.0 DC AND AC CHARACTERISTICS - PIC12C508/PIC12C509

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified V_{DD} range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean - 3σ) respectively, where σ is standard deviation.

FIGURE 12-1: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE ($V_{DD} = 2.5V$)

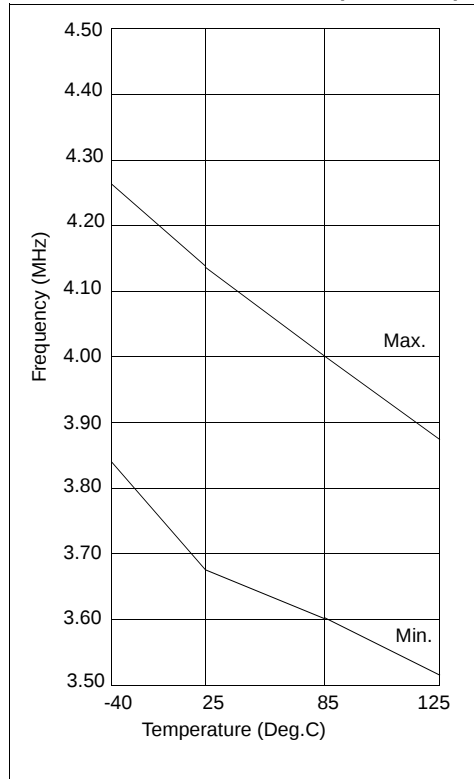
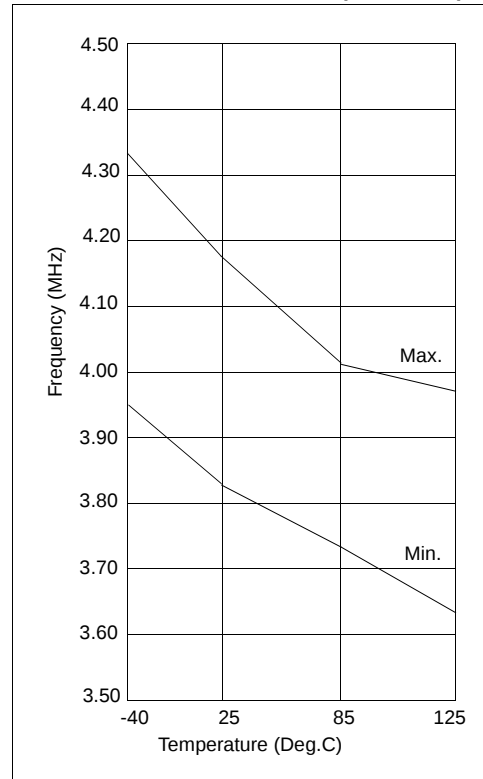


FIGURE 12-2: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE ($V_{DD} = 5.0V$)



PIC12C5XX

TABLE 12-1: DYNAMIC I_{DD} (TYPICAL) - WDT ENABLED, 25°C

Oscillator	Frequency	V _{DD} = 2.5V	V _{DD} = 5.5V
External RC	4 MHz	250 µA*	780 µA*
Internal RC	4 MHz	420 µA	1.1 mA
XT	4 MHz	251 µA	780 µA
LP	32 KHz	15 µA	37 µA

*Does not include current through external R&C.

FIGURE 12-3: WDT TIMER TIME-OUT PERIOD VS. V_{DD}

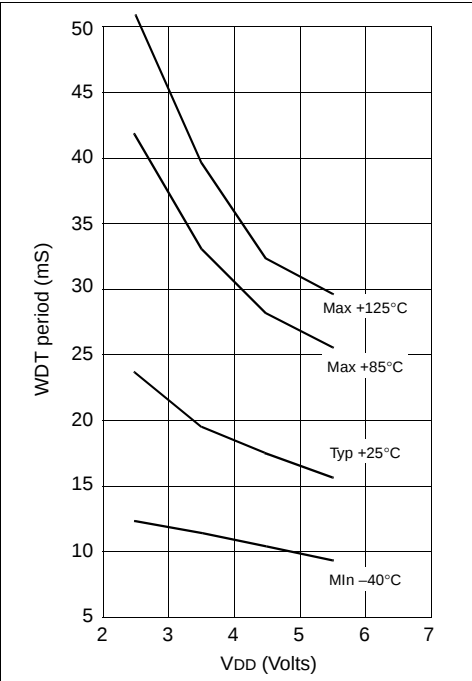
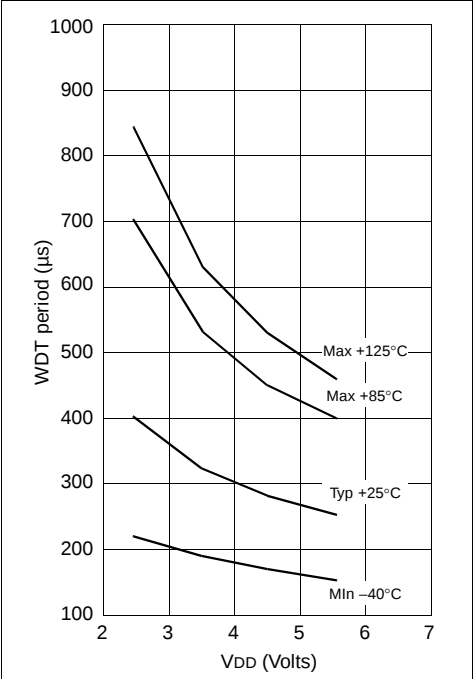


FIGURE 12-4: SHORT DRT PERIOD VS. V_{DD}



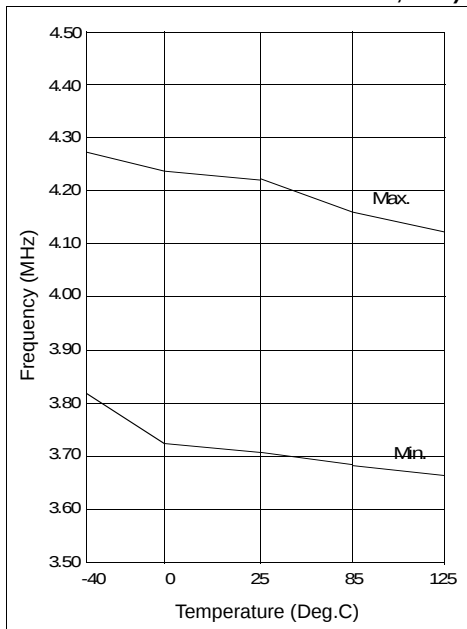
NOTES:

14.0 DC AND AC CHARACTERISTICS - PIC12C508A/PIC12C509A/ PIC12LC508A/PIC12LC509A, PIC12CE518/PIC12CE519/PIC12CR509A/ PIC12LCE518/PIC12LCE519/ PIC12LCR509A

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified V_{DD} range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean - 3σ) respectively, where σ is standard deviation.

**FIGURE 14-1: CALIBRATED INTERNAL RC
FREQUENCY RANGE VS.
TEMPERATURE ($V_{DD} = 5.0V$)
(INTERNAL RC IS
CALIBRATED TO 25°C, 5.0V)**



**FIGURE 14-2: CALIBRATED INTERNAL RC
FREQUENCY RANGE VS.
TEMPERATURE ($V_{DD} = 2.5V$)
(INTERNAL RC IS
CALIBRATED TO 25°C, 5.0V)**

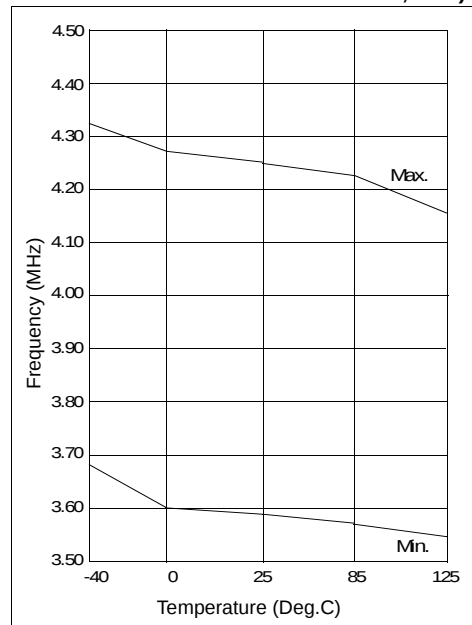


FIGURE 14-9: IOL vs. VOL, VDD = 2.5 V

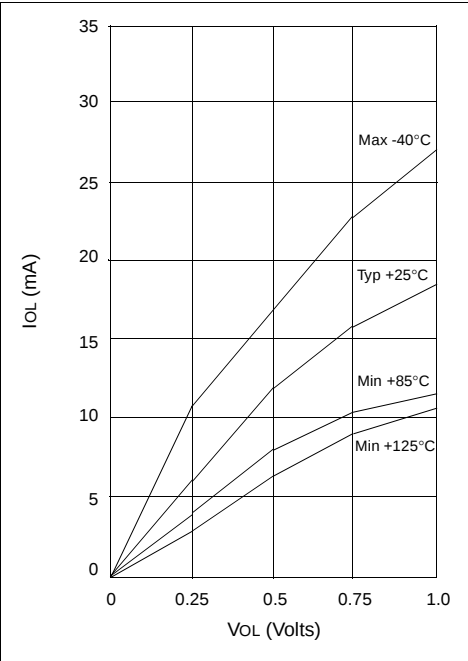


FIGURE 14-11: IOH vs. VOH, VDD = 5.5 V

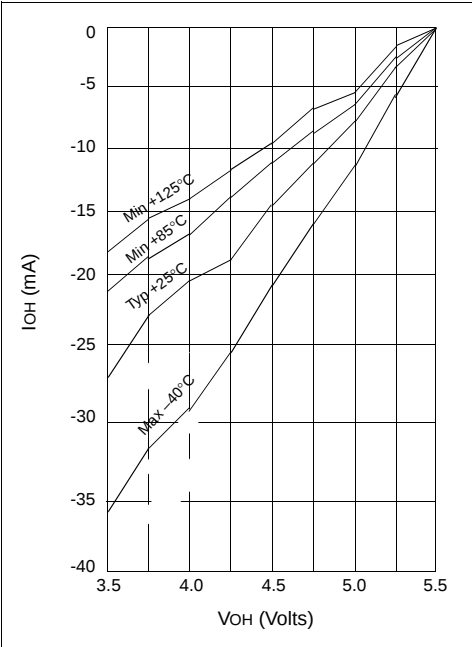


FIGURE 14-10: IOL vs. VOL, VDD = 3.5 V

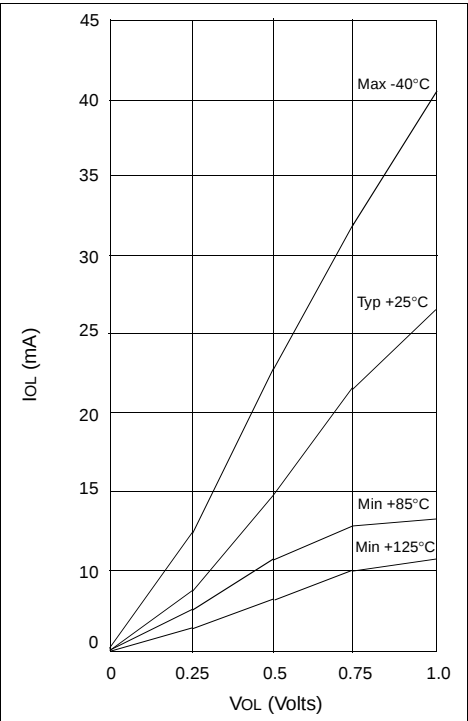
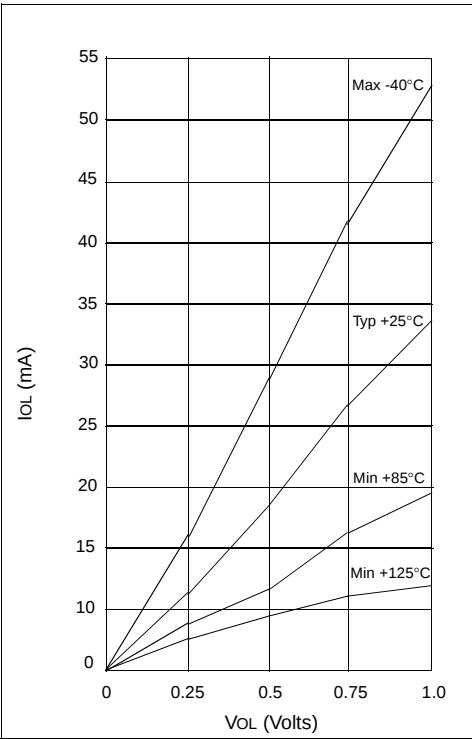
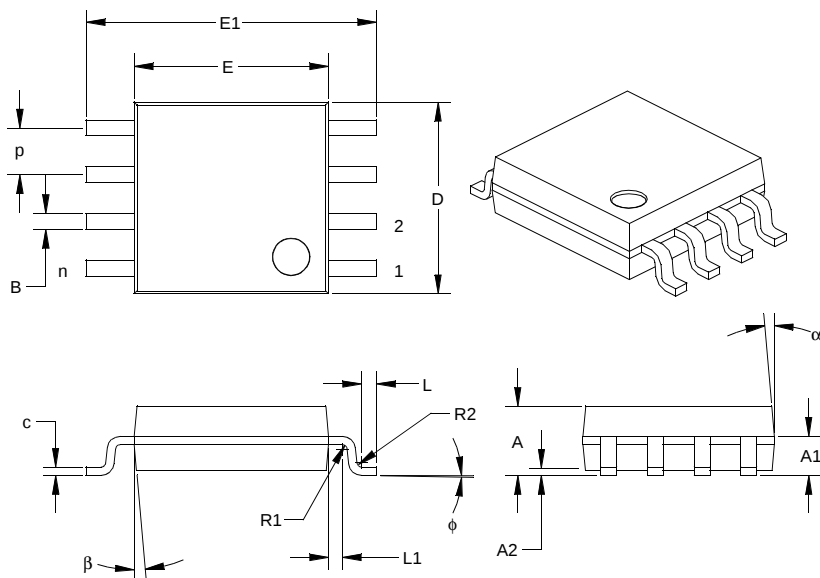


FIGURE 14-12: IOL vs. VOL, VDD = 5.5 V



PIC12C5XX

Package Type: K04-056 8-Lead Plastic Small Outline (SM) – Medium, 208 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.050			1.27	
Number of Pins	n		8			8	
Overall Pack. Height	A	0.070	0.074	0.079	1.78	1.89	2.00
Shoulder Height	A1	0.037	0.042	0.048	0.94	1.08	1.21
Standoff	A2	0.002	0.005	0.009	0.05	0.14	0.22
Molded Package Length	D [†]	0.200	0.205	0.210	5.08	5.21	5.33
Molded Package Width	E [‡]	0.203	0.208	0.213	5.16	5.28	5.41
Outside Dimension	E1	0.300	0.313	0.325	7.62	7.94	8.26
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	φ	0	4	8	0	4	8
Radius Centerline	L1	0.010	0.015	0.020	0.25	0.38	0.51
Lead Thickness	c	0.008	0.009	0.010	0.19	0.22	0.25
Lower Lead Width	B [†]	0.014	0.017	0.020	0.36	0.43	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter.

† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."



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