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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.209", 5.30mm Width)
Supplier Device Package	8-SOIJ
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic12c508t-04-sm">https://www.e-xfl.com/product-detail/microchip-technology/pic12c508t-04-sm</a>

## 5.0 I/O PORT

As with any other register, the I/O register can be written and read under program control. However, read instructions (e.g., `MOVF GPIO, W`) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers are all set. See Section 7.0 for SCL and SDA description for PIC12CE5XX.

### 5.1 GPIO

GPIO is an 8-bit I/O register. Only the low order 6 bits are used (GP5:GP0). Bits 7 and 6 are unimplemented and read as '0's. Please note that GP3 is an input only pin. The configuration word can set several I/O's to alternate functions. When acting as alternate functions the pins will read as '0' during port read. Pins GP0, GP1, and GP3 can be configured with weak pull-ups and also with wake-up on change. The wake-up on change and weak pull-up functions are not pin selectable. If pin 4 is configured as MCLR, weak pull-up is always on and wake-up on change for this pin is not enabled.

### 5.2 TRIS Register

The output driver control register is loaded with the contents of the W register by executing the `TRIS f` instruction. A '1' from a TRIS register bit puts the corresponding output driver in a hi-impedance mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer. The exceptions are GP3 which is input only and GP2 which may be controlled by the option register, see Figure 4-5.

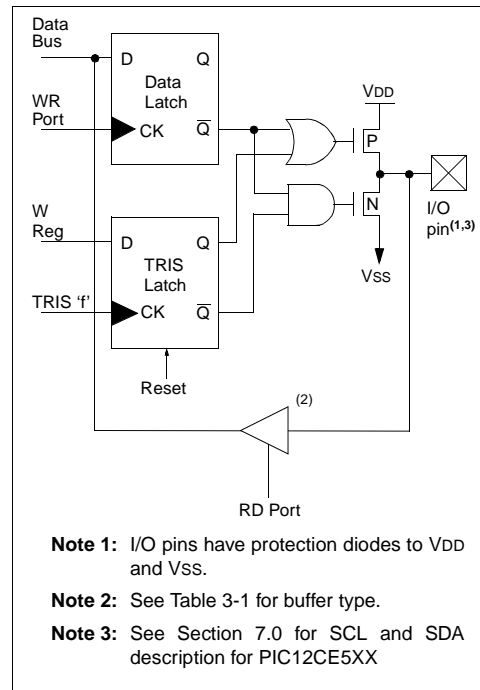
**Note:** A read of the ports reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high, but the external system is holding it low, a read of the port will indicate that the pin is low.

The TRIS registers are "write-only" and are set (output drivers disabled) upon RESET.

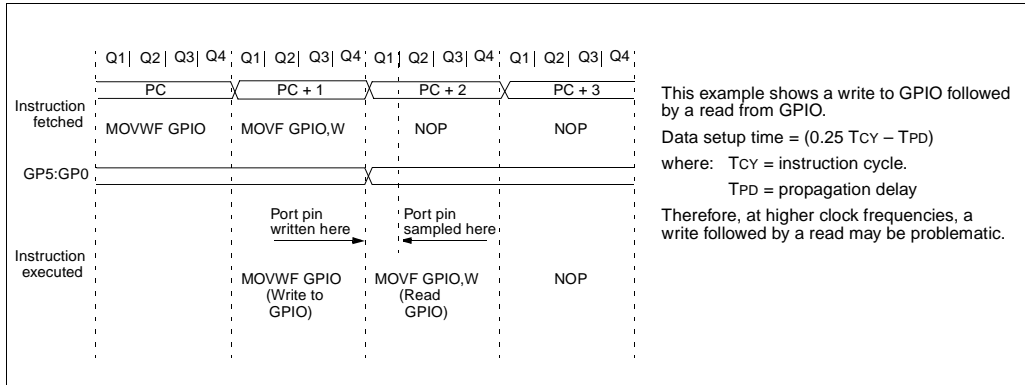
## 5.3 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 5-1. All port pins, except GP3 which is input only, may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., `MOVF GPIO, W`). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit in TRIS must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin (except GP3) can be programmed individually as input or output.

**FIGURE 5-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN**



**FIGURE 5-2: SUCCESSIVE I/O OPERATION**



## 6.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
  - Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
  - Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module.

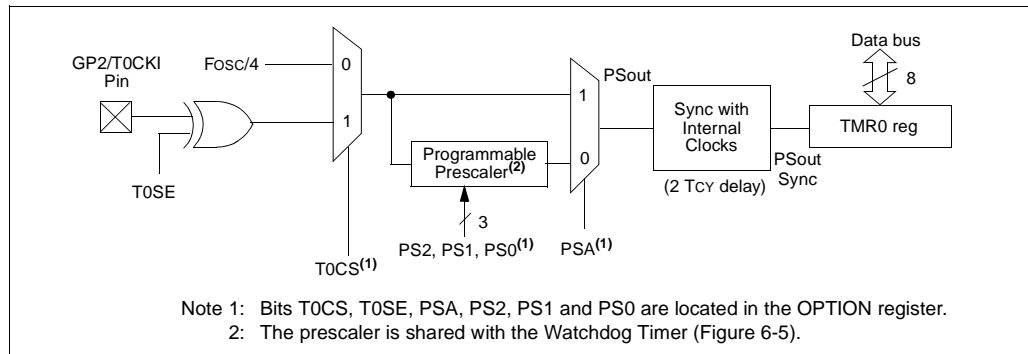
Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two instruction cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The T0SE bit (OPTION<4>) determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.1.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. Section 6.2 details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 6-1.

**FIGURE 6-1: TIMER0 BLOCK DIAGRAM**



## 6.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (TOSC) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

### 6.1.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-4). Therefore, it is necessary for T0CKI to be high for at least 2TOSC (and a small RC delay of 20 ns) and low for at least 2TOSC (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

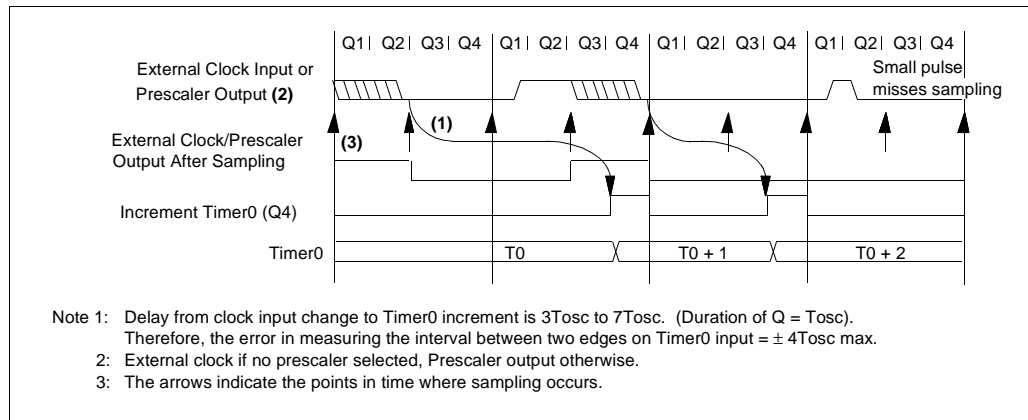
### 6.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 6-4 shows the delay from the external clock edge to the timer incrementing.

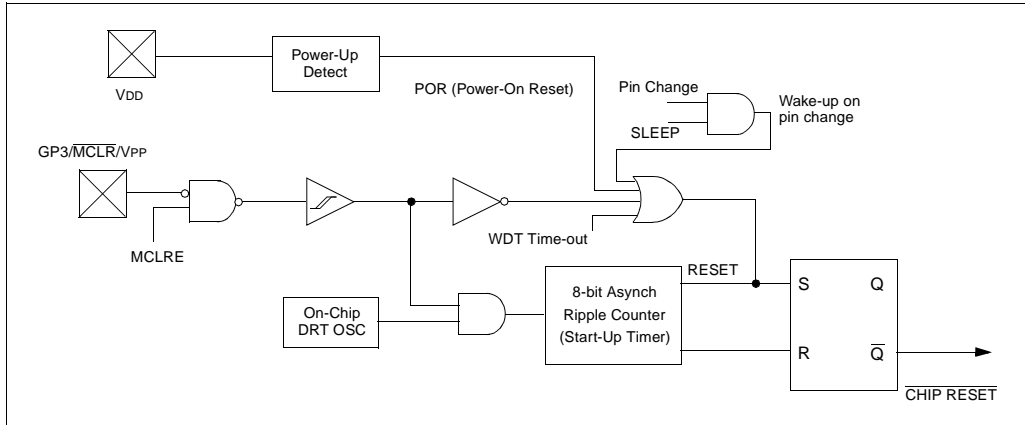
### 6.1.3 OPTION REGISTER EFFECT ON GP2 TRIS

If the option register is set to read TIMER0 from the pin, the port is forced to an input regardless of the TRIS register setting.

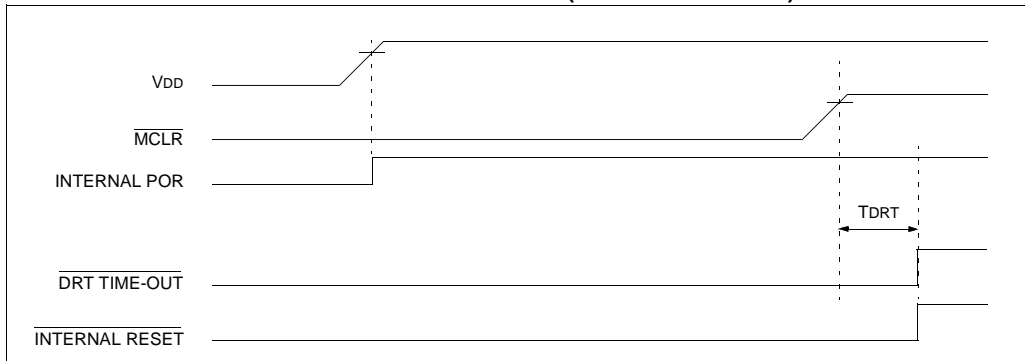
**FIGURE 6-4: TIMER0 TIMING WITH EXTERNAL CLOCK**



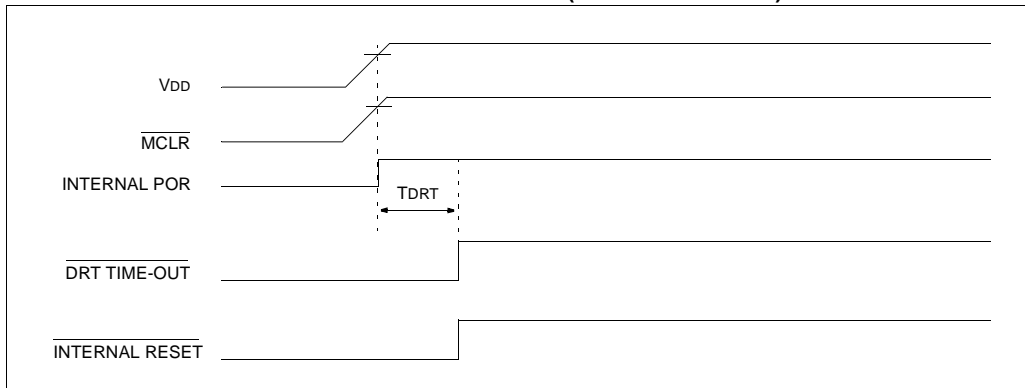
**FIGURE 8-8: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT**



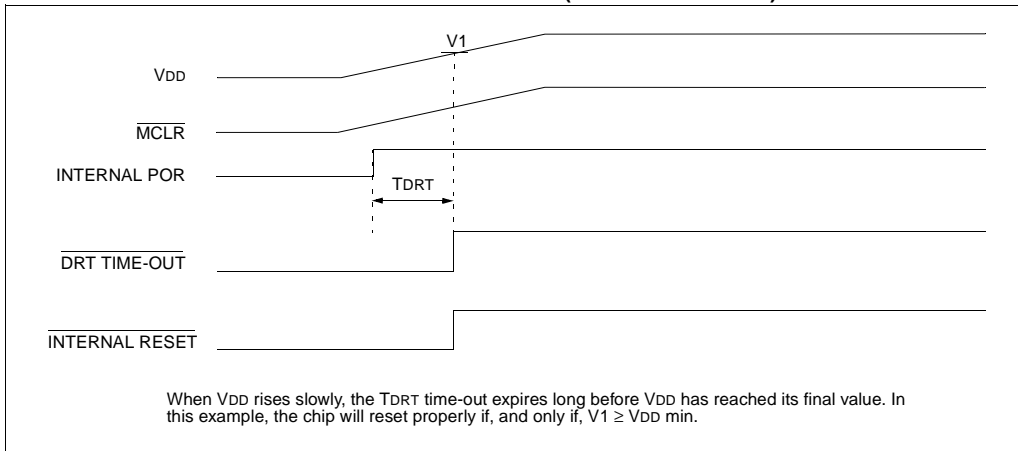
**FIGURE 8-9: TIME-OUT SEQUENCE ON POWER-UP ( $\overline{\text{MCLR}}$  PULLED LOW)**



**FIGURE 8-10: TIME-OUT SEQUENCE ON POWER-UP ( $\overline{\text{MCLR}}$  TIED TO  $V_{DD}$ ): FAST  $V_{DD}$  RISE TIME**



**FIGURE 8-11: TIME-OUT SEQUENCE ON POWER-UP ( $\overline{\text{MCLR}}$  TIED TO  $\text{V}_{\text{DD}}$ ): SLOW  $\text{V}_{\text{DD}}$  RISE TIME**



## 8.5 Device Reset Timer (DRT)

In the PIC12C5XX, DRT runs from RESET and varies based on oscillator selection (see Table 8-5.)

The DRT operates on an internal RC oscillator. The processor is kept in RESET as long as the DRT is active. The DRT delay allows  $\text{V}_{\text{DD}}$  to rise above  $\text{V}_{\text{DD min}}$ , and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the device in a RESET condition for approximately 18 ms after  $\overline{\text{MCLR}}$  has reached a logic high ( $\text{V}_{\text{IH}}\overline{\text{MCLR}}$ ) level. Thus, programming GP3/ $\overline{\text{MCLR}}$ / $\text{V}_{\text{PP}}$  as  $\overline{\text{MCLR}}$  and using an external RC network connected to the  $\overline{\text{MCLR}}$  input is not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications, as well as allowing the use of the GP3/ $\overline{\text{MCLR}}$ / $\text{V}_{\text{PP}}$  pin as a general purpose input.

The Device Reset time delay will vary from chip to chip due to  $\text{V}_{\text{DD}}$ , temperature, and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out. This is particularly important for applications using the WDT to wake from SLEEP mode automatically.

## 8.6 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the external RC oscillator of the GP5/OSC1/CLKIN pin and the internal 4 MHz oscillator. That means that the WDT will run even if the main processor clock has been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT reset or wake-up reset generates a device RESET.

The  $\overline{\text{TO}}$  bit ( $\text{STATUS}\langle 4 \rangle$ ) will be cleared upon a Watchdog Timer reset.

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Section 8.1). Refer to the PIC12C5XX Programming Specifications to determine how to access the configuration word.

**TABLE 8-5: DRT (DEVICE RESET TIMER PERIOD)**

Oscillator Configuration	POR Reset	Subsequent Resets
IntRC & ExtRC	18 ms (typical)	300 $\mu\text{s}$ (typical)
XT & LP	18 ms (typical)	18 ms (typical)

## 8.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, a time-out period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see DC specs).

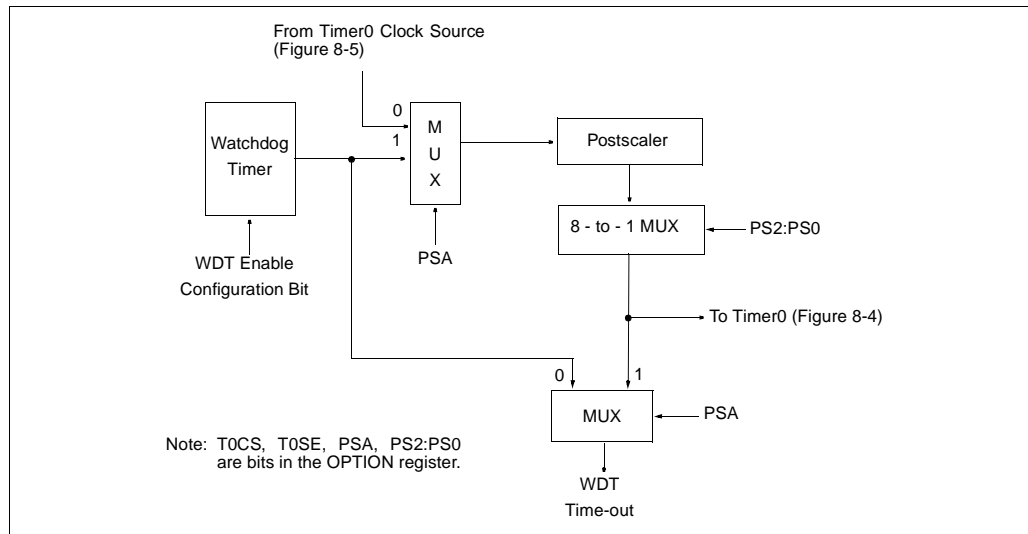
Under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

## 8.6.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The SLEEP instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT wake-up reset.

**FIGURE 8-12: WATCHDOG TIMER BLOCK DIAGRAM**



**TABLE 8-6: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	OPTION	GPWU	GPPU	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: Shaded boxes = Not used by Watchdog Timer, – = unimplemented, read as '0', u = unchanged



# PIC12C5XX

BSF	Bit Set f		
Syntax:	[ <i>label</i> ] BSF    f,b		
Operands:	$0 \leq f \leq 31$ $0 \leq b \leq 7$		
Operation:	$1 \rightarrow (f<b>)$		
Status Affected:	None		
Encoding:	0101	bbbf	ffff
Description:	Bit 'b' in register 'f' is set.		
Words:	1		
Cycles:	1		
Example:	BSF	FLAG_REG,	7
Before Instruction			
FLAG_REG = 0x0A			
After Instruction			
FLAG_REG = 0x8A			

BTFSC		Bit Test f, Skip if Clear				
Syntax:	[ <i>label</i> ] BTFSC f,b					
Operands:	0 ≤ f ≤ 31 0 ≤ b ≤ 7					
Operation:	skip if (f<b>) = 0					
Status Affected:	None					
Encoding:	<table border="1"><tr><td>0110</td><td>bbbf</td><td>ffff</td></tr></table>			0110	bbbf	ffff
0110	bbbf	ffff				
Description:	If bit 'b' in register 'f' is 0 then the next instruction is skipped.  If bit 'b' is 0 then the next instruction fetched during the current instruction execution is discarded, and an NOP is executed instead, making this a 2 cycle instruction.					
Words:	1					
Cycles:	1(2)					
Example:	HERE FALSE TRUE	BTFSC GOTO • • •	FLAG, 1 PROCESS_CODE			
Before Instruction						
PC	=	address (HERE)				
After Instruction						
if FLAG<1>	=	0,				
PC	=	address (TRUE);				
if FLAG<1>	=	1,				
PC	=	address (FALSE)				

BTFSS		Bit Test f, Skip if Set																
Syntax:	[ <i>label</i> ] BTFSS f,b																	
Operands:	0 ≤ f ≤ 31 0 ≤ b < 7																	
Operation:	skip if (f<b>) = 1																	
Status Affected:	None																	
Encoding:	<table border="1"><tr><td>0111</td><td>bbbf</td><td>ffff</td></tr></table>			0111	bbbf	ffff												
0111	bbbf	ffff																
Description:	If bit 'b' in register 'f' is '1' then the next instruction is skipped. If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and an NOP is executed instead, making this a 2 cycle instruction.																	
Words:	1																	
Cycles:	1(2)																	
Example:	<table><tr><td>HERE</td><td>BTFSS</td><td>FLAG,1</td></tr><tr><td>FALSE</td><td>GOTO</td><td>PROCESS_CODE</td></tr><tr><td>TRUE</td><td></td><td></td></tr><tr><td></td><td>•</td><td></td></tr><tr><td></td><td>•</td><td></td></tr></table>			HERE	BTFSS	FLAG,1	FALSE	GOTO	PROCESS_CODE	TRUE				•			•	
HERE	BTFSS	FLAG,1																
FALSE	GOTO	PROCESS_CODE																
TRUE																		
	•																	
	•																	
Before Instruction																		
PC	=	address ( HERE )																
After Instruction																		
If FLAG<1>	=	0,																
PC	=	address ( FALSE );																
if FLAG<1>	=	1,																
PC	=	address ( TRUE )																

## CALL Subroutine Call

**Syntax:** [ *label* ] CALL *k*

**Operands:**  $0 \leq k \leq 255$

**Operation:** (PC) + 1  $\rightarrow$  Top of Stack;  
 $k \rightarrow PC<7:0>$ ;  
 (STATUS<6:5>)  $\rightarrow PC<10:9>$ ;  
 $0 \rightarrow PC<8>$

**Status Affected:** None

**Encoding:**

1001	kkkk	kkkk
------	------	------

**Description:** Subroutine call. First, return address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two cycle instruction.

**Words:** 1

**Cycles:** 2

**Example:** HERE CALL THERE

Before Instruction  
 PC = address (HERE)

After Instruction  
 PC = address (THERE)  
 TOS = address (HERE + 1)

## CLRF Clear f

**Syntax:** [ *label* ] CLRF *f*

**Operands:**  $0 \leq f \leq 31$

**Operation:**  $00h \rightarrow (f)$ ;  
 $1 \rightarrow Z$

**Status Affected:** Z

**Encoding:**

0000	011f	ffff
------	------	------

**Description:** The contents of register 'f' are cleared and the Z bit is set.

**Words:** 1

**Cycles:** 1

**Example:** CLRF FLAG\_REG

Before Instruction  
 FLAG\_REG = 0x5A

After Instruction  
 FLAG\_REG = 0x00  
 Z = 1

## CLRW Clear W

**Syntax:** [ *label* ] CLRW

**Operands:** None

**Operation:**  $00h \rightarrow (W)$ ;  
 $1 \rightarrow Z$

**Status Affected:** Z

**Encoding:**

0000	0100	0000
------	------	------

**Description:** The W register is cleared. Zero bit (Z) is set.

**Words:** 1

**Cycles:** 1

**Example:** CLRW

Before Instruction  
 W = 0x5A

After Instruction  
 W = 0x00  
 Z = 1

## CLRWDTClear Watchdog Timer

**Syntax:** [ *label* ] CLRWDTClear Watchdog Timer

**Operands:** None

**Operation:**  $00h \rightarrow WDT$ ;  
 $0 \rightarrow WDT$  prescaler (if assigned);  
 $1 \rightarrow \overline{TO}$ ;  
 $1 \rightarrow \overline{PD}$

**Status Affected:**  $\overline{TO}$ ,  $\overline{PD}$

**Encoding:**

0000	0000	0100
------	------	------

**Description:** The CLRWDTClear Watchdog Timer instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits  $\overline{TO}$  and  $\overline{PD}$  are set.

**Words:** 1

**Cycles:** 1

**Example:** CLRWDTClear Watchdog Timer

Before Instruction  
 WDT counter = ?

After Instruction  
 WDT counter = 0x00  
 WDT prescale = 0  
 $\overline{TO}$  = 1  
 $\overline{PD}$  = 1

## 10.6 SIMICE Entry-Level Hardware Simulator

SIMICE is an entry-level hardware development system designed to operate in a PC-based environment with Microchip's simulator MPLAB™-SIM. Both SIMICE and MPLAB-SIM run under Microchip Technology's MPLAB Integrated Development Environment (IDE) software. Specifically, SIMICE provides hardware simulation for Microchip's PIC12C5XX, PIC12CE5XX, and PIC16C5X families of PICmicro® 8-bit microcontrollers. SIMICE works in conjunction with MPLAB-SIM to provide non-real-time I/O port emulation. SIMICE enables a developer to run simulator code for driving the target system. In addition, the target system can provide input to the simulator code. This capability allows for simple and interactive debugging without having to manually generate MPLAB-SIM stimulus files. SIMICE is a valuable debugging tool for entry-level system development.

## 10.7 PICDEM-1 Low-Cost PICmicro® Demonstration Board

The PICDEM-1 is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The users can program the sample microcontrollers provided with the PICDEM-1 board, on a PRO MATE II or PICSTART-Plus programmer, and easily test firmware. The user can also connect the PICDEM-1 board to the MPLAB-ICE emulator and download the firmware to the emulator for testing. Additional prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push-button switches and eight LEDs connected to PORTB.

## 10.8 PICDEM-2 Low-Cost PIC16CXX Demonstration Board

The PICDEM-2 is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-2 board, on a PRO MATE II programmer or PICSTART-Plus, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-2 board to test firmware. Additional prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push-button switches, a potentiometer for simulated analog input, a Serial EEPROM to demonstrate usage of the I<sup>2</sup>C bus and separate headers for connection to an LCD module and a keypad.

## 10.9 PICDEM-3 Low-Cost PIC16CXXX Demonstration Board

The PICDEM-3 is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with a LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-3 board, on a PRO MATE II programmer or PICSTART Plus with an adapter socket, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-3 board to test firmware. Additional prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include an RS-232 interface, push-button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM-3 board is an LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM-3 provides an additional RS-232 interface and Windows 3.1 software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

## 11.1 DC CHARACTERISTICS: PIC12C508/509 (Commercial, Industrial, Extended)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)					
Parm No.	Characteristic	Sym	Min	Typ <sup>(1)</sup>	Max	Units	Conditions
D001	Supply Voltage	VDD	2.5 3.0		5.5 5.5	V V	FOSC = DC to 4 MHz (Commercial/ Industrial) FOSC = DC to 4 MHz (Extended)
D002	RAM Data Retention Voltage <sup>(2)</sup>	VDR		1.5*		V	Device in SLEEP mode
D003	VDD Start Voltage to ensure Power-on Reset	VPOR		VSS		V	See section on Power-on Reset for details
D004	VDD Rise Rate to ensure Power-on Reset	SVDD	0.05 *			V/ms	See section on Power-on Reset for details
D010 D010C D010A	Supply Current <sup>(3)</sup>	IDD	—	.78 1.1 10 14 14	2.4 2.4 27 35 35	mA mA $\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$	XT and EXTRC options <sup>(4)</sup> FOSC = 4 MHz, VDD = 5.5V INTRC Option FOSC = 4 MHz, VDD = 5.5V LP OPTION, Commercial Temperature FOSC = 32 kHz, VDD = 3.0V, WDT disabled LP OPTION, Industrial Temperature FOSC = 32 kHz, VDD = 3.0V, WDT disabled LP OPTION, Extended Temperature FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D020 D021 D021B	Power-Down Current <sup>(5)</sup>	IPD	— — —	0.25 0.25 2	4 5 18	$\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$	VDD = 3.0V, Commercial WDT disabled VDD = 3.0V, Industrial WDT disabled VDD = 3.0V, Extended WDT disabled
D022		$\Delta\text{IWDT}$	— — —	3.75 3.75 3.75	8 9 14	$\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$	VDD = 3.0V, Commercial VDD = 3.0V, Industrial VDD = 3.0V, Extended

\* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

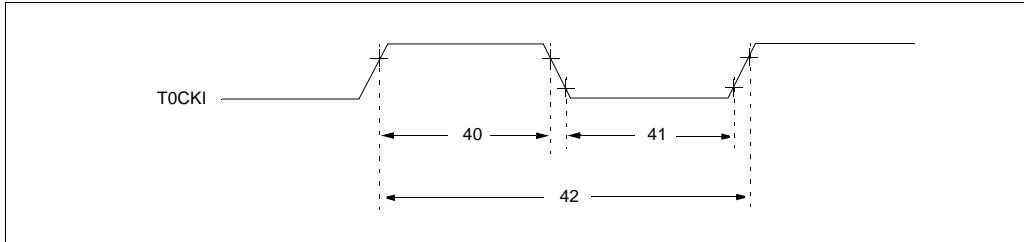
b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula:  $I_R = V_{DD}/2R_{ext}$  (mA) with Rext in kOhm.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

# PIC12C5XX

**FIGURE 11-5: TIMER0 CLOCK TIMINGS - PIC12C508/C509**



**TABLE 11-7: TIMER0 CLOCK REQUIREMENTS - PIC12C508/C509**

AC Characteristics			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) Operating Voltage $V_{DD}$ range is described in Section 11.1.				
Parameter No.	Sym	Characteristic	Min	Typ <sup>(1)</sup>	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	$0.5 T_{CY} + 20^*$	—	—	ns	
		- With Prescaler	$10^*$	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	$0.5 T_{CY} + 20^*$	—	—	ns	
		- With Prescaler	$10^*$	—	—	ns	
42	Tt0P	T0CKI Period	$20 \text{ or } \frac{T_{CY} + 40^*}{N}$	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

\* These parameters are characterized but not tested.

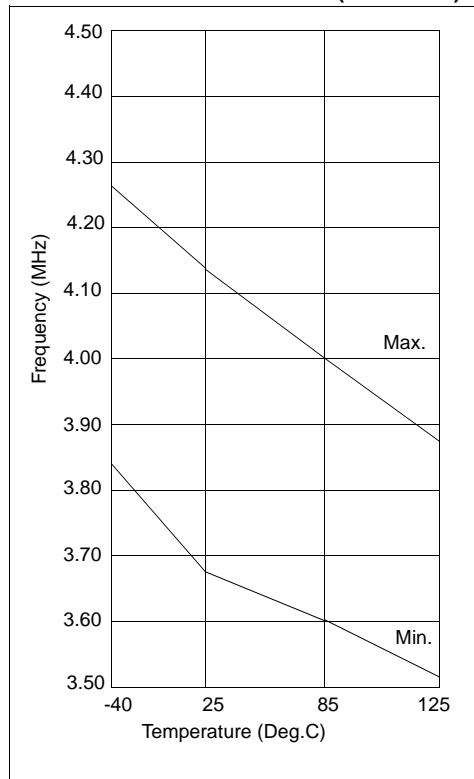
Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

## 12.0 DC AND AC CHARACTERISTICS - PIC12C508/PIC12C509

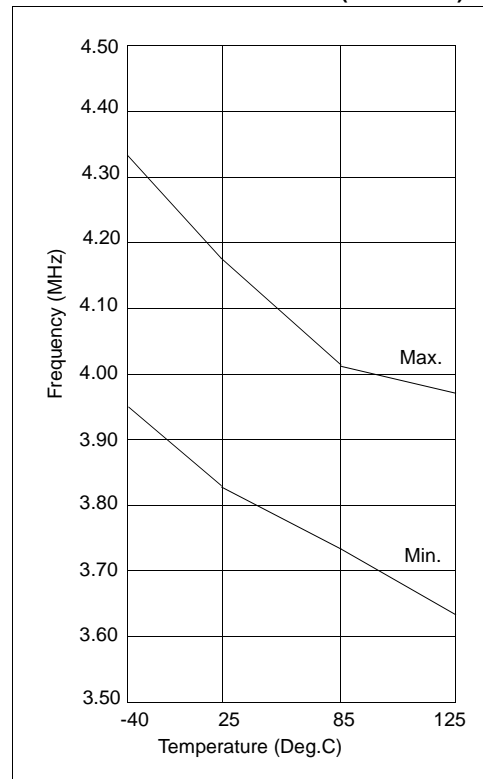
The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3 $\sigma$ ) and (mean - 3 $\sigma$ ) respectively, where  $\sigma$  is standard deviation.

**FIGURE 12-1: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE (VDD = 2.5V)**



**FIGURE 12-2: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE (VDD = 5.0V)**



## 13.1 DC CHARACTERISTICS: PIC12C508A/509A (Commercial, Industrial, Extended) PIC12CE518/519 (Commercial, Industrial, Extended) PIC12CR509A (Commercial, Industrial, Extended)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature      0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended)					
Parm No.	Characteristic	Sym	Min	Typ <sup>(1)</sup>	Max	Units	Conditions
D001	Supply Voltage	VDD	3.0		5.5	V	FOSC = DC to 4 MHz (Commercial/ Industrial, Extended)
D002	RAM Data Retention Voltage <sup>(2)</sup>	VDR		1.5*		V	Device in SLEEP mode
D003	VDD Start Voltage to ensure Power-on Reset	VPOR		VSS		V	See section on Power-on Reset for details
D004	VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See section on Power-on Reset for details
D010	Supply Current <sup>(3)</sup>	IDD	—	0.8	1.4	mA	XT and EXTRC options (Note 4) FOSC = 4 MHz, VDD = 5.5V
D010C			—	0.8	1.4	mA	INTRC Option FOSC = 4 MHz, VDD = 5.5V
D010A			—	19	27	μA	LP OPTION, Commercial Temperature FOSC = 32 kHz, VDD = 3.0V, WDT disabled
			—	19	35	μA	LP OPTION, Industrial Temperature FOSC = 32 kHz, VDD = 3.0V, WDT disabled
			—	30	55	μA	LP OPTION, Extended Temperature FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D020 D021 D021B	Power-Down Current <sup>(5)</sup>	IPD	—	0.25	4	μA	VDD = 3.0V, Commercial WDT disabled
—			0.25	5	μA	VDD = 3.0V, Industrial WDT disabled	
—			2	12	μA	VDD = 3.0V, Extended WDT disabled	
D022	Power-Down Current	ΔIWDT	—	2.2	5	μA	VDD = 3.0V, Commercial
—			2.2	6	μA	VDD = 3.0V, Industrial	
—			4	11	μA	VDD = 3.0V, Extended	
	Supply Current <sup>(3)</sup> During read/write to EEPROM peripheral	ΔIEE	—	0.1	0.2	mA	FOSC = 4 MHz, Vdd = 5.5V, SCL = 400kHz

\* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
- 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
  - a) The test conditions for all IDD measurements in active operation mode are:  
OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
  - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
- 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kOhm.
- 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

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**TABLE 13-1: PULL-UP RESISTOR RANGES\* - PIC12C508A, PIC12C509A, PIC12CR509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519**

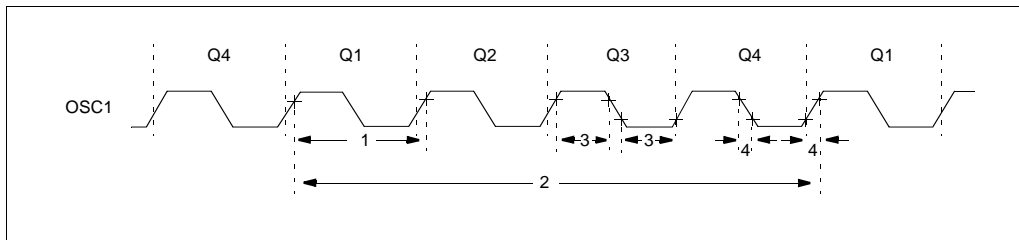
V <sub>DD</sub> (Volts)	Temperature (°C)	Min	Typ	Max	Units
GP0/GP1					
2.5	–40	38K	42K	63K	Ω
	25	42K	48K	63K	Ω
	85	42K	49K	63K	Ω
	125	50K	55K	63K	Ω
5.5	–40	15K	17K	20K	Ω
	25	18K	20K	23K	Ω
	85	19K	22K	25K	Ω
	125	22K	24K	28K	Ω
GP3					
2.5	–40	285K	346K	417K	Ω
	25	343K	414K	532K	Ω
	85	368K	457K	532K	Ω
	125	431K	504K	593K	Ω
5.5	–40	247K	292K	360K	Ω
	25	288K	341K	437K	Ω
	85	306K	371K	448K	Ω
	125	351K	407K	500K	Ω

\* These parameters are characterized but not tested.



## 13.6 Timing Diagrams and Specifications

**FIGURE 13-2: EXTERNAL CLOCK TIMING - PIC12C508A, PIC12C509A, PIC12CR509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519**



**TABLE 13-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519**

<b>AC Characteristics</b> <b>Standard Operating Conditions (unless otherwise specified)</b> Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial), $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial), $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) Operating Voltage $V_{DD}$ range is described in Section 13.1							
Parameter No.	Sym	Characteristic	Min	Typ <sup>(1)</sup>	Max	Units	Conditions
	Fosc	External CLKIN Frequency <sup>(2)</sup>	DC	—	4	MHz	XT osc mode
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency <sup>(2)</sup>	DC	—	4	MHz	EXTRC osc mode
			0.1	—	4	MHz	XT osc mode
1	Tosc	External CLKIN Period <sup>(2)</sup>	DC	—	200	kHz	LP osc mode
			250	—	—	ns	XT osc mode
		Oscillator Period <sup>(2)</sup>	5	—	—	ms	LP osc mode
			250	—	—	ns	EXTRC osc mode
2	Tcy	Instruction Cycle Time <sup>(3)</sup>	250	—	10,000	ns	XT osc mode
			5	—	—	ms	LP osc mode
3	TosL, TosH	Clock in (OSC1) Low or High Time	—	—	—	ns	XT oscillator
			50*	—	—	ms	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	2*	—	—	ns	XT oscillator
			—	—	25*	ns	LP oscillator
			—	—	50*	ns	LP oscillator

\* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (Tcy) equals four times the input oscillator time base period.

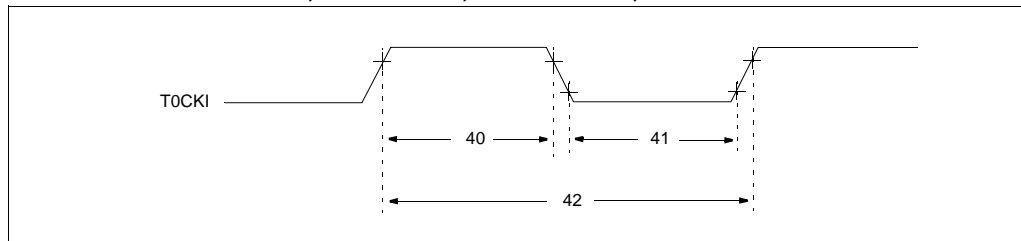
# PIC12C5XX

**TABLE 13-6: DRT (DEVICE RESET TIMER PERIOD) - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519**

Oscillator Configuration	POR Reset	Subsequent Resets
IntRC & ExtRC	18 ms (typical) <sup>(1)</sup>	300 $\mu$ s (typical) <sup>(1)</sup>
XT & LP	18 ms (typical) <sup>(1)</sup>	18 ms (typical) <sup>(1)</sup>

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 13-5: TIMER0 CLOCK TIMINGS - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519**



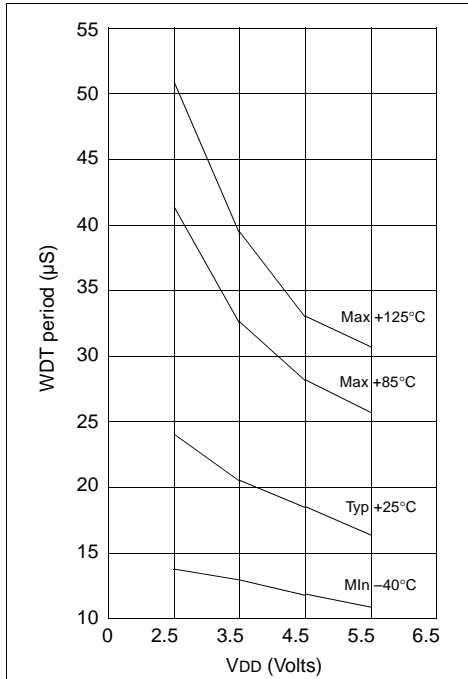
**TABLE 13-7: TIMER0 CLOCK REQUIREMENTS - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519**

AC Characteristics			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended)				
			Operating Voltage VDD range is described in Section 13.1.				
Parameter No.	Sym	Characteristic	Min	Typ <sup>(1)</sup>	Max	Units	Conditions
40	Ti0H	T0CKI High Pulse Width - No Prescaler	0.5 Tcy + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Ti0L	T0CKI Low Pulse Width - No Prescaler	0.5 Tcy + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Ti0P	T0CKI Period	20 or $\frac{Tcy + 40}{N}$	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

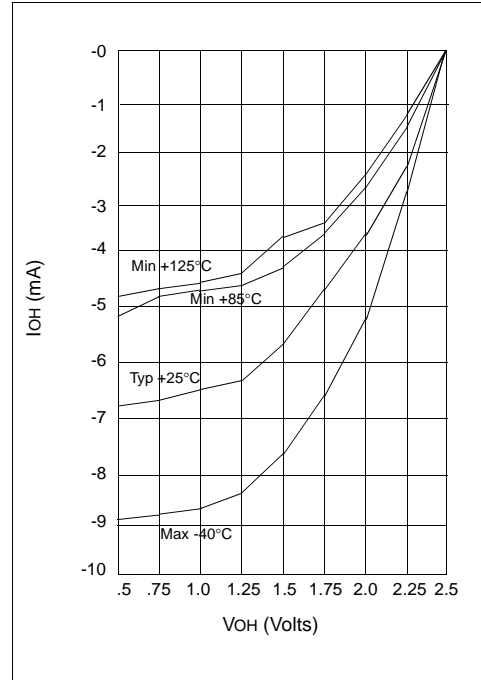
\* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

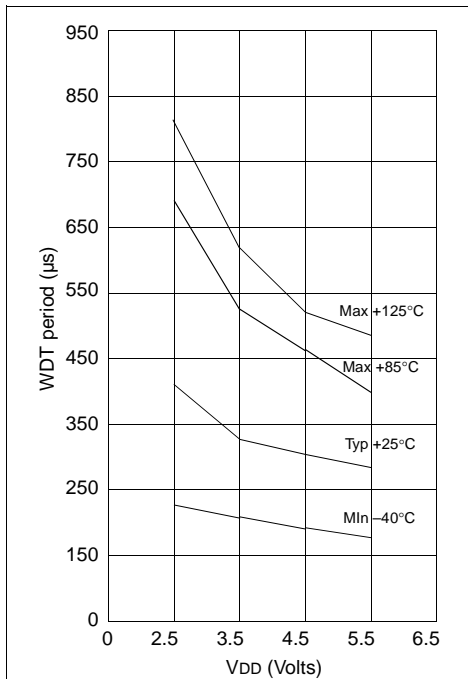
**FIGURE 14-5: WDT TIMER TIME-OUT PERIOD vs.  $V_{DD}$**



**FIGURE 14-7:  $I_{OH}$  vs.  $V_{OH}$ ,  $V_{DD} = 2.5$  V**



**FIGURE 14-6: SHORT DRT PERIOD VS.  $V_{DD}$**



**FIGURE 14-8:  $I_{OH}$  vs.  $V_{OH}$ ,  $V_{DD} = 3.5$  V**

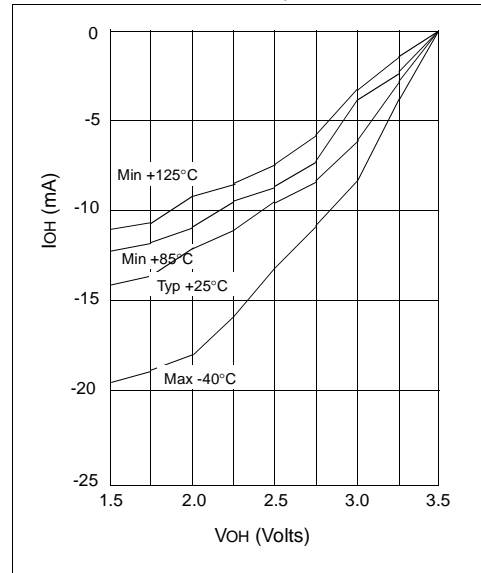
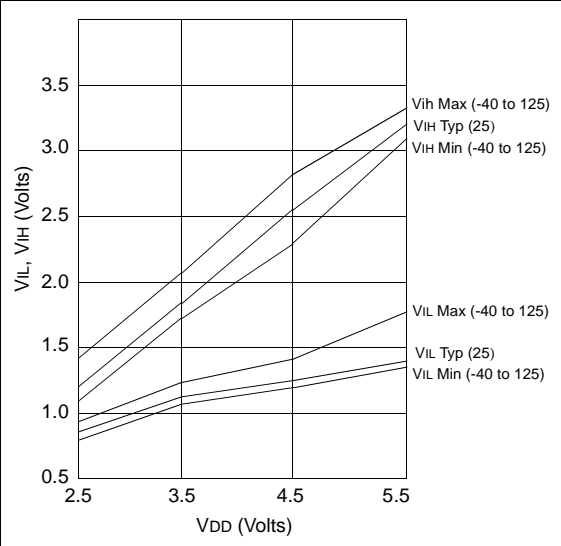


FIGURE 14-15: VIL, VIH OF NMCLR, AND T0CKI VS. VDD





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