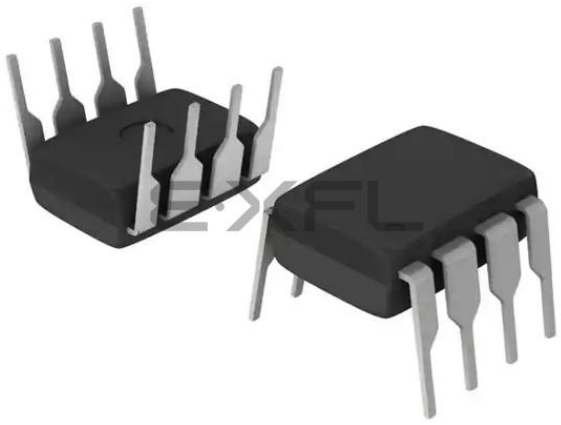

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 5 |
| Program Memory Size | 1.5KB (1K x 12) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 41 x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 8-DIP (0.300", 7.62mm) |
| Supplier Device Package | 8-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic12c509-04e-p |

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- Fill out and mail in the reader response form in the back of this data sheet.
- E-mail us at webmaster@microchip.com.

We appreciate your assistance in making this a better document.

**NOTES:**

### 4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1).

The special registers can be classified into two sets. The special function registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

**TABLE 4-1: SPECIAL FUNCTION REGISTER (SFR) SUMMARY**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-On Reset | Value on All Other Resets(2) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| N/A | TRIS | — | — | | | | | | | --11 1111 | --11 1111 |
| N/A | OPTION | Contains control bits to configure Timer0, Timer0/WDT prescaler, wake-up on change, and weak pull-ups | | | | | | | | 1111 1111 | 1111 1111 |
| 00h | INDF | Uses contents of FSR to address data memory (not a physical register) | | | | | | | | xxxx xxxx | uuuu uuuu |
| 01h | TMR0 | 8-bit real-time clock/counter | | | | | | | | xxxx xxxx | uuuu uuuu |
| 02h(1) | PCL | Low order 8 bits of PC | | | | | | | | 1111 1111 | 1111 1111 |
| 03h | STATUS | GPWUF | — | PA0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C | 0001 1xxx | q00q quuu(3) |
| 04h | FSR (PIC12C508/ PIC12C508A/ PIC12C518) | Indirect data memory address pointer | | | | | | | | 111x xxxx | 111u uuuu |
| 04h | FSR (PIC12C509/ PIC12C509A/ PIC12CR509A/ PIC12CE519) | Indirect data memory address pointer | | | | | | | | 110x xxxx | 11uu uuuu |
| 05h | OSCCAL (PIC12C508/ PIC12C509) | CAL3 | CAL2 | CAL1 | CAL0 | — | — | — | — | 0111 ---- | uuuu ---- |
| 05h | OSCCAL (PIC12C508A/ PIC12C509A/ PIC12CE518/ PIC12CE519/ PIC12CR509A) | CAL5 | CAL4 | CAL3 | CAL2 | CAL1 | CAL0 | — | — | 1000 00-- | uuuu uu-- |
| 06h | GPIO (PIC12C508/ PIC12C509/ PIC12C508A/ PIC12C509A/ PIC12CR509A) | — | — | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | --xx xxxx | --uu uuuu |
| 06h | GPIO (PIC12CE518/ PIC12CE519) | SCL | SDA | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | 11xx xxxx | 11uu uuuu |

Legend: Shaded boxes = unimplemented or unused, – = unimplemented, read as '0' (if applicable)
x = unknown, u = unchanged, q = see the tables in Section 8.7 for possible values.

Note 1: The upper byte of the Program Counter is not directly accessible. See Section 4.6 for an explanation of how to access these bits.

2: Other (non power-up) resets include external reset through $\overline{MCLR}$, watchdog timer and wake-up on pin change reset.

3: If reset was due to wake-up on pin change then bit 7 = 1. All other resets will cause bit 7 = 0.

### 4.4 OPTION Register

The OPTION register is a 8-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the `OPTION` instruction, the contents of the W register will be transferred to the OPTION register. A RESET sets the OPTION<7:0> bits.

| | |
|---|---|
| **Note:** | If TRIS bit is set to '0', the wake-up on change and pull-up functions are disabled for that pin; i.e., note that TRIS overrides OPTION control of $\overline{\text{GPPU}}$ and $\overline{\text{GPWU}}$. |
| **Note:** | If the T0CS bit is set to '1', GP2 is forced to be an input even if TRIS GP2 = '0'. |

**FIGURE 4-5: OPTION REGISTER**

| W-1 | W-1 | W-1 | W-1 | W-1 | W-1 | W-1 | W-1 |
|---|---|---|---|---|---|---|---|
| $\overline{\text{GPWU}}$ | $\overline{\text{GPPU}}$ | T0CS | T0SE | PSA | PS2 | PS1 | PS0 |
| bit7 | 6 | 5 | 4 | 3 | 2 | 1 | bit0 |

W = Writable bit
U = Unimplemented bit
- n = Value at POR reset
Reference Table 4-1 for other resets.

bit 7: **$\overline{\text{GPWU}}$:** Enable wake-up on pin change (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 6: **$\overline{\text{GPPU}}$**: Enable weak pull-ups (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 5: **T0CS**: Timer0 clock source select bit
1 = Transition on T0CKI pin
0 = Transition on internal instruction cycle clock, Fosc/4

bit 4: **T0SE**: Timer0 source edge select bit
1 = Increment on high to low transition on the T0CKI pin
0 = Increment on low to high transition on the T0CKI pin

bit 3: **PSA**: Prescaler assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0: **PS2:PS0**: Prescaler rate select bits

| Bit Value | Timer0 Rate | WDT Rate |
|---|---|---|
| 000 | 1 : 2 | 1 : 1 |
| 001 | 1 : 4 | 1 : 2 |
| 010 | 1 : 8 | 1 : 4 |
| 011 | 1 : 16 | 1 : 8 |
| 100 | 1 : 32 | 1 : 16 |
| 101 | 1 : 64 | 1 : 32 |
| 110 | 1 : 128 | 1 : 64 |
| 111 | 1 : 256 | 1 : 128 |

## 4.6 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

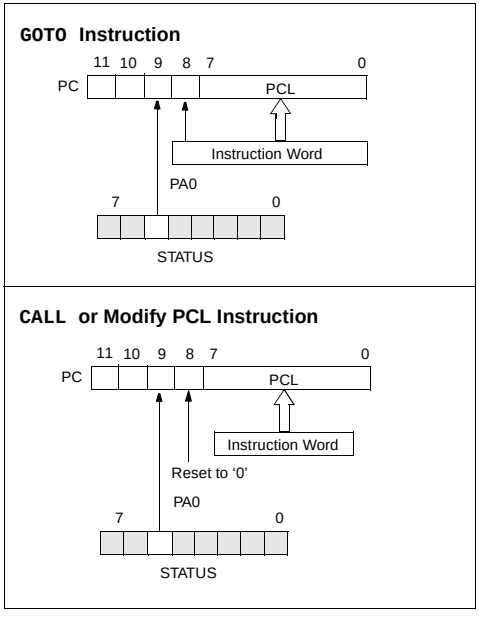
For a GOTO instruction, bits 8:0 of the PC are provided by the GOTO instruction word. The PC Latch (PCL) is mapped to PC<7:0>. Bit 5 of the STATUS register provides page information to bit 9 of the PC (Figure 4-8).

For a CALL instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-8).

Instructions where the PCL is the destination, or Modify PCL instructions, include MOVWF PC, ADDWF PC, and BSF PC,5.

| | |
|---|---|
| **Note:** | Because PC<8> is cleared in the CALL instruction, or any Modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long). |

**FIGURE 4-8: LOADING OF PC BRANCH INSTRUCTIONS - PIC12C5XX**




### 4.6.1 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page i.e., the oscillator calibration instruction. After executing MOVLW XX, the PC will roll over to location 00h, and begin executing user code.

The STATUS register page preselect bits are cleared upon a RESET, which means that page 0 is preselected.

Therefore, upon a RESET, a GOTO instruction will automatically cause the program to jump to page 0 until the value of the page bits is altered.

## 4.7 Stack

PIC12C5XX devices have a 12-bit wide L.I.F.O. hardware push/pop stack.

A CALL instruction will *push* the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential CALL's are executed, only the most recent two return addresses are stored.

A RETLW instruction will *pop* the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential RETLW's are executed, the stack will be filled with the address previously stored in level 2. Note that the W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

Upon any reset, the contents of the stack remain unchanged, however the program counter (PCL) will also be reset to 0.

| | |
|---|---|
| **Note 1:** | There are no STATUS bits to indicate stack overflows or stack underflow conditions. |
| **Note 2:** | There are no instructions mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL and RETLW instructions. |

**TABLE 5-1: SUMMARY OF PORT REGISTERS**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-On Reset | Value on All Other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| N/A | TRIS | — | — | | | | | | | --11 1111 | --11 1111 |
| N/A | OPTION | $\overline{GPWU}$ | $\overline{GPPU}$ | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| 03H | STATUS | GPWUF | — | PAO | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C | 0001 1xxx | q00q quuu(1) |
| 06h | GPIO (PIC12C508/ PIC12C509/ PIC12C508A/ PIC12C509A/ PIC12CR509A) | — | — | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | --xx xxxx | --uu uuuu |
| 06h | GPIO (PIC12CE518/ PIC12CE519) | SCL | SDA | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | 11xx xxxx | 11uu uuuu |

Legend: Shaded cells not used by Port Registers, read as '0', — = unimplemented, read as '0', x = unknown, u = unchanged, q = see tables in Section 8.7 for possible values.

Note 1: If reset was due to wake-up on change, then bit 7 = 1. All other resets will cause bit 7 = 0.

## 5.4 I/O Programming Considerations

### 5.4.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of GPIO will cause all eight bits of GPIO to be read into the CPU, bit5 to be set and the GPIO value to be written to the output latches. If another bit of GPIO is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

**EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT**

```
;Initial GPIO Settings
; GPIO<5:3> Inputs
; GPIO<2:0> Outputs
;
;                    GPIO latch  GPIO pins
;                    ----------  ----------
  BCF   GPIO, 5    ;--01 -ppp   --11 pppp
  BCF   GPIO, 4    ;--10 -ppp   --11 pppp
  MOVLW 007h        ;
  TRIS  GPIO       ;--10 -ppp   --11 pppp
;
;Note that the user may have expected the pin
;values to be --00 pppp. The 2nd BCF caused
;GP5 to be latched as the pin value (High).
```

### 5.4.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

**FIGURE 7-3: DATA TRANSFER SEQUENCE ON THE SERIAL BUS**

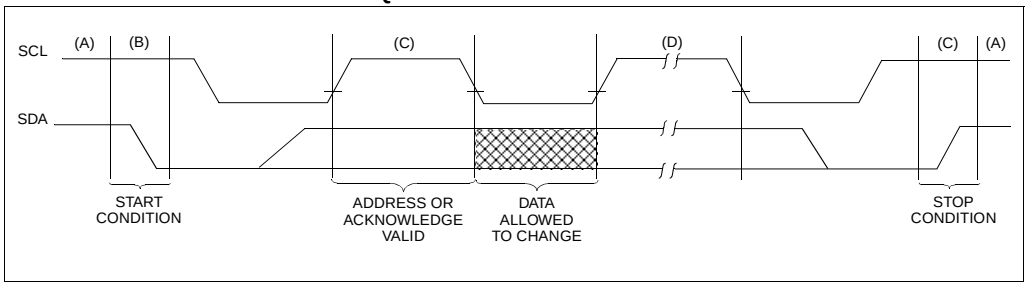
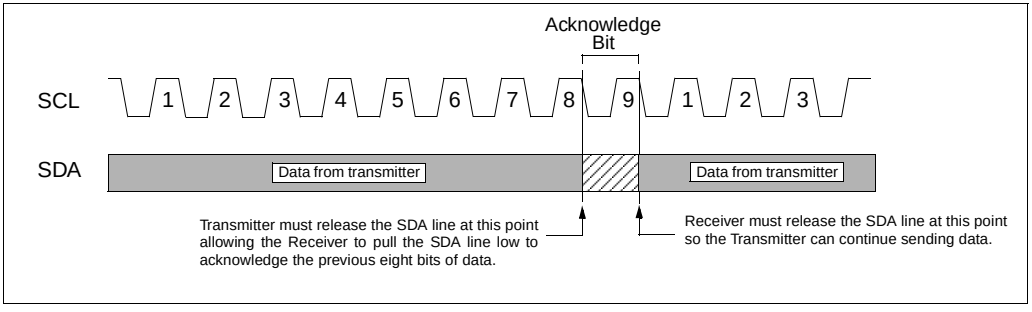



**FIGURE 7-4: ACKNOWLEDGE TIMING**

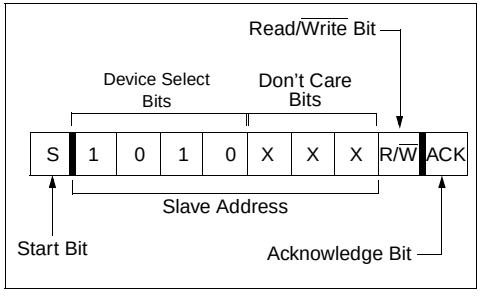



## 7.2 Device Addressing

After generating a START condition, the bus master transmits a control byte consisting of a slave address and a Read/$\overline{\text{Write}}$ bit that indicates what type of operation is to be performed. The slave address consists of a 4-bit device code (1010) followed by three don't care bits.

The last bit of the control byte determines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. (Figure 7-5). The bus is monitored for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

**FIGURE 7-5: CONTROL BYTE FORMAT**



## 8.2 Oscillator Configurations

### 8.2.1 OSCILLATOR TYPES

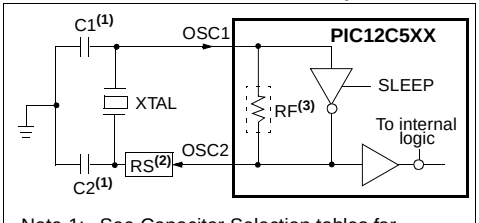
The PIC12C5XX can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

- LP: Low Power Crystal
- XT: Crystal/Resonator
- INTRC: Internal 4 MHz Oscillator
- EXTRC: External Resistor/Capacitor

### 8.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT or LP modes, a crystal or ceramic resonator is connected to the GP5/OSC1/CLKIN and GP4/OSC2 pins to establish oscillation (Figure 8-2). The PIC12C5XX oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT or LP modes, the device can have an external clock source drive the GP5/OSC1/CLKIN pin (Figure 8-3).

**FIGURE 8-2: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (XT OR LP OSC CONFIGURATION)**




Note 1: See Capacitor Selection tables for recommended values of C1 and C2.
2: A series resistor (RS) may be required for AT strip cut crystals.
3: RF approximate value = 10 MΩ.

**FIGURE 8-3: EXTERNAL CLOCK INPUT OPERATION (XT OR LP OSC CONFIGURATION)**

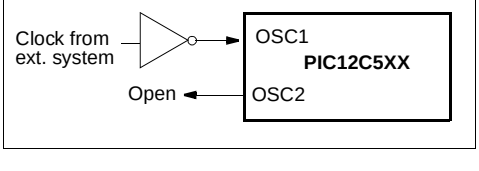



**TABLE 8-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS - PIC12C5XX**

| Osc Type | Resonator Freq | Cap. Range C1 | Cap. Range C2 |
|---|---|---|---|
| XT | 4.0 MHz | 30 pF | 30 pF |

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

**TABLE 8-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - PIC12C5XX**

| Osc Type | Resonator Freq | Cap.Range C1 | Cap. Range C2 |
|---|---|---|---|
| LP | 32 kHz(1) | 15 pF | 15 pF |
| XT | 200 kHz | 47-68 pF | 47-68 pF |
| | 1 MHz | 15 pF | 15 pF |
| | 4 MHz | 15 pF | 15 pF |

Note 1: For $V_{DD}$ > 4.5V, C1 = C2 ≈ 30 pF is recommended.

These values are for design guidance only. Rs may be required to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

### 8.7 Time-Out Sequence, Power Down, and Wake-up from SLEEP Status Bits (TO/PD/GPWUF)

The $\overline{TO}$, $\overline{PD}$, and GPWUF bits in the STATUS register can be tested to determine if a RESET condition has been caused by a power-up condition, a $\overline{MCLR}$ or Watchdog Timer (WDT) reset.

**TABLE 8-7: $\overline{TO}$/$\overline{PD}$/GPWUF STATUS AFTER RESET**

| GPWUF | $\overline{TO}$ | $\overline{PD}$ | RESET caused by |
|---|---|---|---|
| 0 | 0 | 0 | WDT wake-up from SLEEP |
| 0 | 0 | u | WDT time-out (not from SLEEP) |
| 0 | 1 | 0 | $\overline{MCLR}$ wake-up from SLEEP |
| 0 | 1 | 1 | Power-up |
| 0 | u | u | $\overline{MCLR}$ not during SLEEP |
| 1 | 1 | 0 | Wake-up from SLEEP on pin change |

Legend: u = unchanged

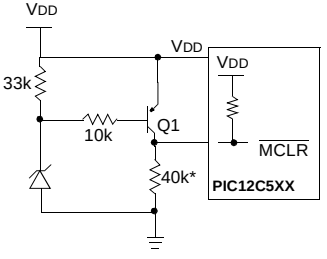
Note 1: The $\overline{TO}$, $\overline{PD}$, and GPWUF bits maintain their status (u) until a reset occurs. A low-pulse on the $\overline{MCLR}$ input does not change the $\overline{TO}$, $\overline{PD}$, and GPWUF status bits.

### 8.8 Reset on Brown-Out

A brown-out is a condition where device power ($V_{DD}$) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

To reset PIC12C5XX devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 8-13 , Figure 8-14 and Figure 8-15

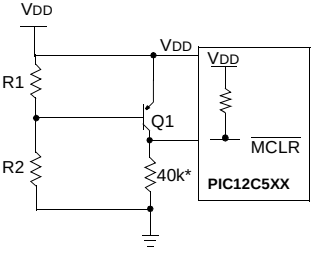
**FIGURE 8-13: BROWN-OUT PROTECTION CIRCUIT 1**




This circuit will activate reset when $V_{DD}$ goes below Vz + 0.7V (where Vz = Zener voltage).

*Refer to Figure 8-7 and Table 11-1 for internal weak pull-up on $\overline{MCLR}$.

**FIGURE 8-14: BROWN-OUT PROTECTION CIRCUIT 2**

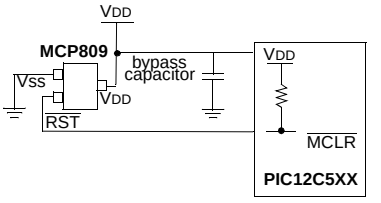



This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when $V_{DD}$ is below a certain level such that:

$$V_{DD} \bullet \frac{R1}{R1 + R2} = 0.7V$$

*Refer to Figure 8-7 and Table 11-1 for internal weak pull-up on $\overline{MCLR}$.

**FIGURE 8-15: BROWN-OUT PROTECTION CIRCUIT 3**




This brown-out protection circuit employs Microchip Technology's MCP809 microcontroller supervisor. The MCP8XX and MCP1XX family of supervisors provide push-pull and open collector outputs with both high and low active reset pins. There are 7 different trip point selections to accomodate 5V and 3V systems.

## 8.9 Power-Down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

### 8.9.1 SLEEP

The Power-Down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{TO}$ bit (STATUS<4>) is set, the $\overline{PD}$ bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low, or hi-impedance).

It should be noted that a RESET generated by a WDT time-out does not drive the $\overline{MCLR}$ pin low.

For lowest current consumption while powered down, the T0CKI input should be at $V_{DD}$ or $V_{SS}$ and the GP3/$\overline{MCLR}$/$V_{PP}$ pin must be at a logic high level ($V_{IHMC}$) if $\overline{MCLR}$ is enabled.

### 8.9.2 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

1. An external reset input on GP3/$\overline{MCLR}$/$V_{PP}$ pin, when configured as $\overline{MCLR}$.
2. A Watchdog Timer time-out reset (if WDT was enabled).
3. A change on input pin GP0, GP1, or GP3/$\overline{MCLR}$/$V_{PP}$ when wake-up on change is enabled.

These events cause a device reset. The $\overline{TO}$, $\overline{PD}$, and GPWUF bits can be used to determine the cause of device reset. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up). The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked. The GPWUF bit indicates a change in state while in SLEEP at pins GP0, GP1, or GP3 (since the last time there was a file or bit operation on GP port).

| | |
|---|---|
| **Caution:** | Right before entering SLEEP, read the input pins. When in SLEEP, wake up occurs when the values at the pins change from the state they were in at the last reading. If a wake-up on change occurs and the pins are not read before reentering SLEEP, a wake up will occur immediately even if no pins change while in SLEEP mode. |

The WDT is cleared when the device wakes from sleep, regardless of the wake-up source.

## 8.10 Program Verification/Code Protection

If the code protection bit has not been programmed, the on-chip program memory can be read out for verification purposes.

The first 64 locations can be read by the PIC12C5XX regardless of the code protection bit setting.

The last memory location cannot be read if code protection is enabled on the PIC12C508/509.

The last memory location can be read regardless of the code protection bit setting on the PIC12C508A/509A/CR509A/CE518/CE519.

## 8.11 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '0's.

**CALL** **Subroutine Call**

Syntax: [ *label* ] CALL k

Operands: 0 ≤ k ≤ 255

Operation: (PC) + 1→ Top of Stack;
k → PC<7:0>;
(STATUS<6:5>) → PC<10:9>;
0 → PC<8>

Status Affected: None

Encoding:

| 1001 | kkkk | kkkk |
|---|---|---|

Description: Subroutine call. First, return address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two cycle instruction.

Words: 1

Cycles: 2

Example:
```
HERE    CALL    THERE
```
Before Instruction
PC = address (HERE)
After Instruction
PC = address (THERE)
TOS = address (HERE + 1)

**CLRF** **Clear f**

Syntax: [ *label* ] CLRF f

Operands: 0 ≤ f ≤ 31

Operation: 00h → (f);
1 → Z

Status Affected: Z

Encoding:

| 0000 | 011f | ffff |
|---|---|---|

Description: The contents of register 'f' are cleared and the Z bit is set.

Words: 1

Cycles: 1

Example:
```
CLRF    FLAG_REG
```
Before Instruction
FLAG_REG = 0x5A
After Instruction
FLAG_REG = 0x00
Z = 1

**CLRW** **Clear W**

Syntax: [ *label* ] CLRW

Operands: None

Operation: 00h → (W);
1 → Z

Status Affected: Z

Encoding:

| 0000 | 0100 | 0000 |
|---|---|---|

Description: The W register is cleared. Zero bit (Z) is set.

Words: 1

Cycles: 1

Example:
```
CLRW
```
Before Instruction
W = 0x5A
After Instruction
W = 0x00
Z = 1

**CLRWDT** **Clear Watchdog Timer**

Syntax: [ *label* ] CLRWDT

Operands: None

Operation: 00h → WDT;
0 → WDT prescaler (if assigned);
1 → $\overline{TO}$;
1 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

| 0000 | 0000 | 0100 |
|---|---|---|

Description: The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

Words: 1

Cycles: 1

Example:
```
CLRWDT
```
Before Instruction
WDT counter = ?
After Instruction
WDT counter = 0x00
WDT prescale = 0
$\overline{TO}$ = 1
$\overline{PD}$ = 1

### 10.10 MPLAB Integrated Development Environment Software

The MPLAB IDE Software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a windows based application which contains:

- A full featured editor
- Three operating modes
  - editor
  - emulator
  - simulator
- A project manager
- Customizable tool bar and key mapping
- A status bar with project information
- Extensive on-line help

MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PICmicro® tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file

The ability to use MPLAB with Microchip's simulator allows a consistent platform and the ability to easily switch from the low cost simulator to the full featured emulator with minimal retraining due to development tools.

### 10.11 Assembler (MPASM)

The MPASM Universal Macro Assembler is a PC-hosted symbolic assembler. It supports all microcontroller series including the PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX, and PIC17CXX families.

MPASM offers full featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from MPLAB-ICE, Microchip's Universal Emulator System.

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro assembly capability.
- Produces all the files (Object, Listing, Symbol, and special) required for symbolic debug with Microchip's emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a rich directive language to support programming of the PICmicro®. Directives are helpful in making the development of your assemble source code shorter and more maintainable.

### 10.12 Software Simulator (MPLAB-SIM)

The MPLAB-SIM Software Simulator allows code development in a PC host environment. It allows the user to simulate the PICmicro® series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in; single step, execute until break, or in a trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C17 and MPASM. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

### 10.13 MPLAB-C17 Compiler

The MPLAB-C17 Code Development System is a complete ANSI 'C' compiler and integrated development environment for Microchip's PIC17CXXX family of microcontrollers. The compiler provides powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compiler provides symbol information that is compatible with the MPLAB IDE memory display.

### 10.14 Fuzzy Logic Development System (*fuzzy*TECH-MP)

*fuzzy*TECH-MP fuzzy logic development tool is available in two versions - a low cost introductory version, MP Explorer, for designers to gain a comprehensive working knowledge of fuzzy logic system design; and a full-featured version, *fuzzy*TECH-MP, Edition for implementing more complex systems.

Both versions include Microchip's *fuzzy*LAB™ demonstration board for hands-on experience with fuzzy logic systems implementation.

### 10.15 SEEVAL® Evaluation and Programming System

The SEEVAL SEEPROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials™ and secure serials. The Total Endurance™ Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

**NOTES:**

**TABLE 13-8: EEPROM MEMORY BUS TIMING REQUIREMENTS - PIC12CE5XX ONLY.**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C, Vcc = 3.0V to 5.5V (commercial)<br>–40°C ≤ TA ≤ +85°C, Vcc = 3.0V to 5.5V (industrial)<br>–40°C ≤ TA ≤ +125°C, Vcc = 4.5V to 5.5V (extended)<br>Operating Voltage VDD range is described in Section 13.1 | | | | |
|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Units** | **Conditions** |
| Clock frequency | FCLK | —<br>—<br>— | 100<br>100<br>400 | kHz | 4.5V ≤ Vcc ≤ 5.5V (E Temp range)<br>3.0V ≤ Vcc ≤ 4.5V<br>4.5V ≤ Vcc ≤ 5.5V |
| Clock high time | THIGH | 4000<br>4000<br>600 | —<br>—<br>— | ns | 4.5V ≤ Vcc ≤ 5.5V (E Temp range)<br>3.0V ≤ Vcc ≤ 4.5V<br>4.5V ≤ Vcc ≤ 5.5V |
| Clock low time | TLOW | 4700<br>4700<br>1300 | —<br>—<br>— | ns | 4.5V ≤ Vcc ≤ 5.5V (E Temp range)<br>3.0V ≤ Vcc ≤ 4.5V<br>4.5V ≤ Vcc ≤ 5.5V |
| SDA and SCL rise time (Note 1) | TR | —<br>—<br>— | 1000<br>1000<br>300 | ns | 4.5V ≤ Vcc ≤ 5.5V (E Temp range)<br>3.0V ≤ Vcc ≤ 4.5V<br>4.5V ≤ Vcc ≤ 5.5V |
| SDA and SCL fall time | TF | — | 300 | ns | (Note 1) |
| START condition hold time | THD:STA | 4000<br>4000<br>600 | —<br>—<br>— | ns | 4.5V ≤ Vcc ≤ 5.5V (E Temp range)<br>3.0V ≤ Vcc ≤ 4.5V<br>4.5V ≤ Vcc ≤ 5.5V |
| START condition setup time | TSU:STA | 4700<br>4700<br>600 | —<br>—<br>— | ns | 4.5V ≤ Vcc ≤ 5.5V (E Temp range)<br>3.0V ≤ Vcc ≤ 4.5V<br>4.5V ≤ Vcc ≤ 5.5V |
| Data input hold time | THD:DAT | 0 | — | ns | (Note 2) |
| Data input setup time | TSU:DAT | 250<br>250<br>100 | —<br>—<br>— | ns | 4.5V ≤ Vcc ≤ 5.5V (E Temp range)<br>3.0V ≤ Vcc ≤ 4.5V<br>4.5V ≤ Vcc ≤ 5.5V |
| STOP condition setup time | TSU:STO | 4000<br>4000<br>600 | —<br>—<br>— | ns | 4.5V ≤ Vcc ≤ 5.5V (E Temp range)<br>3.0V ≤ Vcc ≤ 4.5V<br>4.5V ≤ Vcc ≤ 5.5V |
| Output valid from clock (Note 2) | TAA | —<br>—<br>— | 3500<br>3500<br>900 | ns | 4.5V ≤ Vcc ≤ 5.5V (E Temp range)<br>3.0V ≤ Vcc ≤ 4.5V<br>4.5V ≤ Vcc ≤ 5.5V |
| Bus free time: Time the bus must be free before a new transmission can start | TBUF | 4700<br>4700<br>1300 | —<br>—<br>— | ns | 4.5V ≤ Vcc ≤ 5.5V (E Temp range)<br>3.0V ≤ Vcc ≤ 4.5V<br>4.5V ≤ Vcc ≤ 5.5V |
| Output fall time from VIH minimum to VIL maximum | TOF | 20+0.1 CB | 250 | ns | (Note 1), CB ≤ 100 pF |
| Input filter spike suppression (SDA and SCL pins) | TSP | — | 50 | ns | (Notes 1, 3) |
| Write cycle time | TWC | — | 4 | ms | |
| Endurance | | 1M | — | cycles | 25°C, VCC = 5.0V, Block Mode (Note 4) |

**Note 1:** Not 100% tested. CB = total capacitance of one bus line in pF.

**2:** As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

**3:** The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

**4:** This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on Microchip's website.

**FIGURE 14-5: WDT TIMER TIME-OUT PERIOD vs. VDD**

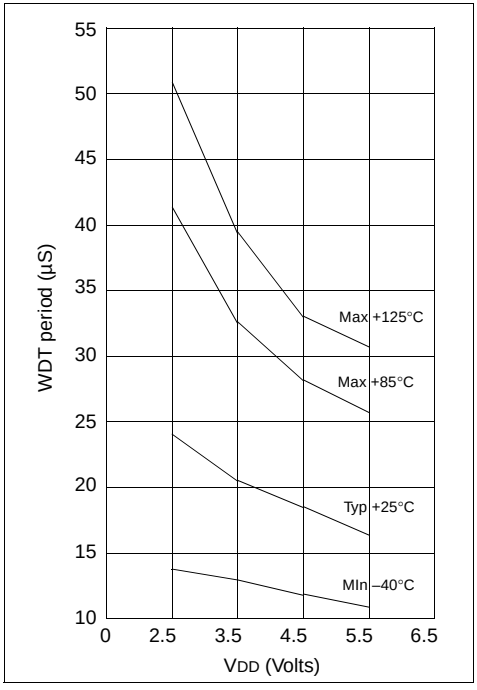



**FIGURE 14-6: SHORT DRT PERIOD VS. VDD**

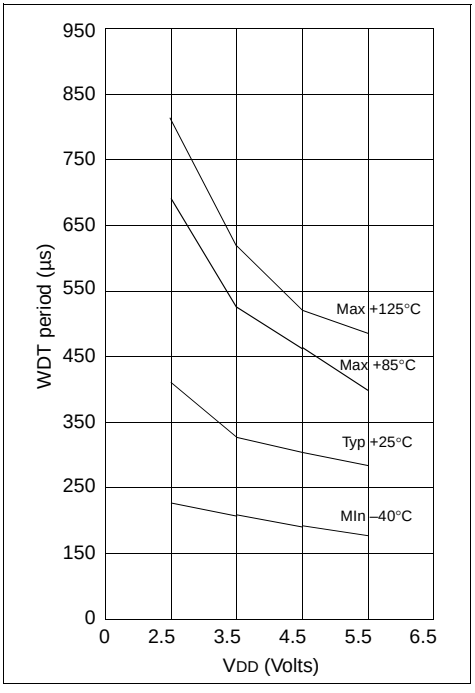



**FIGURE 14-7: IOH vs. VOH, VDD = 2.5 V**

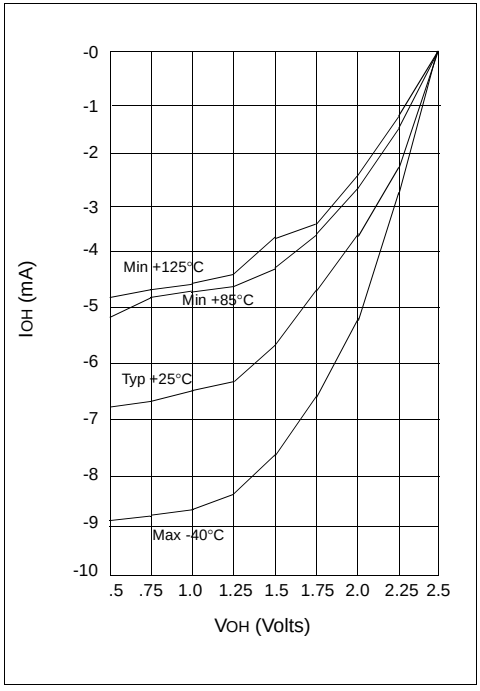
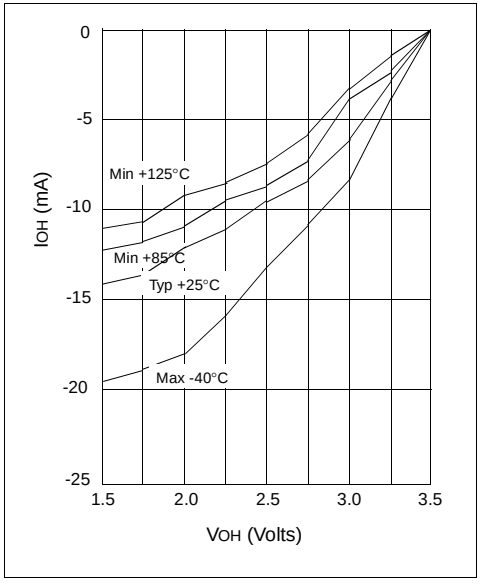


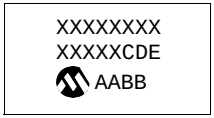

**FIGURE 14-8: IOH vs. VOH, VDD = 3.5 V**



## 15.0 PACKAGING INFORMATION

### 15.1 Package Marking Information

8-Lead PDIP (300 mil)

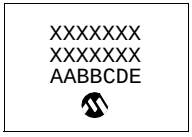



Example


8-Lead SOIC (150 mil)

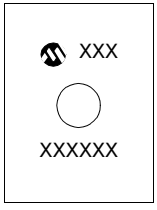

Example


8-Lead SOIC (208 mil)

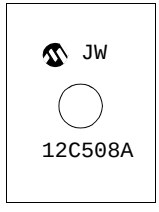



Example


8-Lead Windowed Ceramic Side Brazed (300 mil)



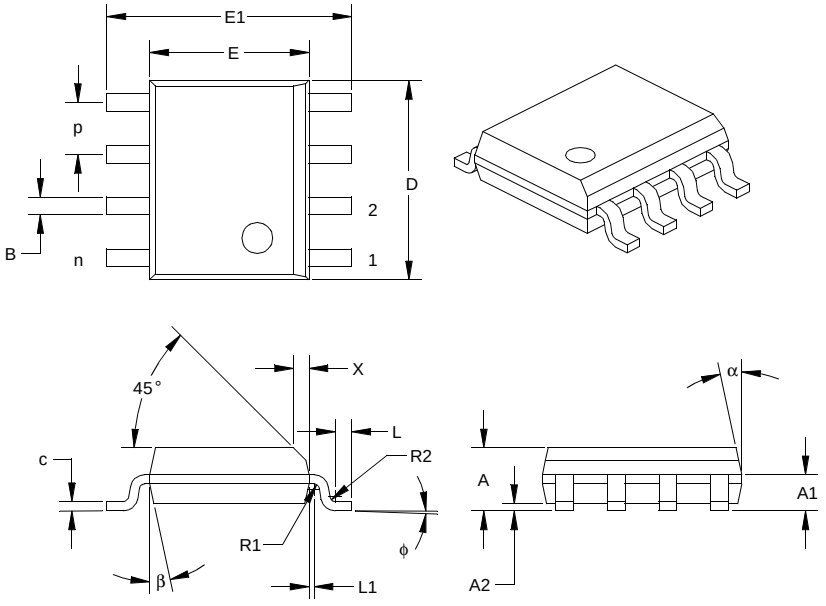

Example




| | | |
|---|---|---|
| **Legend:** | MM...M | Microchip part number information |
| | XX...X | Customer specific information* |
| | AA | Year code (last 2 digits of calendar year) |
| | BB | Week code (week of January 1 is week ‘01’) |
| | C | Facility code of the plant at which wafer is manufactured<br>O = Outside Vendor<br>C = 5” Line<br>S = 6” Line<br>H = 8” Line |
| | D | Mask revision number |
| | E | Assembly code of the plant or country of origin in which part was assembled |
| **Note**: | | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information. |

***** Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

**Package Type: K04-057 8-Lead Plastic Small Outline (SN) – Narrow, 150 mil**



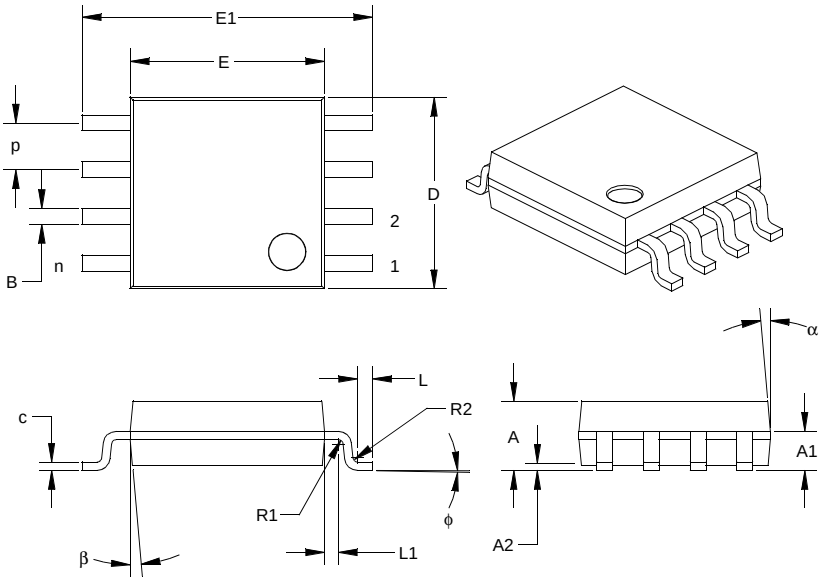

| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Pitch | p | | 0.050 | | | 1.27 | |
| Number of Pins | n | | 8 | | | 8 | |
| Overall Pack. Height | A | 0.054 | 0.061 | 0.069 | 1.37 | 1.56 | 1.75 |
| Shoulder Height | A1 | 0.027 | 0.035 | 0.044 | 0.69 | 0.90 | 1.11 |
| Standoff | A2 | 0.004 | 0.007 | 0.010 | 0.10 | 0.18 | 0.25 |
| Molded Package Length | D‡ | 0.189 | 0.193 | 0.196 | 4.80 | 4.89 | 4.98 |
| Molded Package Width | E‡ | 0.150 | 0.154 | 0.157 | 3.81 | 3.90 | 3.99 |
| Outside Dimension | E1 | 0.229 | 0.237 | 0.244 | 5.82 | 6.01 | 6.20 |
| Chamfer Distance | X | 0.010 | 0.015 | 0.020 | 0.25 | 0.38 | 0.51 |
| Shoulder Radius | R1 | 0.005 | 0.005 | 0.010 | 0.13 | 0.13 | 0.25 |
| Gull Wing Radius | R2 | 0.005 | 0.005 | 0.010 | 0.13 | 0.13 | 0.25 |
| Foot Length | L | 0.011 | 0.016 | 0.021 | 0.28 | 0.41 | 0.53 |
| Foot Angle | ϕ | 0 | 4 | 8 | 0 | 4 | 8 |
| Radius Centerline | L1 | 0.000 | 0.005 | 0.010 | 0.00 | 0.13 | 0.25 |
| Lead Thickness | c | 0.008 | 0.009 | 0.010 | 0.19 | 0.22 | 0.25 |
| Lower Lead Width | B† | 0.014 | 0.017 | 0.020 | 0.36 | 0.43 | 0.51 |
| Mold Draft Angle Top | α | 0 | 12 | 15 | 0 | 12 | 15 |
| Mold Draft Angle Bottom | β | 0 | 12 | 15 | 0 | 12 | 15 |

* Controlling Parameter.

† Dimension “B” does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003” (0.076 mm) per side or 0.006” (0.152 mm) more than dimension “B.”

‡ Dimensions “D” and “E” do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010” (0.254 mm) per side or 0.020” (0.508 mm) more than dimensions “D” or “E.”

**Package Type: K04-056 8-Lead Plastic Small Outline (SM) – Medium, 208 mil**




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Pitch | p | | 0.050 | | | 1.27 | |
| Number of Pins | n | | 8 | | | 8 | |
| Overall Pack. Height | A | 0.070 | 0.074 | 0.079 | 1.78 | 1.89 | 2.00 |
| Shoulder Height | A1 | 0.037 | 0.042 | 0.048 | 0.94 | 1.08 | 1.21 |
| Standoff | A2 | 0.002 | 0.005 | 0.009 | 0.05 | 0.14 | 0.22 |
| Molded Package Length | D‡ | 0.200 | 0.205 | 0.210 | 5.08 | 5.21 | 5.33 |
| Molded Package Width | E‡ | 0.203 | 0.208 | 0.213 | 5.16 | 5.28 | 5.41 |
| Outside Dimension | E1 | 0.300 | 0.313 | 0.325 | 7.62 | 7.94 | 8.26 |
| Shoulder Radius | R1 | 0.005 | 0.005 | 0.010 | 0.13 | 0.13 | 0.25 |
| Gull Wing Radius | R2 | 0.005 | 0.005 | 0.010 | 0.13 | 0.13 | 0.25 |
| Foot Length | L | 0.011 | 0.016 | 0.021 | 0.28 | 0.41 | 0.53 |
| Foot Angle | ϕ | 0 | 4 | 8 | 0 | 4 | 8 |
| Radius Centerline | L1 | 0.010 | 0.015 | 0.020 | 0.25 | 0.38 | 0.51 |
| Lead Thickness | c | 0.008 | 0.009 | 0.010 | 0.19 | 0.22 | 0.25 |
| Lower Lead Width | B† | 0.014 | 0.017 | 0.020 | 0.36 | 0.43 | 0.51 |
| Mold Draft Angle Top | α | 0 | 12 | 15 | 0 | 12 | 15 |
| Mold Draft Angle Bottom | β | 0 | 12 | 15 | 0 | 12 | 15 |

* Controlling Parameter.

† Dimension “B” does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003” (0.076 mm) per side or 0.006” (0.152 mm) more than dimension “B.”

‡ Dimensions “D” and “E” do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010” (0.254 mm) per side or 0.020” (0.508 mm) more than dimensions “D” or “E.”

**Note the following details of the code protection feature on PICmicro® MCUs.**

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable”.
- Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our product.

If you have any further questions about this matter, please contact the local sales office nearest to you.



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*Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999. The Company’s quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs and microperipheral products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001 certified.*

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