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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	41 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.209", 5.30mm Width)
Supplier Device Package	8-SOIJ
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12c509at-04i-sm

PIC12C5XX

4.2 Data Memory Organization

Data memory is composed of registers, or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: special function registers and general purpose registers.

The special function registers include the TMR0 register, the Program Counter (PC), the Status Register, the I/O registers (ports), and the File Select Register (FSR). In addition, special purpose registers are used to control the I/O port configuration and prescaler options.

The general purpose registers are used for data and control information under command of the instructions.

For the PIC12C508, PIC12C508A and PIC12CE518, the register file is composed of 7 special function registers and 25 general purpose registers (Figure 4-2).

For the PIC12C509, PIC12C509A, PIC12CR509A, and PIC12CE519 the register file is composed of 7 special function registers, 25 general purpose registers, and 16 general purpose registers that may be addressed using a banking scheme (Figure 4-3).

4.2.1 GENERAL PURPOSE REGISTER FILE

The general purpose register file is accessed either directly or indirectly through the file select register FSR (Section 4.8).

FIGURE 4-2: PIC12C508, PIC12C508A AND PIC12CE518 REGISTER FILE MAP

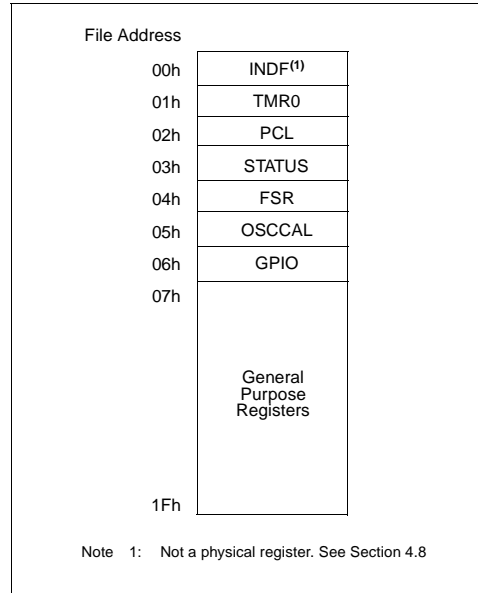
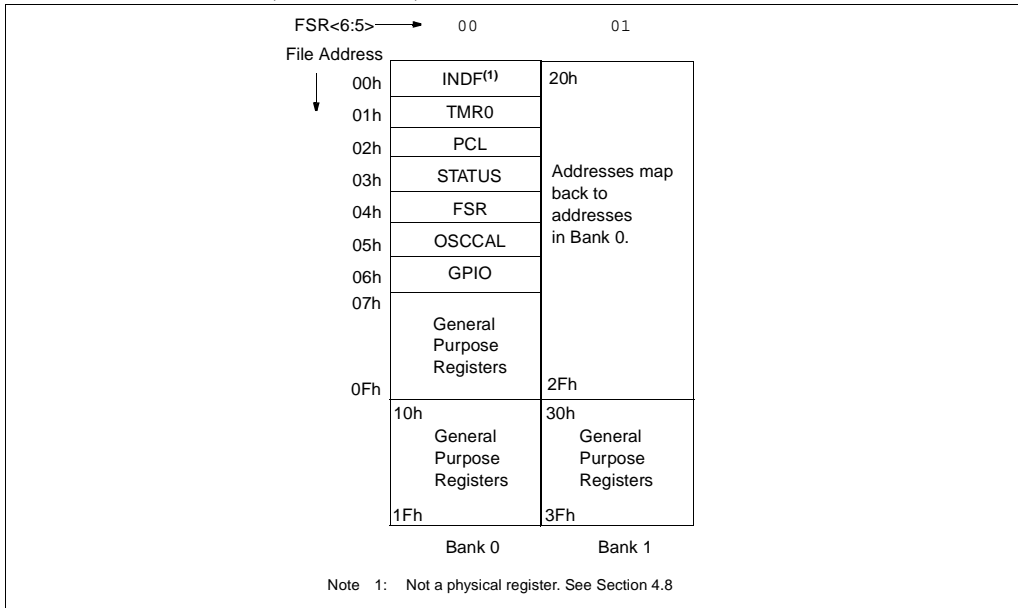


FIGURE 4-3: PIC12C509, PIC12C509A, PIC12CR509A AND PIC12CE519 REGISTER FILE MAP



4.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status, and the page preselect bit for program memories larger than 512 words.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the \overline{TO} and \overline{PD} bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS register because these instructions do not affect the Z, DC or C bits from the STATUS register. For other instructions, which do affect STATUS bits, see Instruction Set Summary.

FIGURE 4-4: STATUS REGISTER (ADDRESS:03h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
GPWUF	—	PA0	\overline{TO}	\overline{PD}	Z	DC	C
bit7	6	5	4	3	2	1	bit0

bit 7: **GPWUF**: GPIO reset bit
1 = Reset due to wake-up from SLEEP on pin change
0 = After power up or other reset

bit 6: **Unimplemented**

bit 5: **PA0**: Program page preselect bits
1 = Page 1 (200h - 3FFh) - PIC12C509, PIC12C509A, PIC12CR509A and PIC12CE519
0 = Page 0 (000h - 1FFh) - PIC12C5XX
Each page is 512 bytes.
Using the PA0 bit as a general purpose read/write bit in devices which do not use it for program page preselect is not recommended since this may affect upward compatibility with future products.

bit 4: **\overline{TO}** : Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: **\overline{PD}** : Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/borrow bit (for `ADDWF` and `SUBWF` instructions)
ADDWF
1 = A carry from the 4th low order bit of the result occurred
0 = A carry from the 4th low order bit of the result did not occur
SUBWF
1 = A borrow from the 4th low order bit of the result did not occur
0 = A borrow from the 4th low order bit of the result occurred

bit 0: **C**: Carry/borrow bit (for `ADDWF`, `SUBWF` and `RRF`, `RLF` instructions)
ADDWF
1 = A carry occurred
0 = A carry did not occur
SUBWF
1 = A borrow did not occur
0 = A borrow occurred
RRF or RLF
Load bit with LSB or MSB, respectively

R = Readable bit
W = Writable bit
- n = Value at POR reset

PIC12C5XX

4.5 OSCCAL Register

The Oscillator Calibration (OSCCAL) register is used to calibrate the internal 4 MHz oscillator. It contains four to six bits for calibration. Increasing the cal value increases the frequency. See Section 7.2.5 for more information on the internal oscillator.

FIGURE 4-6: OSCCAL REGISTER (ADDRESS 05h) FOR PIC12C508 AND PIC12C509

R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	U-0	U-0
CAL3	CAL2	CAL1	CAL0	—	—	—	—
bit7				bit0			

R = Readable bit
W = Writable bit
U = Unimplemented bit,
read as '0'
- n = Value at POR reset

bit 7-4: **CAL<3:0>**: Calibration

bit 3-0: **Unimplemented**: Read as '0'

FIGURE 4-7: OSCCAL REGISTER (ADDRESS 05h) FOR PIC12C508A/C509A/CR509A/12CE518/12CE519

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	—
bit7						bit0	

bit 7-2: **CAL<5:0>**: Calibration

bit 1-0: **Unimplemented**: Read as '0'

R = Readable bit
W = Writable bit
U = Unimplemented bit,
read as '0'
- n = Value at POR reset

4.6 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

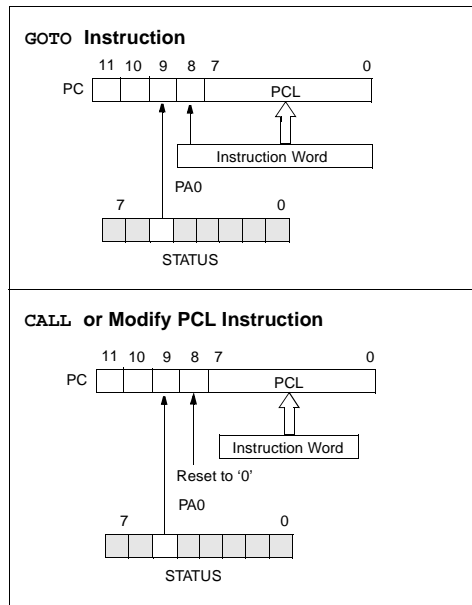
For a GOTO instruction, bits 8:0 of the PC are provided by the GOTO instruction word. The PC Latch (PCL) is mapped to PC<7:0>. Bit 5 of the STATUS register provides page information to bit 9 of the PC (Figure 4-8).

For a CALL instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-8).

Instructions where the PCL is the destination, or Modify PCL instructions, include MOVWF PC, ADDWF PC, and BSF PC, 5.

Note: Because PC<8> is cleared in the CALL instruction, or any Modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-8: LOADING OF PC BRANCH INSTRUCTIONS - PIC12C5XX



4.6.1 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page i.e., the oscillator calibration instruction. After executing MOVLW XX, the PC will roll over to location 00h, and begin executing user code.

The STATUS register page preselect bits are cleared upon a RESET, which means that page 0 is pre-selected.

Therefore, upon a RESET, a GOTO instruction will automatically cause the program to jump to page 0 until the value of the page bits is altered.

4.7 Stack

PIC12C5XX devices have a 12-bit wide L.I.F.O. hardware push/pop stack.

A CALL instruction will *push* the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential CALLs are executed, only the most recent two return addresses are stored.

A RETLW instruction will *pop* the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential RETLW's are executed, the stack will be filled with the address previously stored in level 2. Note that the W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

Upon any reset, the contents of the stack remain unchanged, however the program counter (PCL) will also be reset to 0.

Note 1: There are no STATUS bits to indicate stack overflows or stack underflow conditions.

Note 2: There are no instructions mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL and RETLW instructions.

TABLE 5-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	TRIS	—	—							--11 1111	--11 1111
N/A	OPTION	GPWU	GPPU	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
03H	STATUS	GPWUF	—	PAO	\overline{TO}	\overline{PD}	Z	DC	C	0001 1xxx	q00q quuu ⁽¹⁾
06h	GPIO (PIC12C508/ PIC12C509/ PIC12C508A/ PIC12C509A/ PIC12CR509A)	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	--uu uuuu
06h	GPIO (PIC12CE518/ PIC12CE519)	SCL	SDA	GP5	GP4	GP3	GP2	GP1	GP0	11xx xxxx	11uu uuuu

Legend: Shaded cells not used by Port Registers, read as '0', — = unimplemented, read as '0', x = unknown, u = unchanged, q = see tables in Section 8.7 for possible values.

Note 1: If reset was due to wake-up on change, then bit 7 = 1. All other resets will cause bit 7 = 0.

5.4 I/O Programming Considerations

5.4.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of GPIO will cause all eight bits of GPIO to be read into the CPU, bit5 to be set and the GPIO value to be written to the output latches. If another bit of GPIO is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```

;Initial GPIO Settings
; GPIO<5:3> Inputs
; GPIO<2:0> Outputs
;
;
;          GPIO latch  GPIO pins
;          -----
BCF  GPIO, 5  ;--01 -ppp  --11 pppp
BCF  GPIO, 4  ;--10 -ppp  --11 pppp
MOVLW 007h    ;
TRIS  GPIO    ;--10 -ppp  --11 pppp
;
;Note that the user may have expected the pin
;values to be --00 pppp. The 2nd BCF caused
;GP5 to be latched as the pin value (High).

```

5.4.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

7.0.2 SERIAL CLOCK

This SCL input is used to synchronize the data transfer from and to the device.

7.1 BUS CHARACTERISTICS

The following **bus protocol** is to be used with the EEPROM data memory.

- Data transfer may be initiated only when the bus is not busy.

During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 7-3).

7.1.1 BUS NOT BUSY (A)

Both data and clock lines remain HIGH.

7.1.2 START DATA TRANSFER (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

7.1.3 STOP DATA TRANSFER (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

7.1.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

7.1.5 ACKNOWLEDGE

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

<p>Note: Acknowledge bits are not generated if an internal programming cycle is in progress.</p>

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition (Figure 7-4).

7.3 WRITE OPERATIONS

7.3.1 BYTE WRITE

Following the start signal from the master, the device code (4 bits), the don't care bits (3 bits), and the R/W bit (which is a logic low) are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer. Only the lower four address bits are used by the device, and the upper four bits are don't cares. The address byte is acknowledgeable and the master device will then transmit the data word to be written into the addressed memory location. The memory acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time will not generate acknowledge signals (Figure 7-7). After a byte write command, the internal address counter will not be incremented and will point to the same address location that was just written. If a stop bit is transmitted to the device at any point in the write command sequence before the entire sequence is complete, then the command will abort and no data will be written. If more than 8 data bits are transmitted before the stop bit is sent, then the device will clear the previously loaded byte and begin loading the data buffer again. If more than one data byte is transmitted to the device and a stop bit is sent before a full eight data bits have been transmitted, then the write command will abort and no data will be written. The EEPROM memory employs a VCC threshold detector circuit which disables the internal erase/write logic if the VCC is below minimum VDD.

Byte write operations must be preceded and immediately followed by a bus not busy bus cycle where both SDA and SCL are held high.

7.4 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/W = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the start bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-6 for flow diagram.

FIGURE 7-6: ACKNOWLEDGE POLLING FLOW

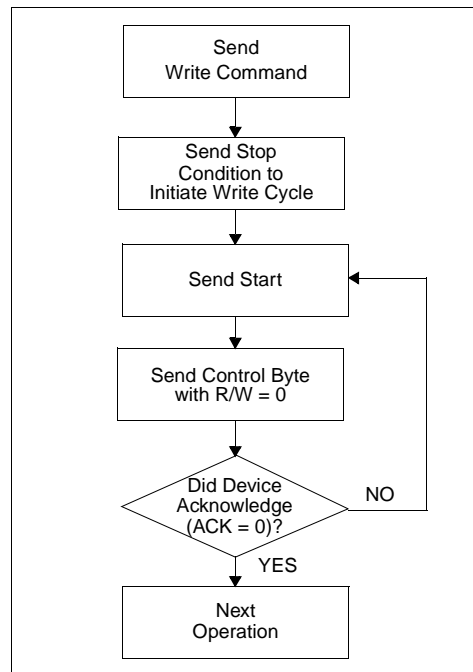
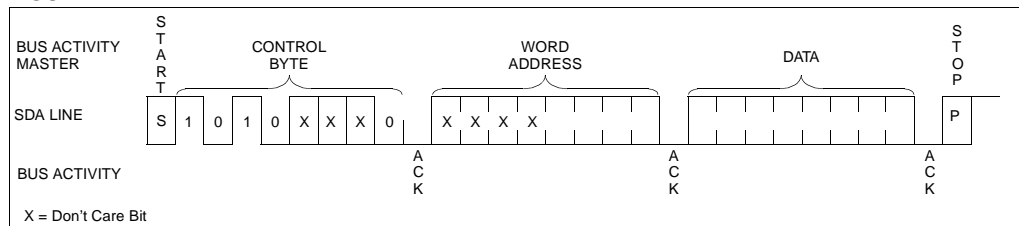


FIGURE 7-7: BYTE WRITE



8.7 Time-Out Sequence, Power Down, and Wake-up from SLEEP Status Bits (TO/PD/GPWUF)

The \overline{TO} , \overline{PD} , and GPWUF bits in the STATUS register can be tested to determine if a RESET condition has been caused by a power-up condition, a \overline{MCLR} or Watchdog Timer (WDT) reset.

TABLE 8-7: $\overline{TO}/\overline{PD}/\overline{GPWUF}$ STATUS AFTER RESET

GPWUF	\overline{TO}	\overline{PD}	RESET caused by
0	0	0	WDT wake-up from SLEEP
0	0	u	WDT time-out (not from SLEEP)
0	1	0	\overline{MCLR} wake-up from SLEEP
0	1	1	Power-up
0	u	u	\overline{MCLR} not during SLEEP
1	1	0	Wake-up from SLEEP on pin change

Legend: u = unchanged

Note 1: The \overline{TO} , \overline{PD} , and GPWUF bits maintain their status (u) until a reset occurs. A low-pulse on the \overline{MCLR} input does not change the \overline{TO} , \overline{PD} , and GPWUF status bits.

8.8 Reset on Brown-Out

A brown-out is a condition where device power (V_{DD}) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

To reset PIC12C5XX devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 8-13, Figure 8-14 and Figure 8-15

FIGURE 8-13: BROWN-OUT PROTECTION CIRCUIT 1

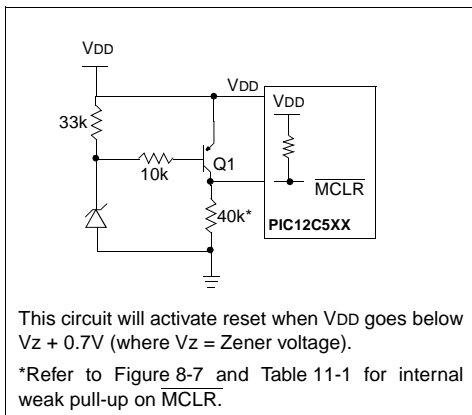


FIGURE 8-14: BROWN-OUT PROTECTION CIRCUIT 2

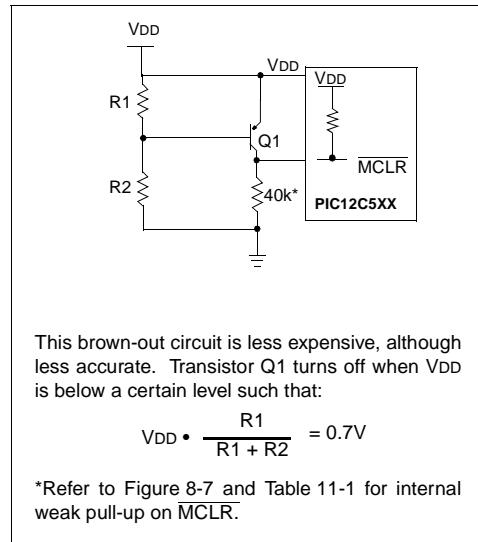
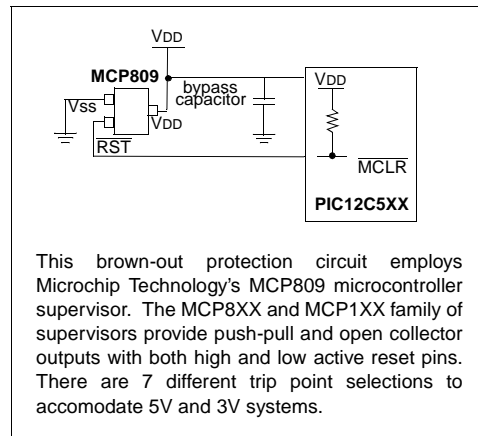


FIGURE 8-15: BROWN-OUT PROTECTION CIRCUIT 3



8.12 In-Circuit Serial Programming

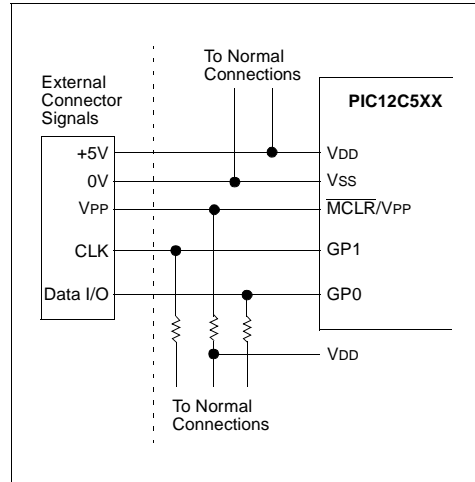
The PIC12C5XX microcontrollers with EPROM program memory can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a program/verify mode by holding the GP1 and GP0 pins low while raising the MCLR (VPP) pin from V_{IL} to V_{IH} (see programming specification). GP1 becomes the programming clock and GP0 becomes the programming data. Both GP1 and GP0 are Schmitt Trigger inputs in this mode.

After reset, a 6-bit command is then supplied to the device. Depending on the command, 14-bits of program data are then supplied to or from the device, depending if the command was a load or a read. For complete details of serial programming, please refer to the PIC12C5XX Programming Specifications.

A typical in-circuit serial programming connection is shown in Figure 8-16.

FIGURE 8-16: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



SLEEP	Enter SLEEP Mode			
Syntax:	[<i>label</i>] SLEEP			
Operands:	None			
Operation:	00h → WDT; 0 → WDT prescaler; 1 → \overline{TO} ; 0 → \overline{PD}			
Status Affected:	\overline{TO} , \overline{PD} , GPWUF			
Encoding:	<table border="1"><tr><td>0000</td><td>0000</td><td>0011</td></tr></table>	0000	0000	0011
0000	0000	0011		
Description:	<p>Time-out status bit (\overline{TO}) is set. The power down status bit (\overline{PD}) is cleared. GPWUF is unaffected.</p> <p>The WDT and its prescaler are cleared.</p> <p>The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP for more details.</p>			
Words:	1			
Cycles:	1			
Example:	SLEEP			

SUBWF	Subtract W from f			
Syntax:	[label] SUBWF f,d			
Operands:	$0 \leq f \leq 31$ $d \in [0,1]$			
Operation:	$(f) - (W) \rightarrow (\text{dest})$			
Status Affected:	C, DC, Z			
Encoding:	<table border="1"><tr><td>0000</td><td>10df</td><td>ffff</td></tr></table>	0000	10df	ffff
0000	10df	ffff		
Description:	Subtract (2's complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.			
Words:	1			
Cycles:	1			
Example 1:	SUBWF REG1, 1			

Before Instruction

REG1 = 3
W = 2
C = ?

After Instruction

REG1 = 1
W = 2
C = 1 ; result is positive

Example 2:

Before Instruction

REG1 = 2
W = 2
C = ?

After Instruction

REG1 = 0
W = 2
C = 1 ; result is zero

Example 3:

Before Instruction

REG1 = 1
W = 2
C = ?

After Instruction

REG1 = FF
W = 2
C = 0 ; result is negative

10.10 MPLAB Integrated Development Environment Software

The MPLAB IDE Software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a windows based application which contains:

- A full featured editor
- Three operating modes
 - editor
 - emulator
 - simulator
- A project manager
- Customizable tool bar and key mapping
- A status bar with project information
- Extensive on-line help

MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PICmicro[®] tools (automatically updates all project information)
- Debug using:
 - source files
 - absolute listing file

The ability to use MPLAB with Microchip's simulator allows a consistent platform and the ability to easily switch from the low cost simulator to the full featured emulator with minimal retraining due to development tools.

10.11 Assembler (MPASM)

The MPASM Universal Macro Assembler is a PC-hosted symbolic assembler. It supports all microcontroller series including the PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX, and PIC17CXX families.

MPASM offers full featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from MPLAB-ICE, Microchip's Universal Emulator System.

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro assembly capability.
- Produces all the files (Object, Listing, Symbol, and special) required for symbolic debug with Microchip's emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a rich directive language to support programming of the PICmicro[®]. Directives are helpful in making the development of your assemble source code shorter and more maintainable.

10.12 Software Simulator (MPLAB-SIM)

The MPLAB-SIM Software Simulator allows code development in a PC host environment. It allows the user to simulate the PICmicro[®] series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in; single step, execute until break, or in a trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C17 and MPASM. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

10.13 MPLAB-C17 Compiler

The MPLAB-C17 Code Development System is a complete ANSI 'C' compiler and integrated development environment for Microchip's PIC17CXXX family of microcontrollers. The compiler provides powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compiler provides symbol information that is compatible with the MPLAB IDE memory display.

10.14 Fuzzy Logic Development System (fuzzyTECH-MP)

fuzzyTECH-MP fuzzy logic development tool is available in two versions - a low cost introductory version, MP Explorer, for designers to gain a comprehensive working knowledge of fuzzy logic system design; and a full-featured version, *fuzzyTECH-MP*, Edition for implementing more complex systems.

Both versions include Microchip's *fuzzyLAB*[™] demonstration board for hands-on experience with fuzzy logic systems implementation.

10.15 SEEVAL[®] Evaluation and Programming System

The SEEVAL SEEPROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials[™] and secure serials. The Total Endurance[™] Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

TABLE 10-1: DEVELOPMENT TOOLS FROM MICROCHIP

	PIC12C5XX	PIC14000	PIC16C5X	PIC16CXXX	PIC16C6X	PIC16C7XX	PIC16C8X	PIC16C9XX	PIC17C4X	PIC17C7XX	24CXX 25CXX 93CXX	HCS200 HCS300 HCS301
Emulator Products												
MPLAB™-ICE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
ICEPIC™ Low-Cost In-Circuit Emulator			✓	✓	✓	✓	✓	✓				
Software Tools												
MPLAB™ Integrated Development Environment	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
MPLAB™ C17* Compiler									✓	✓		
fuzzyTECH®-MP Explorer/Editor Fuzzy Logic Dev. Tool	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Total Endurance™ Software Model											✓	
Programmers												
PICSTART®Plus Low-Cost Universal Dev. Kit	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
PRO MATE® II Universal Programmer	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓
KEELOQ® Programmer												✓
Demo Boards												
SEEVAL® Designers Kit											✓	
SIMICE	✓		✓									
PICDEM-14A		✓										
PICDEM-1			✓	✓			✓		✓			
PICDEM-2					✓	✓						
PICDEM-3								✓				
KEELOQ® Evaluation Kit												✓
KEELOQ Transponder Kit												✓

11.4 Timing Diagrams and Specifications

FIGURE 11-2: EXTERNAL CLOCK TIMING - PIC12C508/C509

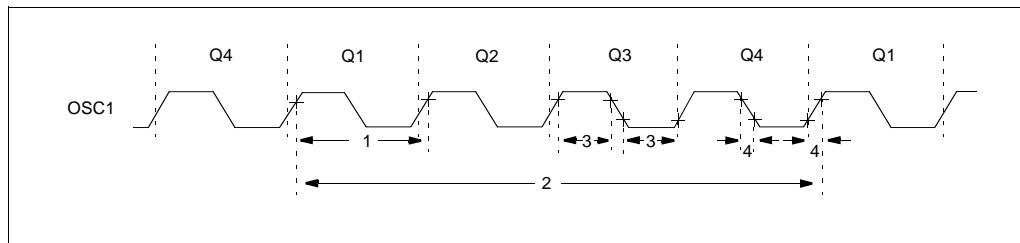


TABLE 11-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC12C508/C509

AC Characteristics Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial), $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial), $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) Operating Voltage V_{DD} range is described in Section 11.1							
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
	Fosc	External CLKIN Frequency ⁽²⁾	DC	—	4	MHz	XT osc mode
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency ⁽²⁾	0.1	—	4	MHz	XT osc mode
			DC	—	200	kHz	LP osc mode
1	Tosc	External CLKIN Period ⁽²⁾	250	—	—	ns	EXTRC osc mode
			250	—	—	ns	XT osc mode
			5	—	—	ms	LP osc mode
		Oscillator Period ⁽²⁾	250	—	—	ns	EXTRC osc mode
			250	—	10,000	ns	XT osc mode
			5	—	—	ms	LP osc mode
2	Tcy	Instruction Cycle Time ⁽³⁾	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			2*	—	—	ms	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	50*	ns	LP oscillator

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (Tcy) equals four times the input oscillator time base period.

13.0 ELECTRICAL CHARACTERISTICS - PIC12C508A/PIC12C509A/ PIC12LC508A/PIC12LC509A/PIC12CR509A/PIC12CE518/PIC12CE519/ PIC12LCE518/PIC12LCE519/PIC12LCR509A

Absolute Maximum Ratings†

Ambient Temperature under bias	-40°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on V _{DD} with respect to V _{SS}	0 to +7.0 V
Voltage on $\overline{\text{MCLR}}$ with respect to V _{SS}	0 to +14 V
Voltage on all other pins with respect to V _{SS}	-0.3 V to (V _{DD} + 0.3 V)
Total Power Dissipation ⁽¹⁾	700 mW
Max. Current out of V _{SS} pin	200 mA
Max. Current into V _{DD} pin	150 mA
Input Clamp Current, I _{IK} (V _I < 0 or V _I > V _{DD})	±20 mA
Output Clamp Current, I _{OK} (V _O < 0 or V _O > V _{DD}).....	±20 mA
Max. Output Current sunk by any I/O pin.....	25 mA
Max. Output Current sourced by any I/O pin.....	25 mA
Max. Output Current sourced by I/O port (GPIO)	100 mA
Max. Output Current sunk by I/O port (GPIO)	100 mA

Note 1: Power Dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

13.2 DC CHARACTERISTICS: **PIC12LC508A/509A (Commercial, Industrial)**
PIC12LCE518/519 (Commercial, Industrial)
PIC12LCR509A (Commercial, Industrial)

DC Characteristics Power Supply Pins			Standard Operating Conditions (unless otherwise specified)						
			Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) −40°C ≤ TA ≤ +85°C (industrial)						
Parm No.	Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions		
D001	Supply Voltage	VDD	2.5		5.5	V	FOSC = DC to 4 MHz (Commercial/ Industrial)		
D002	RAM Data Retention Voltage ⁽²⁾	VDR		1.5*		V	Device in SLEEP mode		
D003	VDD Start Voltage to ensure Power-on Reset	VPOR		VSS		V	See section on Power-on Reset for details		
D004	VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See section on Power-on Reset for details		
D010	Supply Current ⁽³⁾	IDD	—	0.4	0.8	mA	XT and EXTRC options (Note 4) FOSC = 4 MHz, VDD = 2.5V		
D010C			—	0.4	0.8	mA	INTRC Option FOSC = 4 MHz, VDD = 2.5V		
D010A			—	15	23	μA	LP OPTION, Commercial Temperature FOSC = 32 kHz, VDD = 2.5V, WDT disabled		
			—	15	31	μA	LP OPTION, Industrial Temperature FOSC = 32 kHz, VDD = 2.5V, WDT disabled		
D020	Power-Down Current ⁽⁵⁾	IPD	—	0.2	3	μA	VDD = 2.5V, Commercial		
D021			—	0.2	4	μA	VDD = 2.5V, Industrial		
D021B									
		ΔIWD	—	2.0	4	mA	VDD = 2.5V, Commercial		
				2.0	5	mA	VDD = 2.5V, Industrial		

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kOhm.

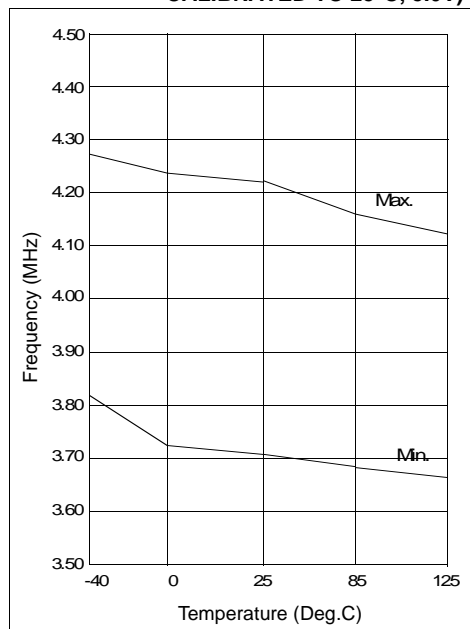
5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

14.0 DC AND AC CHARACTERISTICS - PIC12C508A/PIC12C509A/ PIC12LC508A/PIC12LC509A, PIC12CE518/PIC12CE519/PIC12CR509A/ PIC12LCE518/PIC12LCE519/ PIC12LCR509A

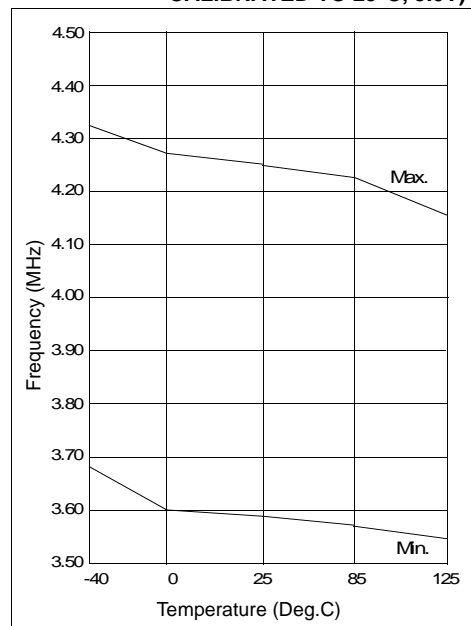
The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified V_{DD} range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean - 3σ) respectively, where σ is standard deviation.

**FIGURE 14-1: CALIBRATED INTERNAL RC
FREQUENCY RANGE VS.
TEMPERATURE ($V_{DD} = 5.0V$)
(INTERNAL RC IS
CALIBRATED TO 25°C, 5.0V)**



**FIGURE 14-2: CALIBRATED INTERNAL RC
FREQUENCY RANGE VS.
TEMPERATURE ($V_{DD} = 2.5V$)
(INTERNAL RC IS
CALIBRATED TO 25°C, 5.0V)**



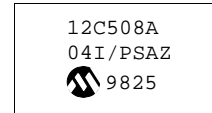
15.0 PACKAGING INFORMATION

15.1 Package Marking Information

8-Lead PDIP (300 mil)



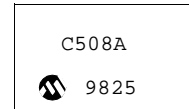
Example



8-Lead SOIC (150 mil)



Example



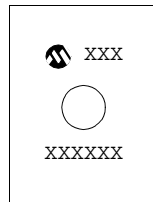
8-Lead SOIC (208 mil)



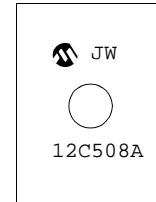
Example



8-Lead Windowed Ceramic Side Brazed (300 mil)



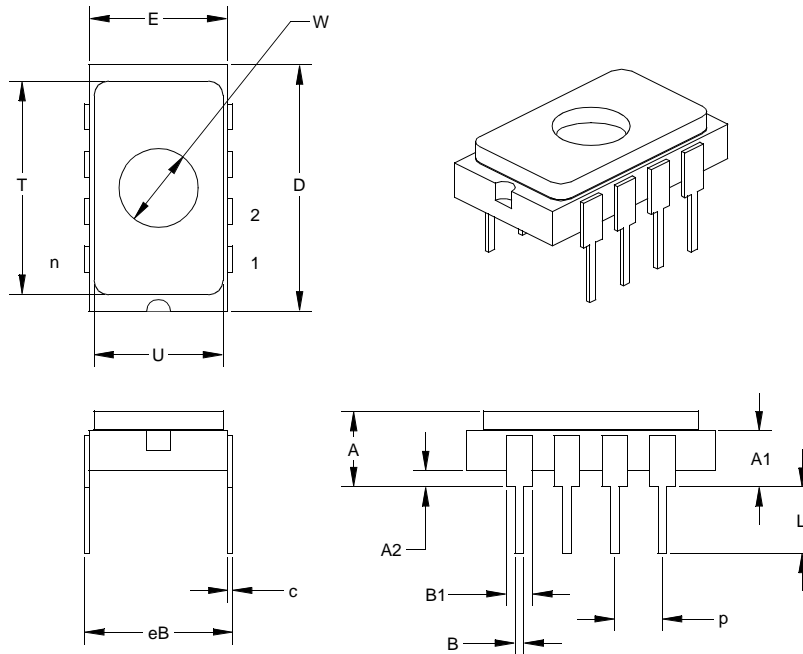
Example



Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured
		O = Outside Vendor
		C = 5" Line
		S = 6" Line
		H = 8" Line
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.	

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

Package Type: K04-084 8-Lead Ceramic Side Brazed Dual In-line with Window (JW) – 300 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		8			8	
Pitch	p	0.098	0.100	0.102	2.49	2.54	2.59
Lower Lead Width	B	0.016	0.018	0.020	0.41	0.46	0.51
Upper Lead Width	B1	0.050	0.055	0.060	1.27	1.40	1.52
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.145	0.165	0.185	3.68	4.19	4.70
Top of Body to Seating Plane	A1	0.103	0.123	0.143	2.62	3.12	3.63
Base to Seating Plane	A2	0.025	0.035	0.045	0.64	0.89	1.14
Tip to Seating Plane	L	0.130	0.140	0.150	3.30	3.56	3.81
Package Length	D	0.510	0.520	0.530	12.95	13.21	13.46
Package Width	E	0.280	0.290	0.300	7.11	7.37	7.62
Overall Row Spacing	eB	0.310	0.338	0.365	7.87	8.57	9.27
Window Diameter	W	0.161	0.166	0.171	4.09	4.22	4.34
Lid Length	T	0.440	0.450	0.460	11.18	11.43	11.68
Lid Width	U	0.260	0.270	0.280	6.60	6.86	7.11

* Controlling Parameter.

NOTES:

Note the following details of the code protection feature on PICmicro® MCUs.

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable”.
- Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our product.

If you have any further questions about this matter, please contact the local sales office nearest to you.

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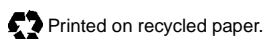
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