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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 5 |
| Program Memory Size | 1.5KB (1K x 12) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 41 x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 8-SOIC (0.209", 5.30mm Width) |
| Supplier Device Package | 8-SOIJ |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic12c509t-04e-sm |

## 2.0 PIC12C5XX DEVICE VARIETIES

A variety of packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC12C5XX Product Identification System at the back of this data sheet to specify the correct part number.

### 2.1 UV Erasable Devices

The UV erasable version, offered in ceramic side brazed package, is optimal for prototype development and pilot programs.

The UV erasable version can be erased and reprogrammed to any of the configuration modes.

| | |
|---|---|
| **Note:** | Please note that erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be saved prior to erasing the part. |

Microchip's PICSTART® PLUS and PRO MATE® programmers all support programming of the PIC12C5XX. Third party programmers also are available; refer to the *Microchip Third Party Guide* for a list of sources.

### 2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates or small volume applications.

The OTP devices, packaged in plastic packages permit the user to program them once. In addition to the program memory, the configuration bits must also be programmed.

### 2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

### 2.4 Serialized Quick-Turnaround Production (SQTP℠) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

### 2.5 Read Only Memory (ROM) Device

Microchip offers masked ROM to give the customer a low cost option for high volume, mature products.

**NOTES:**

## 3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC12C5XX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC12C5XX uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12-bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (1µs @ 4MHz) except for program branches.

The table below lists program memory (EPROM), data memory (RAM), ROM memory, and non-volatile (EEPROM) for each device.

| Device | Memory | | | |
|---|---|---|---|---|
| | EPROM Program | ROM Program | RAM Data | EEPROM Data |
| PIC12C508 | 512 x 12 | | 25 | |
| PIC12C509 | 1024 x 12 | | 41 | |
| PIC12C508A | 512 x 12 | | 25 | |
| PIC12C509A | 1024 x 12 | | 41 | |
| PIC12CR509A | | 1024 x 12 | 41 | |
| PIC12CE518 | 512 x 12 | | 25 x 8 | 16 x 8 |
| PIC12CE519 | 1024 x 12 | | 41 x 8 | 16 x 8 |

The PIC12C5XX can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC12C5XX has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC12C5XX simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC12C5XX device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit borrow}}$ out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1.

### 4.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status, and the page preselect bit for program memories larger than 512 words.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS register because these instructions do not affect the Z, DC or C bits from the STATUS register. For other instructions, which do affect STATUS bits, see Instruction Set Summary.

**FIGURE 4-4: STATUS REGISTER (ADDRESS:03h)**

| R/W-0 | R/W-0 | R/W-0 | R-1 | R-1 | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| GPWUF | — | PA0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C |
| bit7 | 6 | 5 | 4 | 3 | 2 | 1 | bit0 |

R = Readable bit
W = Writable bit
- n = Value at POR reset

bit 7: **GPWUF**: GPIO reset bit
1 = Reset due to wake-up from SLEEP on pin change
0 = After power up or other reset

bit 6: **Unimplemented**

bit 5: **PA0**: Program page preselect bits
1 = Page 1 (200h - 3FFh) - PIC12C509, PIC12C509A, PIC12CR509A and PIC12CE519
0 = Page 0 (000h - 1FFh) - PIC12C5XX
Each page is 512 bytes.
Using the PA0 bit as a general purpose read/write bit in devices which do not use it for program page preselect is not recommended since this may affect upward compatibility with future products.

bit 4: **$\overline{TO}$**: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: **$\overline{PD}$**: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (for `ADDWF` and `SUBWF` instructions)
**ADDWF**
1 = A carry from the 4th low order bit of the result occurred
0 = A carry from the 4th low order bit of the result did not occur
**SUBWF**
1 = A borrow from the 4th low order bit of the result did not occur
0 = A borrow from the 4th low order bit of the result occurred

bit 0: **C**: Carry/$\overline{borrow}$ bit (for `ADDWF`, `SUBWF` and `RRF`, `RLF` instructions)

| **ADDWF** | **SUBWF** | **RRF or RLF** |
|---|---|---|
| 1 = A carry occurred | 1 = A borrow did not occur | Load bit with LSB or MSB, respectively |
| 0 = A carry did not occur | 0 = A borrow occurred | |

### 4.4 OPTION Register

The OPTION register is a 8-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the `OPTION` instruction, the contents of the W register will be transferred to the OPTION register. A RESET sets the OPTION<7:0> bits.

| | |
|---|---|
| **Note:** | If TRIS bit is set to '0', the wake-up on change and pull-up functions are disabled for that pin; i.e., note that TRIS overrides OPTION control of $\overline{\text{GPPU}}$ and $\overline{\text{GPWU}}$. |
| **Note:** | If the T0CS bit is set to '1', GP2 is forced to be an input even if TRIS GP2 = '0'. |

**FIGURE 4-5: OPTION REGISTER**

| W-1 | W-1 | W-1 | W-1 | W-1 | W-1 | W-1 | W-1 |
|---|---|---|---|---|---|---|---|
| $\overline{\text{GPWU}}$ | $\overline{\text{GPPU}}$ | T0CS | T0SE | PSA | PS2 | PS1 | PS0 |
| bit7 | 6 | 5 | 4 | 3 | 2 | 1 | bit0 |

W = Writable bit
U = Unimplemented bit
- n = Value at POR reset
Reference Table 4-1 for other resets.

bit 7: **$\overline{\text{GPWU}}$:** Enable wake-up on pin change (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 6: **$\overline{\text{GPPU}}$**: Enable weak pull-ups (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 5: **T0CS**: Timer0 clock source select bit
1 = Transition on T0CKI pin
0 = Transition on internal instruction cycle clock, Fosc/4

bit 4: **T0SE**: Timer0 source edge select bit
1 = Increment on high to low transition on the T0CKI pin
0 = Increment on low to high transition on the T0CKI pin

bit 3: **PSA**: Prescaler assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0: **PS2:PS0**: Prescaler rate select bits

| Bit Value | Timer0 Rate | WDT Rate |
|---|---|---|
| 000 | 1 : 2 | 1 : 1 |
| 001 | 1 : 4 | 1 : 2 |
| 010 | 1 : 8 | 1 : 4 |
| 011 | 1 : 16 | 1 : 8 |
| 100 | 1 : 32 | 1 : 16 |
| 101 | 1 : 64 | 1 : 32 |
| 110 | 1 : 128 | 1 : 64 |
| 111 | 1 : 256 | 1 : 128 |

**NOTES:**

**FIGURE 6-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE**

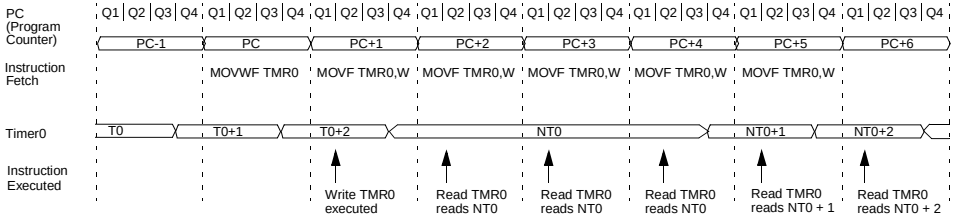



**FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2**

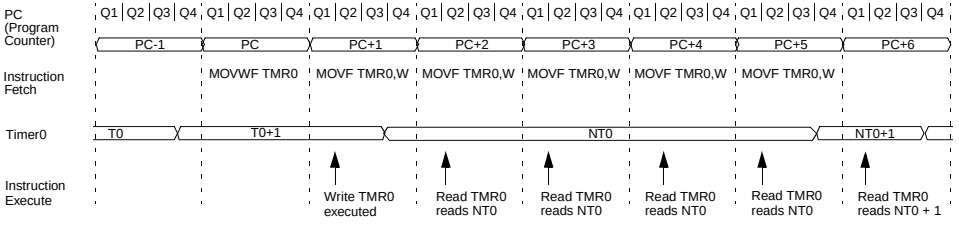



**TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-On Reset | Value on All Other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 01h | TMR0 | Timer0 - 8-bit real-time clock/counter | | | | | | | | xxxx xxxx | uuuu uuuu |
| N/A | OPTION | $\overline{GPWU}$ | $\overline{GPPU}$ | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| N/A | TRIS | — | — | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | --11 1111 | --11 1111 |

Legend: Shaded cells not used by Timer0, - = unimplemented, x = unknown, u = unchanged,

**FIGURE 7-3: DATA TRANSFER SEQUENCE ON THE SERIAL BUS**

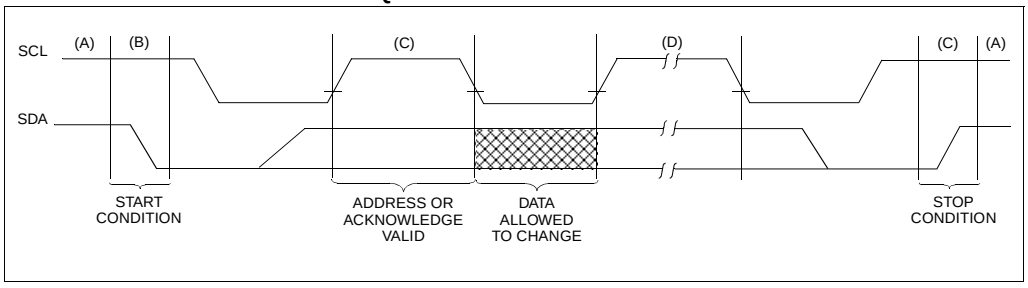
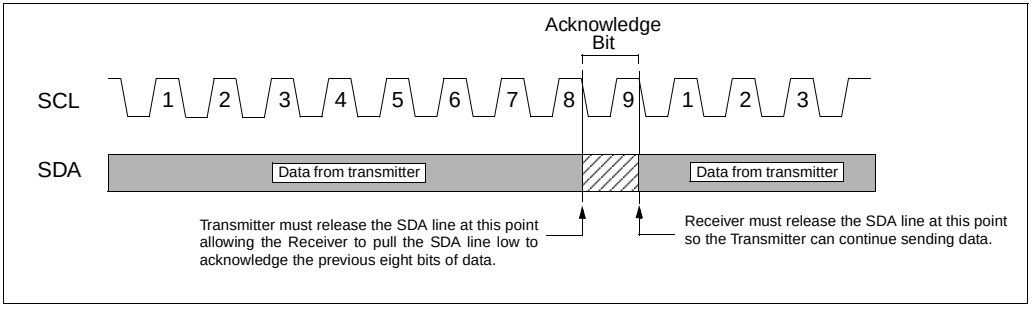



**FIGURE 7-4: ACKNOWLEDGE TIMING**

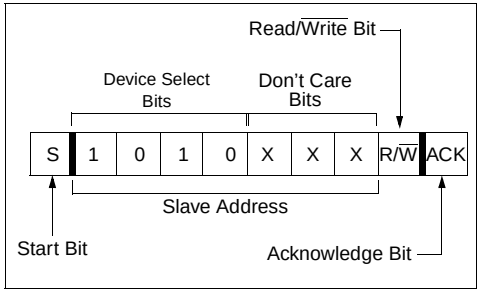



## 7.2 Device Addressing

After generating a START condition, the bus master transmits a control byte consisting of a slave address and a Read/$\overline{\text{Write}}$ bit that indicates what type of operation is to be performed. The slave address consists of a 4-bit device code (1010) followed by three don't care bits.

The last bit of the control byte determines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. (Figure 7-5). The bus is monitored for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

**FIGURE 7-5: CONTROL BYTE FORMAT**



### 8.2.5 INTERNAL 4 MHz RC OSCILLATOR

The internal RC oscillator provides a fixed 4 MHz (nominal) system clock at VDD = 5V and 25°C, see "Electrical Specifications" section for information on variation over voltage and temperature.

In addition, a calibration instruction is programmed into the top of memory which contains the calibration value for the internal RC oscillator. This location is never code protected regardless of the code protect settings. This value is programmed as a `MOVLW XX` instruction where XX is the calibration value, and is placed at the reset vector. This will load the W register with the calibration value upon reset and the PC will then roll over to the users program at address 0x000. The user then has the option of writing the value to the OSCCAL Register (05h) or ignoring it.

OSCCAL, when written to with the calibration value, will "trim" the internal oscillator to remove process variation from the oscillator frequency. .

| | |
|---|---|
| **Note:** | Please note that erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be read prior to erasing the part. so it can be reprogrammed correctly later. |

For the PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, and PIC12CR509A, bits <7:2>, CAL5-CAL0 are used for calibration. Adjusting CAL5-0 from 000000 to 111111 yields a higher clock speed. Note that bits 1 and 0 of OSCCAL are unimplemented and should be written as 0 when modifying OSCCAL for compatibility with future devices.

For the PIC12C508 and PIC12C509, the upper 4 bits of the register are used. Writing a larger value in this location yields a higher clock speed.

## 8.3 RESET

The device differentiates between various kinds of reset:

a) Power on reset (POR)

b) $\overline{\text{MCLR}}$ reset during normal operation

c) $\overline{\text{MCLR}}$ reset during SLEEP

d) WDT time-out reset during normal operation

e) WDT time-out reset during SLEEP

f) Wake-up from SLEEP on pin change

Some registers are not reset in any way; they are unknown on POR and unchanged in any other reset. Most other registers are reset to "reset state" on power-on reset (POR), $\overline{\text{MCLR}}$, WDT or wake-up on pin change reset during normal operation. They are not affected by a WDT reset during SLEEP or $\overline{\text{MCLR}}$ reset during SLEEP, since these resets are viewed as resumption of normal operation. The exceptions to this are $\overline{\text{TO}}$, $\overline{\text{PD}}$, and GPWUF bits. They are set or cleared differently in different reset situations. These bits are used in software to determine the nature of reset. See Table 8-3 for a full description of reset states of all registers.

### 8.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, a time-out period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see DC specs).

Under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

### 8.6.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The SLEEP instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT wake-up reset.

**FIGURE 8-12: WATCHDOG TIMER BLOCK DIAGRAM**

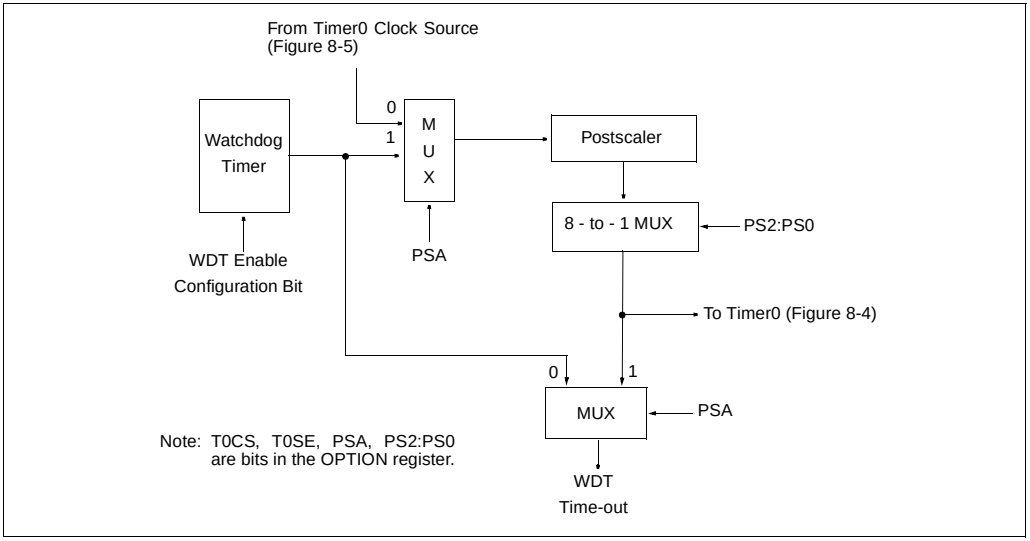



**TABLE 8-6: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-On Reset | Value on All Other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| N/A | OPTION | $\overline{GPWU}$ | $\overline{GPPU}$ | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |

Legend: Shaded boxes = Not used by Watchdog Timer, – = unimplemented, read as '0', u = unchanged

# 10.0 DEVELOPMENT SUPPORT

## 10.1 Development Tools

The PICmicro® microcontrollers are supported with a full range of hardware and software development tools:

- MPLAB™-ICE Real-Time In-Circuit Emulator
- ICEPIC™ Low-Cost PIC16C5X and PIC16CXXX In-Circuit Emulator
- PRO MATE® II Universal Programmer
- PICSTART® Plus Entry-Level Prototype Programmer
- SIMICE
- PICDEM-1 Low-Cost Demonstration Board
- PICDEM-2 Low-Cost Demonstration Board
- PICDEM-3 Low-Cost Demonstration Board
- MPASM Assembler
- MPLAB™ SIM Software Simulator
- MPLAB-C17 (C Compiler)
- Fuzzy Logic Development System (*fuzzy*TECH®–MP)
- KEELOQ® Evaluation Kits and Programmer

## 10.2 MPLAB-ICE: High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB-ICE Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro® microcontrollers (MCUs). MPLAB-ICE is supplied with the MPLAB Integrated Development Environment (IDE), which allows editing, “make” and download, and source debugging from a single environment.

Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB-ICE allows expansion to support all new Microchip microcontrollers.

The MPLAB-ICE Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC compatible 386 (and higher) machine platform and Microsoft Windows® 3.x or Windows 95 environment were chosen to best make these features available to you, the end user.

MPLAB-ICE is available in two versions. MPLAB-ICE 1000 is a basic, low-cost emulator system with simple trace capabilities. It shares processor modules with the MPLAB-ICE 2000. This is a full-featured emulator system with enhanced trace, trigger, and data monitoring features. Both systems will operate across the entire operating speed range of the PICmicro® MCU.

## 10.3 ICEPIC: Low-Cost PICmicro® In-Circuit Emulator

ICEPIC is a low-cost in-circuit emulator solution for the Microchip PIC12CXXX, PIC16C5X and PIC16CXXX families of 8-bit OTP microcontrollers.

ICEPIC is designed to operate on PC-compatible machines ranging from 386 through Pentium™ based machines under Windows 3.x, Windows 95, or Windows NT environment. ICEPIC features real time, non-intrusive emulation.

## 10.4 PRO MATE II: Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode. PRO MATE II is CE compliant.

The PRO MATE II has programmable $V_{DD}$ and $V_{PP}$ supplies which allows it to verify programmed memory at $V_{DD}$ min and $V_{DD}$ max for maximum reliability. It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode the PRO MATE II can read, verify or program PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices. It can also set configuration and code-protect bits in this mode.

## 10.5 PICSTART Plus Entry Level Development System

The PICSTART programmer is an easy-to-use, low-cost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. PICSTART Plus is not recommended for production programming.

PICSTART Plus supports all PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices with up to 40 pins. Larger pin count devices such as the PIC16C923, PIC16C924 and PIC17C756 may be supported with an adapter socket. PICSTART Plus is CE compliant.

### 10.10 MPLAB Integrated Development Environment Software

The MPLAB IDE Software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a windows based application which contains:

- A full featured editor
- Three operating modes
  - editor
  - emulator
  - simulator
- A project manager
- Customizable tool bar and key mapping
- A status bar with project information
- Extensive on-line help

MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PICmicro® tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file

The ability to use MPLAB with Microchip's simulator allows a consistent platform and the ability to easily switch from the low cost simulator to the full featured emulator with minimal retraining due to development tools.

### 10.11 Assembler (MPASM)

The MPASM Universal Macro Assembler is a PC-hosted symbolic assembler. It supports all microcontroller series including the PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX, and PIC17CXX families.

MPASM offers full featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from MPLAB-ICE, Microchip's Universal Emulator System.

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro assembly capability.
- Produces all the files (Object, Listing, Symbol, and special) required for symbolic debug with Microchip's emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a rich directive language to support programming of the PICmicro®. Directives are helpful in making the development of your assemble source code shorter and more maintainable.

### 10.12 Software Simulator (MPLAB-SIM)

The MPLAB-SIM Software Simulator allows code development in a PC host environment. It allows the user to simulate the PICmicro® series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in; single step, execute until break, or in a trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C17 and MPASM. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

### 10.13 MPLAB-C17 Compiler

The MPLAB-C17 Code Development System is a complete ANSI 'C' compiler and integrated development environment for Microchip's PIC17CXXX family of microcontrollers. The compiler provides powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compiler provides symbol information that is compatible with the MPLAB IDE memory display.

### 10.14 Fuzzy Logic Development System (*fuzzy*TECH-MP)

*fuzzy*TECH-MP fuzzy logic development tool is available in two versions - a low cost introductory version, MP Explorer, for designers to gain a comprehensive working knowledge of fuzzy logic system design; and a full-featured version, *fuzzy*TECH-MP, Edition for implementing more complex systems.

Both versions include Microchip's *fuzzy*LAB™ demonstration board for hands-on experience with fuzzy logic systems implementation.

### 10.15 SEEVAL® Evaluation and Programming System

The SEEVAL SEEPROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials™ and secure serials. The Total Endurance™ Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

### 11.1 DC CHARACTERISTICS: PIC12C508/509 (Commercial, Industrial, Extended)

| DC Characteristics<br>Power Supply Pins | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C (commercial)<br>–40°C ≤ TA ≤ +85°C (industrial)<br>–40°C ≤ TA ≤ +125°C (extended) | | | | |
|---|---|---|---|---|---|---|---|
| **Parm No.** | **Characteristic** | **Sym** | **Min** | **Typ(1)** | **Max** | **Units** | **Conditions** |
| D001 | **Supply Voltage** | VDD | 2.5 | | 5.5 | V | FOSC = DC to 4 MHz (Commercial/ Industrial) |
| | | | 3.0 | | 5.5 | V | FOSC = DC to 4 MHz (Extended) |
| D002 | **RAM Data Retention Voltage(2)** | VDR | | 1.5* | | V | Device in SLEEP mode |
| D003 | **VDD Start Voltage to ensure Power-on Reset** | VPOR | | VSS | | V | See section on Power-on Reset for details |
| D004 | **VDD Rise Rate to ensure Power-on Reset** | SVDD | 0.05 * | | | V/ms | See section on Power-on Reset for details |
| | **Supply Current(3)** | | | | | | |
| D010 | | IDD | — | .78 | 2.4 | mA | XT and EXTRC options (4)<br>FOSC = 4 MHz, VDD = 5.5V |
| D010C | | | — | 1.1 | 2.4 | mA | INTRC Option<br>FOSC = 4 MHz, VDD = 5.5V |
| D010A | | | — | 10 | 27 | µA | LP OPTION, Commercial Temperature<br>FOSC = 32 kHz, VDD = 3.0V, WDT disabled |
| | | | — | 14 | 35 | µA | LP OPTION, Industrial Temperature<br>FOSC = 32 kHz, VDD = 3.0V, WDT disabled |
| | | | — | 14 | 35 | µA | LP OPTION, Extended Temperature<br>FOSC = 32 kHz, VDD = 3.0V, WDT disabled |
| | **Power-Down Current (5)** | | | | | | |
| D020 | | IPD | — | 0.25 | 4 | µA | VDD = 3.0V, Commercial WDT disabled |
| D021 | | | — | 0.25 | 5 | µA | VDD = 3.0V, Industrial WDT disabled |
| D021B | | | — | 2 | 18 | µA | VDD = 3.0V, Extended WDT disabled |
| D022 | | ΔIWDT | — | 3.75 | 8 | µA | VDD = 3.0V, Commercial |
| | | | — | 3.75 | 9 | µA | VDD = 3.0V, Industrial |
| | | | — | 3.75 | 14 | µA | VDD = 3.0V, Extended |

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kOhm.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

## 11.2 DC CHARACTERISTICS: PIC12C508/509 (Commercial, Industrial, Extended)

| DC CHARACTERISTICS | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating temperature 0°C ≤ TA ≤ +70°C (commercial)<br>–40°C ≤ TA ≤ +85°C (industrial)<br>–40°C ≤ TA ≤ +125°C (extended)<br>Operating voltage VDD range as described in DC spec Section 11.1 and Section 11.2. | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Sym** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | **Input Low Voltage** | | | | | | |
| | I/O ports | VIL | | - | | | |
| D030 | with TTL buffer | | VSS | - | 0.8V | V | 4.5 < VDD ≤ 5.5V |
| | | | | - | 0.15VDD | V | otherwise |
| D031 | with Schmitt Trigger buffer | | VSS | - | 0.15VDD | V | |
| D032 | MCLR, GP2/T0CKI (in EXTRC mode) | | VSS | - | 0.15VDD | V | |
| D033 | OSC1 (EXTRC) (1) | | VSS | - | 0.15VDD | | |
| D033 | OSC1 (in XT and LP) | | VSS | - | 0.3VDD | V | Note1 |
| | **Input High Voltage** | | | | | | |
| | I/O ports | VIH | | - | | | |
| D040 | with TTL buffer | VSS | 2.0V | - | VDD | V | 4.5 ≤ VDD ≤ 5.5V |
| D040A | | | 0.25VDD + 0.8V | - | VDD | V | otherwise |
| D041 | with Schmitt Trigger buffer | | 0.85VDD | - | VDD | V | For entire VDD range |
| D042 | MCLR/GP2/T0CKI | | 0.85VDD | - | VDD | V | |
| D042A | OSC1 (XT and LP) | | 0.7VDD | - | VDD | V | Note1 |
| D043 | OSC1 (in EXTRC mode) | | 0.85VDD | - | VDD | V | |
| D070 | GPIO weak pull-up current | IPUR | 50 | 250 | 400 | µA | VDD = 5V, VPIN = VSS |
| | **Input Leakage Current (2, 3)** | | | | | | For VDD ≤5.5V |
| D060 | I/O ports | IIL | -1 | 0.5 | ±1 | µA | Vss ≤ VPIN ≤ VDD,<br>Pin at hi-impedance |
| D061 | MCLR, GP2/T0CKI | | 20 | 130 | 250 | µA | VPIN = VSS + 0.25V(2) |
| | | | | 0.5 | +5 | µA | VPIN = VDD |
| D063 | OSC1 | | -3 | 0.5 | +3 | µA | Vss ≤ VPIN ≤ VDD,<br>XT and LP options |
| | **Output Low Voltage** | | | | | | |
| D080 | I/O ports/CLKOUT | VOL | - | - | 0.6 | V | IOL = 8.7 mA, VDD = 4.5V |
| | **Output High Voltage** | | | | | | |
| D090 | I/O ports/CLKOUT (3) | VOH | VDD - 0.7 | - | - | V | IOH = -5.4 mA, VDD = 4.5V |
| | **Capacitive Loading Specs on Output Pins** | | | | | | |
| D100 | OSC2 pin | COSC2 | - | - | 15 | pF | In XT and LP modes when external clock is used to drive OSC1. |
| D101 | All I/O pins | CIO | - | - | 50 | pF | |

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C5XX be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

**TABLE 11-5: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC12C508/C509**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C (commercial)<br>–40°C ≤ TA ≤ +85°C (industrial)<br>–40°C ≤ TA ≤ +125°C (extended)<br>Operating Voltage VDD range is described in Section 11.1 | | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter No.** | **Sym** | **Characteristic** | **Min** | **Typ(1)** | **Max** | **Units** | **Conditions** |
| 30 | TmcL | $\overline{\text{MCLR}}$ Pulse Width (low) | 2000* | — | — | ns | VDD = 5 V |
| 31 | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 9* | 18* | 30* | ms | VDD = 5 V (Commercial) |
| 32 | TDRT | Device Reset Timer Period(2) | 9* | 18* | 30* | ms | VDD = 5 V (Commercial) |
| 34 | TioZ | I/O Hi-impedance from $\overline{\text{MCLR}}$ Low | — | — | 2000* | ns | |

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 2: See Table 11-6.

**TABLE 11-6: DRT (DEVICE RESET TIMER PERIOD - PIC12C508/C509)**

| Oscillator Configuration | POR Reset | Subsequent Resets |
|---|---|---|
| IntRC & ExtRC | 18 ms (typical) | 300 µs (typical) |
| XT & LP | 18 ms (typical) | 18 ms (typical) |

**FIGURE 11-5: TIMER0 CLOCK TIMINGS - PIC12C508/C509**

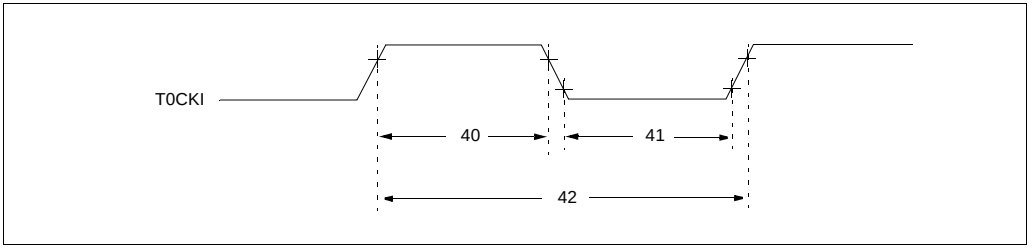



**TABLE 11-7: TIMER0 CLOCK REQUIREMENTS - PIC12C508/C509**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C (commercial)<br>–40°C ≤ TA ≤ +85°C (industrial)<br>–40°C ≤ TA ≤ +125°C (extended)<br>Operating Voltage VDD range is described in Section 11.1. |
|---|---|

| Parameter No. | Sym | Characteristic | Min | Typ(1) | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 40 | Tt0H | T0CKI High Pulse Width - No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | - With Prescaler | 10* | — | — | ns | |
| 41 | Tt0L | T0CKI Low Pulse Width - No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | - With Prescaler | 10* | — | — | ns | |
| 42 | Tt0P | T0CKI Period | 20 or $\frac{T_{CY} + 40}{N}$* | — | — | ns | Whichever is greater.<br>N = Prescale Value (1, 2, 4,..., 256) |

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**TABLE 12-1: DYNAMIC IDD (TYPICAL) - WDT ENABLED, 25°C**

| Oscillator | Frequency | VDD = 2.5V | VDD = 5.5V |
|---|---|---|---|
| External RC | 4 MHz | 250 µA* | 780 µA* |
| Internal RC | 4 MHz | 420 µA | 1.1 mA |
| XT | 4 MHz | 251 µA | 780 µA |
| LP | 32 KHz | 15 µA | 37 µA |

*Does not include current through external R&C.

**FIGURE 12-3: WDT TIMER TIME-OUT PERIOD VS. VDD**

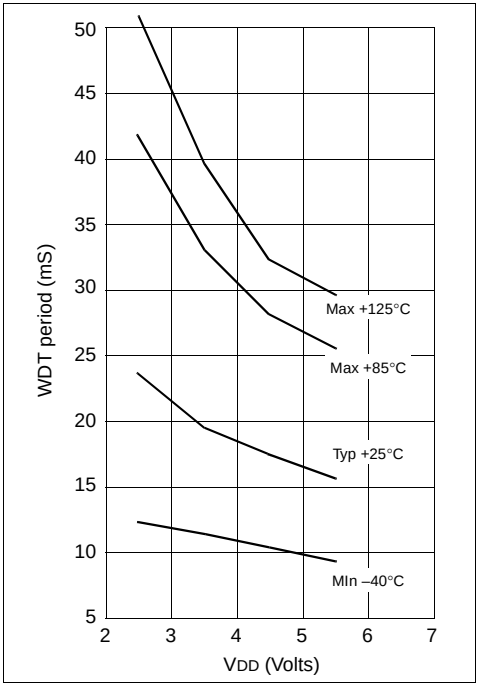
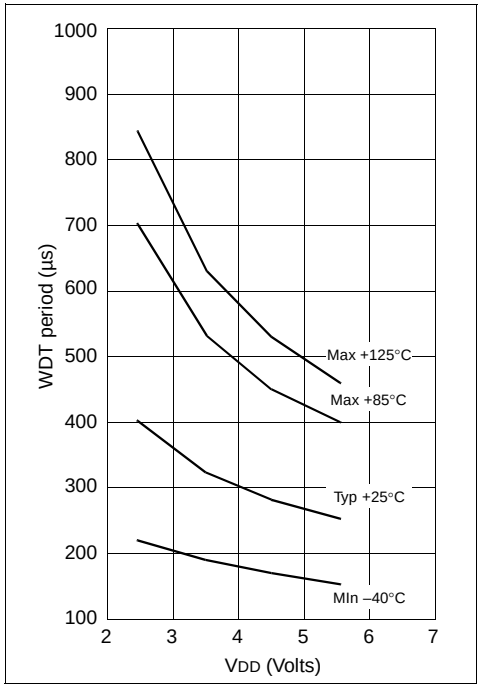



**FIGURE 12-4: SHORT DRT PERIOD VS. VDD**



## 13.2 DC CHARACTERISTICS: PIC12LC508A/509A (Commercial, Industrial) PIC12LCE518/519 (Commercial, Industrial) PIC12LCR509A (Commercial, Industrial)

| DC Characteristics Power Supply Pins | | | Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) | | | | |
|---|---|---|---|---|---|---|---|
| **Parm No.** | **Characteristic** | **Sym** | **Min** | **Typ(1)** | **Max** | **Units** | **Conditions** |
| D001 | **Supply Voltage** | VDD | 2.5 | | 5.5 | V | FOSC = DC to 4 MHz (Commercial/ Industrial) |
| D002 | **RAM Data Retention Voltage(2)** | VDR | | 1.5* | | V | Device in SLEEP mode |
| D003 | **VDD Start Voltage to ensure Power-on Reset** | VPOR | | VSS | | V | See section on Power-on Reset for details |
| D004 | **VDD Rise Rate to ensure Power-on Reset** | SVDD | 0.05* | | | V/ms | See section on Power-on Reset for details |
| D010 | **Supply Current(3)** | IDD | — | 0.4 | 0.8 | mA | XT and EXTRC options (Note 4) FOSC = 4 MHz, VDD = 2.5V |
| D010C | | | — | 0.4 | 0.8 | mA | INTRC Option FOSC = 4 MHz, VDD = 2.5V |
| D010A | | | — | 15 | 23 | µA | LP OPTION, Commercial Temperature FOSC = 32 kHz, VDD = 2.5V, WDT disabled |
| | | | — | 15 | 31 | µA | LP OPTION, Industrial Temperature FOSC = 32 kHz, VDD = 2.5V, WDT disabled |
| D020 | **Power-Down Current (5)** | IPD | | | | | |
| D021 | | | — | 0.2 | 3 | µA | VDD = 2.5V, Commercial |
| D021B | | | — | 0.2 | 4 | µA | VDD = 2.5V, Industrial |
| | | ΔIWDT | — | 2.0 | 4 | mA | VDD = 2.5V, Commercial |
| | | | | 2.0 | 5 | mA | VDD = 2.5V, Industrial |

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kOhm.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

## 13.4 DC CHARACTERISTICS: PIC12LC508A/509A (Commercial, Industrial) PIC12LC518/519 (Commercial, Industrial) PIC12LCR509A (Commercial, Industrial)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating temperature 0°C ≤ TA ≤ +70°C (commercial)<br>–40°C ≤ TA ≤ +85°C (industrial)<br>Operating voltage VDD range as described in DC spec Section 13.1 and Section 13.2. | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Sym** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | **Input Low Voltage** | | | | | | |
| | I/O ports | VIL | | | | | |
| D030 | with TTL buffer | | VSS | - | 0.8V | V | For 4.5V ≤ VDD ≤ 5.5V |
| | | | VSS | - | 0.15VDD | V | otherwise |
| D031 | with Schmitt Trigger buffer | | VSS | - | 0.2VDD | V | |
| D032 | $\overline{MCLR}$, GP2/T0CKI (in EXTRC mode) | | VSS | - | 0.2VDD | V | |
| D033 | OSC1 (in EXTRC mode) | | VSS | - | 0.2VDD | V | Note 1 |
| D033 | OSC1 (in XT and LP) | | VSS | - | 0.3VDD | V | Note 1 |
| | **Input High Voltage** | | | | | | |
| | I/O ports | VIH | | - | | | |
| D040 | with TTL buffer | | 0.25VDD + 0.8V | - | VDD | V | 4.5V ≤ VDD ≤ 5.5V |
| D040A | | | 2.0V | - | VDD | V | otherwise |
| D041 | with Schmitt Trigger buffer | | 0.8VDD | - | VDD | V | For entire VDD range |
| D042 | $\overline{MCLR}$, GP2/T0CKI | | 0.8VDD | - | VDD | V | |
| D042A | OSC1 (XT and LP) | | 0.7VDD | - | VDD | V | Note 1 |
| D043 | OSC1 (in EXTRC mode) | | 0.9VDD | - | VDD | V | |
| D070 | GPIO weak pull-up current (Note 4) | IPUR | 30 | 250 | 400 | µA | VDD = 5V, VPIN = VSS |
| | $\overline{MCLR}$ pull-up current | - | - | - | 30 | µA | VDD = 5V, VPIN = VSS |
| | **Input Leakage Current** (Notes 2, 3) | | | | | | |
| D060 | I/O ports | IIL | - | - | ±1 | µA | Vss ≤ VPIN ≤ VDD, Pin at hi-impedance |
| D061 | T0CKI | | - | - | ±5 | µA | Vss ≤ VPIN ≤ VDD |
| D063 | OSC1 | | - | - | ±5 | µA | Vss ≤ VPIN ≤ VDD, XT and LP osc configuration |
| | **Output Low Voltage** | | | | | | |
| D080 | I/O ports | VOL | - | - | 0.6 | V | IOL = 8.5 mA, VDD = 4.5V, –40°C to +85°C |
| D080A | | | - | - | 0.6 | V | IOL = 7.0 mA, VDD = 4.5V, –40°C to +125°C |
| | **Output High Voltage** | | | | | | |
| D090 | I/O ports (Note 3) | VOH | VDD - 0.7 | - | - | V | IOH = -3.0 mA, VDD = 4.5V, –40°C to +85°C |
| D090A | | | VDD - 0.7 | - | - | V | IOH = -2.5 mA, VDD = 4.5V, –40°C to +125°C |
| | **Capacitive Loading Specs on Output Pins** | | | | | | |
| D100 | OSC2 pin | COSC2 | - | - | 15 | pF | In XT and LP modes when external clock is used to drive OSC1. |
| D101 | All I/O pins | CIO | - | - | 50 | pF | |

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C5XX be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: This spec. applies when GP3/$\overline{MCLR}$ is configured as $\overline{MCLR}$. The leakage current of the $\overline{MCLR}$ circuit is higher than the standard I/O logic.

**FIGURE 14-13: TYPICAL IPD VS. VDD, WATCHDOG DISABLED (25°C)**

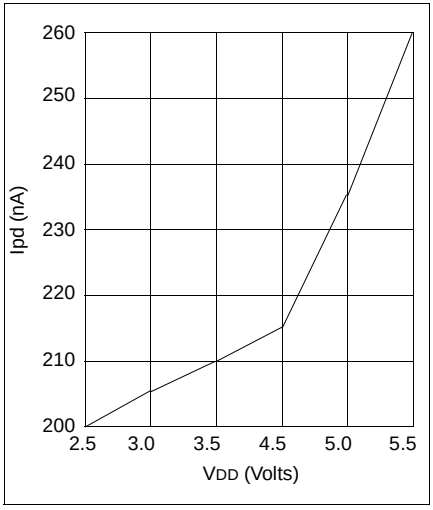



**FIGURE 14-14: VTH (INPUT THRESHOLD VOLTAGE) OF GPIO PINS VS. VDD**