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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	16 x 8
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12ce518-04-p

PIC12C5XX

Pin Diagram - PIC12C508/509

PDIP, 208 mil SOIC, Windowed Ceramic Side Brazed

V$_{DD}$ →	1	8 ← V$_{SS}$
GP5/OSC1/CLKIN ↔	2	7 ↔ GP0
GP4/OSC2 ↔	3	6 ↔ GP1
GP3/$\overline{MCLR}$/V$_{PP}$ →	4	5 ↔ GP2/T0CKI

PIC12C508
PIC12C509

Pin Diagram - PIC12C508A/509A, PIC12CE518/519

PDIP, 150 & 208 mil SOIC, Windowed CERDIP

V$_{DD}$ →	1	8 ← V$_{SS}$
GP5/OSC1/CLKIN ↔	2	7 ↔ GP0
GP4/OSC2 ↔	3	6 ↔ GP1
GP3/$\overline{MCLR}$/V$_{PP}$ →	4	5 ↔ GP2/T0CKI

PIC12C508A
PIC12C509A
PIC12CE518
PIC12CE519

Pin Diagram - PIC12CR509A

PDIP, 150 & 208 mil SOIC

V$_{DD}$ →	1	8 ← V$_{SS}$
GP5/OSC1/CLKIN ↔	2	7 ↔ GP0
GP4/OSC2 ↔	3	6 ↔ GP1
GP3/$\overline{MCLR}$/V$_{PP}$ →	4	5 ↔ GP2/T0CKI

PIC12CR509A

Device Differences

Device	Voltage Range	Oscillator	Oscillator Calibration[2] (Bits)	Process Technology (Microns)
PIC12C508A	3.0-5.5	See Note 1	6	0.7
PIC12LC508A	2.5-5.5	See Note 1	6	0.7
PIC12C508	2.5-5.5	See Note 1	4	0.9
PIC12C509A	3.0-5.5	See Note 1	6	0.7
PIC12LC509A	2.5-5.5	See Note 1	6	0.7
PIC12C509	2.5-5.5	See Note 1	4	0.9
PIC12CR509A	2.5-5.5	See Note 1	6	0.7
PIC12CE518	3.0-5.5	-	6	0.7
PIC12LCE518	2.5-5.5	-	6	0.7
PIC12CE519	3.0-5.5	-	6	0.7
PIC12LCE519	2.5-5.5	-	6	0.7

Note 1: If you change from the PIC12C50X to the PIC12C50XA or to the PIC12CR50XA, please verify oscillator characteristics in your application.

Note 2: See Section 7.2.5 for OSCCAL implementation differences.

2.0 PIC12C5XX DEVICE VARIETIES

A variety of packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC12C5XX Product Identification System at the back of this data sheet to specify the correct part number.

2.1 UV Erasable Devices

The UV erasable version, offered in ceramic side brazed package, is optimal for prototype development and pilot programs.

The UV erasable version can be erased and reprogrammed to any of the configuration modes.

Note:	Please note that erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be saved prior to erasing the part.

Microchip's PICSTART® PLUS and PRO MATE® programmers all support programming of the PIC12C5XX. Third party programmers also are available; refer to the *Microchip Third Party Guide* for a list of sources.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates or small volume applications.

The OTP devices, packaged in plastic packages permit the user to program them once. In addition to the program memory, the configuration bits must also be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround Production (SQTP^SM) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

2.5 Read Only Memory (ROM) Device

Microchip offers masked ROM to give the customer a low cost option for high volume, mature products.

3.0   ARCHITECTURAL OVERVIEW

The high performance of the PIC12C5XX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC12C5XX uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12-bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (1µs @ 4MHz) except for program branches.

The table below lists program memory (EPROM), data memory (RAM), ROM memory, and non-volatile (EEPROM) for each device.

Device	Memory			
	EPROM Program	ROM Program	RAM Data	EEPROM Data
PIC12C508	512 x 12		25	
PIC12C509	1024 x 12		41	
PIC12C508A	512 x 12		25	
PIC12C509A	1024 x 12		41	
PIC12CR509A		1024 x 12	41	
PIC12CE518	512 x 12		25 x 8	16 x 8
PIC12CE519	1024 x 12		41 x 8	16 x 8

The PIC12C5XX can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC12C5XX has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC12C5XX simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC12C5XX device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1.

PIC12C5XX

3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1, and the instruction is fetched from program memory and latched into instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2 and Example 3-1.
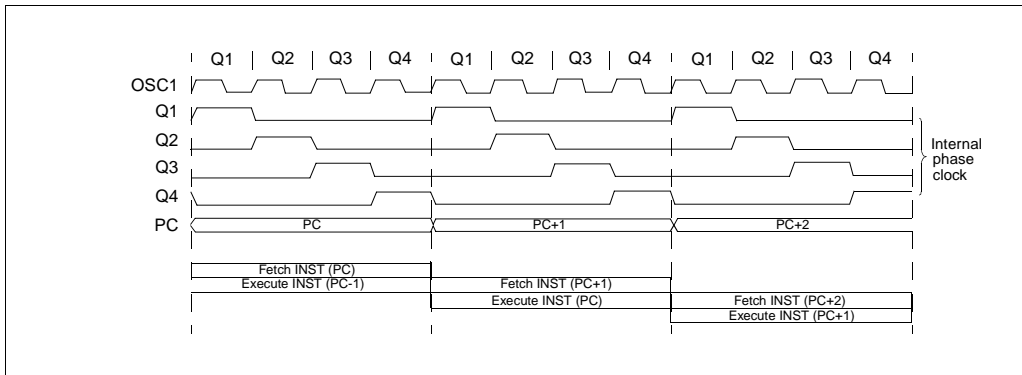
3.2 Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 3-1).
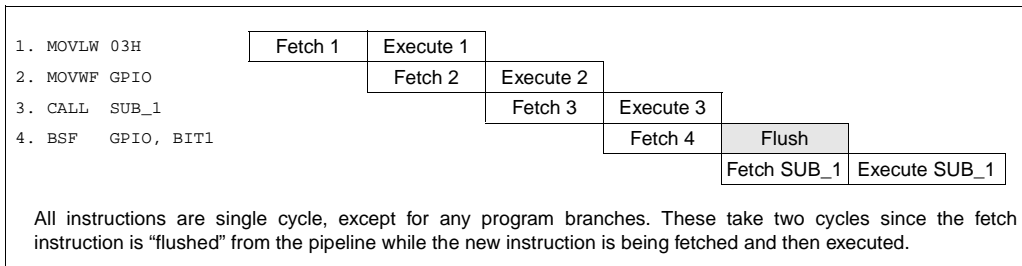
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2:   CLOCK/INSTRUCTION CYCLE

EXAMPLE 3-1:   INSTRUCTION PIPELINE FLOW

All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

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PIC12C5XX

4.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status, and the page preselect bit for program memories larger than 512 words.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u uluu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS register because these instructions do not affect the Z, DC or C bits from the STATUS register. For other instructions, which do affect STATUS bits, see Instruction Set Summary.

FIGURE 4-4: STATUS REGISTER (ADDRESS:03h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
GPWUF	—	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7	6	5	4	3	2	1	bit0

R = Readable bit
W = Writable bit
- n = Value at POR reset

bit 7: **GPWUF**: GPIO reset bit
1 = Reset due to wake-up from SLEEP on pin change
0 = After power up or other reset

bit 6: **Unimplemented**

bit 5: **PA0**: Program page preselect bits
1 = Page 1 (200h - 3FFh) - PIC12C509, PIC12C509A, PIC12CR509A and PIC12CE519
0 = Page 0 (000h - 1FFh) - PIC12C5XX
Each page is 512 bytes.
Using the PA0 bit as a general purpose read/write bit in devices which do not use it for program page preselect is not recommended since this may affect upward compatibility with future products.

bit 4: **$\overline{TO}$**: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: **$\overline{PD}$**: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (for `ADDWF` and `SUBWF` instructions)
ADDWF
1 = A carry from the 4th low order bit of the result occurred
0 = A carry from the 4th low order bit of the result did not occur
SUBWF
1 = A borrow from the 4th low order bit of the result did not occur
0 = A borrow from the 4th low order bit of the result occurred

bit 0: **C**: Carry/$\overline{borrow}$ bit (for `ADDWF`, `SUBWF` and `RRF`, `RLF` instructions)
ADDWF	**SUBWF**	**RRF or RLF**
1 = A carry occurred	1 = A borrow did not occur	Load bit with LSB or MSB, respectively
0 = A carry did not occur	0 = A borrow occurred	

NOTES:

FIGURE 8-8: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT
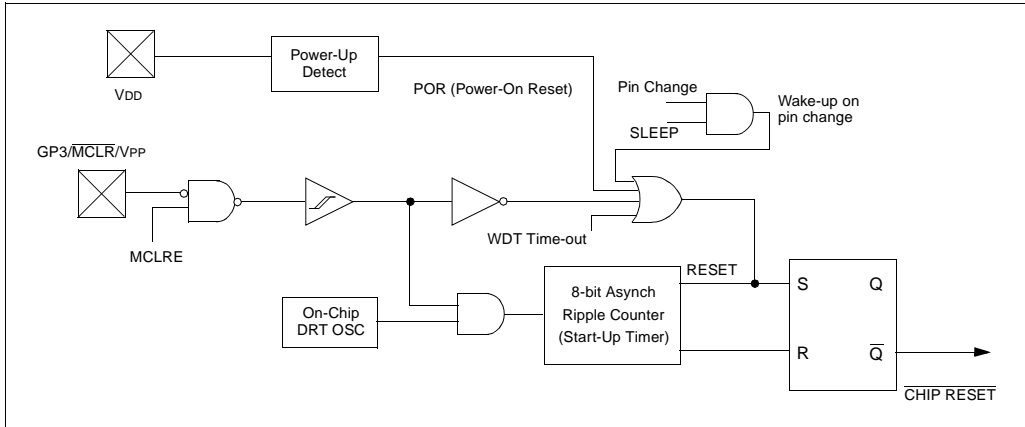
FIGURE 8-9: TIME-OUT SEQUENCE ON POWER-UP (MCLR PULLED LOW)

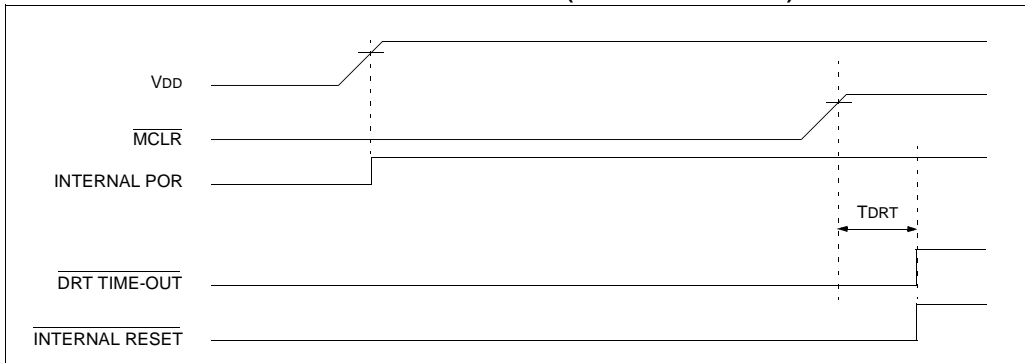**FIGURE 8-10: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): FAST VDD RISE TIME**
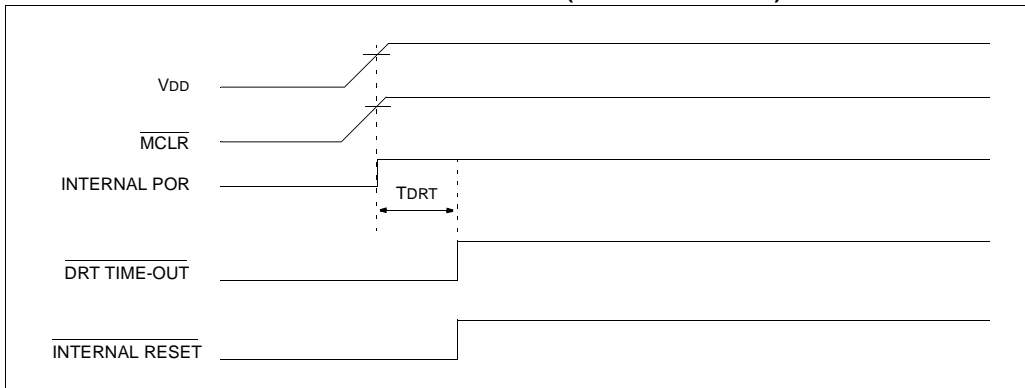
PIC12C5XX

FIGURE 8-11: **TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V$_{DD}$): SLOW V$_{DD}$ RISE TIME**

When V$_{DD}$ rises slowly, the T$_{DRT}$ time-out expires long before V$_{DD}$ has reached its final value. In this example, the chip will reset properly if, and only if, V1 ≥ V$_{DD}$ min.
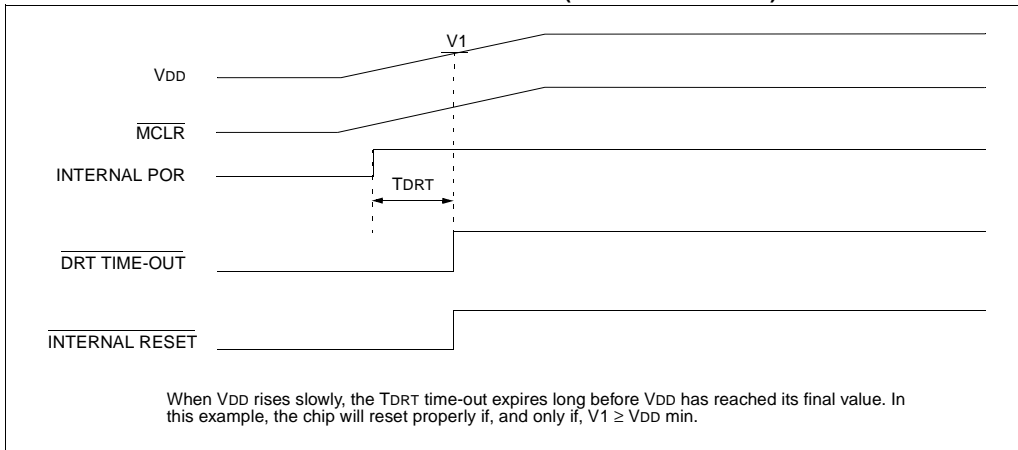
8.5   Device Reset Timer (DRT)

In the PIC12C5XX, DRT runs from RESET and varies based on oscillator selection (see Table 8-5.)

The DRT operates on an internal RC oscillator. The processor is kept in RESET as long as the DRT is active. The DRT delay allows V$_{DD}$ to rise above V$_{DD}$ min., and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the device in a RESET condition for approximately 18 ms after $\overline{\text{MCLR}}$ has reached a logic high (V$_{IH}$$\overline{\text{MCLR}}$) level. Thus, programming GP3/$\overline{\text{MCLR}}$/V$_{PP}$ as $\overline{\text{MCLR}}$ and using an external RC network connected to the $\overline{\text{MCLR}}$ input is not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications, as well as allowing the use of the GP3/$\overline{\text{MCLR}}$/V$_{PP}$ pin as a general purpose input.

The Device Reset time delay will vary from chip to chip due to V$_{DD}$, temperature, and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out. This is particularly important for applications using the WDT to wake from SLEEP mode automatically.

8.6   Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the external RC oscillator of the GP5/OSC1/CLKIN pin and the internal 4 MHz oscillator. That means that the WDT will run even if the main processor clock has been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT reset or wake-up reset generates a device RESET.

The $\overline{\text{TO}}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer reset.

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Section 8.1). Refer to the PIC12C5XX Programming Specifications to determine how to access the configuration word.

TABLE 8-5:   **DRT (DEVICE RESET TIMER PERIOD)**

Oscillator Configuration	POR Reset	Subsequent Resets
IntRC & ExtRC	18 ms (typical)	300 µs (typical)
XT & LP	18 ms (typical)	18 ms (typical)

8.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, a time-out period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see DC specs).

Under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

8.6.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The SLEEP instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT wake-up reset.
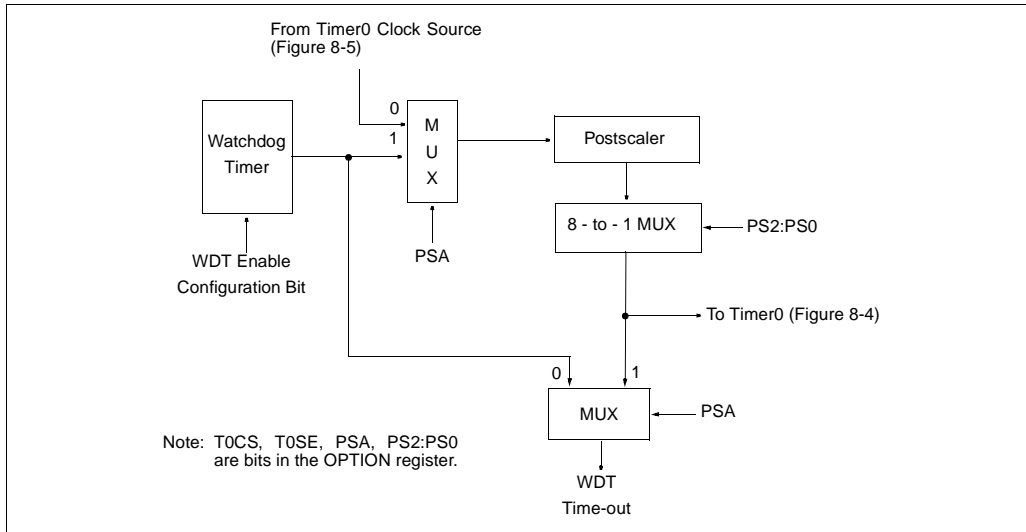
FIGURE 8-12: WATCHDOG TIMER BLOCK DIAGRAM

TABLE 8-6: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	OPTION	GPWU	GPPU	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: Shaded boxes = Not used by Watchdog Timer, − = unimplemented, read as '0', u = unchanged

9.0   INSTRUCTION SET SUMMARY

Each PIC12C5XX instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type, and one or more operands which further specify the operation of the instruction. The PIC12C5XX instruction set summary in Table 9-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 9-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 9-1:   OPCODE FIELD DESCRIPTIONS

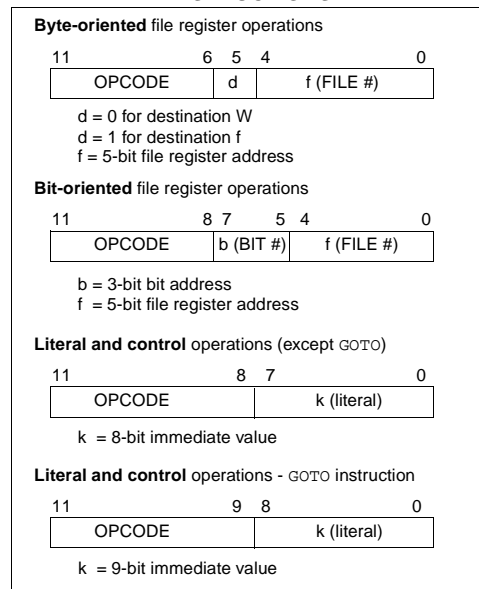| Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0 (store result in W) d = 1 (store result in file register 'f') Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
WDT	Watchdog Timer Counter
$\overline{TO}$	Time-Out bit
$\overline{PD}$	Power-Down bit
dest	Destination, either the W register or the specified register file location
[ ]	Options
( )	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
italics	User defined term (font is courier)

All instructions are executed within a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µs.

Figure 9-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

   0xhhh

where 'h' signifies a hexadecimal digit.

FIGURE 9-1:   GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations

11	6 5	4	0
OPCODE	d	f (FILE #)	

d = 0 for destination W
d = 1 for destination f
f = 5-bit file register address

Bit-oriented file register operations

11	8 7	5 4	0
OPCODE	b (BIT #)	f (FILE #)	

b = 3-bit bit address
f = 5-bit file register address

Literal and control operations (except GOTO)

11	8 7	0
OPCODE	k (literal)	

k = 8-bit immediate value

Literal and control operations - GOTO instruction

11	9 8	0
OPCODE	k (literal)	

k = 9-bit immediate value

ADDWF	Add W and f
Syntax:	[*label*] ADDWF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(W) + (f) $\rightarrow$ (dest)
Status Affected:	C, DC, Z
Encoding:	`0001` `11df` `ffff`
Description:	Add the contents of the W register and register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example:	ADDWF FSR, 0

    Before Instruction
        W = 0x17
        FSR = 0xC2

    After Instruction
        W = 0xD9
        FSR = 0xC2

ANDWF	AND W with f
Syntax:	[*label*] ANDWF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(W) .AND. (f) $\rightarrow$ (dest)
Status Affected:	Z
Encoding:	`0001` `01df` `ffff`
Description:	The contents of the W register are AND'ed with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example:	ANDWF FSR, 1

    Before Instruction
        W = 0x17
        FSR = 0xC2

    After Instruction
        W = 0x17
        FSR = 0x02

ANDLW	And literal with W
Syntax:	[*label*] ANDLW k
Operands:	$0 \le k \le 255$
Operation:	(W).AND. (k) $\rightarrow$ (W)
Status Affected:	Z
Encoding:	`1110` `kkkk` `kkkk`
Description:	The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.
Words:	1
Cycles:	1
Example:	ANDLW 0x5F

    Before Instruction
        W = 0xA3

    After Instruction
        W = 0x03

BCF	Bit Clear f
Syntax:	[*label*] BCF f,b
Operands:	$0 \le f \le 31$ $0 \le b \le 7$
Operation:	0 $\rightarrow$ (f\<b\>)
Status Affected:	None
Encoding:	`0100` `bbbf` `ffff`
Description:	Bit 'b' in register 'f' is cleared.
Words:	1
Cycles:	1
Example:	BCF FLAG_REG, 7

    Before Instruction
        FLAG_REG = 0xC7

    After Instruction
        FLAG_REG = 0x47

CALL	Subroutine Call
Syntax:	[*label*] CALL k
Operands:	0 ≤ k ≤ 255
Operation:	(PC) + 1→ Top of Stack; k → PC<7:0>; (STATUS<6:5>) → PC<10:9>; 0 → PC<8>
Status Affected:	None
Encoding:	1001 kkkk kkkk
Description:	Subroutine call. First, return address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two cycle instruction.
Words:	1
Cycles:	2
Example:	HERE CALL THERE

Before Instruction
PC = address (HERE)
After Instruction
PC = address (THERE)
TOS = address (HERE + 1)

CLRF	Clear f
Syntax:	[*label*] CLRF f
Operands:	0 ≤ f ≤ 31
Operation:	00h → (f); 1 → Z
Status Affected:	Z
Encoding:	0000 011f ffff
Description:	The contents of register 'f' are cleared and the Z bit is set.
Words:	1
Cycles:	1
Example:	CLRF FLAG_REG

Before Instruction
FLAG_REG = 0x5A
After Instruction
FLAG_REG = 0x00
Z   = 1

CLRW	Clear W
Syntax:	[*label*] CLRW
Operands:	None
Operation:	00h → (W); 1 → Z
Status Affected:	Z
Encoding:	0000 0100 0000
Description:	The W register is cleared. Zero bit (Z) is set.
Words:	1
Cycles:	1
Example:	CLRW

Before Instruction
W = 0x5A
After Instruction
W = 0x00
Z = 1

CLRWDT	Clear Watchdog Timer
Syntax:	[*label*] CLRWDT
Operands:	None
Operation:	00h → WDT; 0 → WDT prescaler (if assigned); 1 → $\overline{TO}$; 1 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Encoding:	0000 0000 0100
Description:	The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits $\overline{TO}$ and $\overline{PD}$ are set.
Words:	1
Cycles:	1
Example:	CLRWDT

Before Instruction
WDT counter = ?
After Instruction
WDT counter = 0x00
WDT prescale = 0
$\overline{TO}$ = 1
$\overline{PD}$ = 1

10.16 KEELOQ® Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.

PIC12C5XX

11.4   Timing Diagrams and Specifications

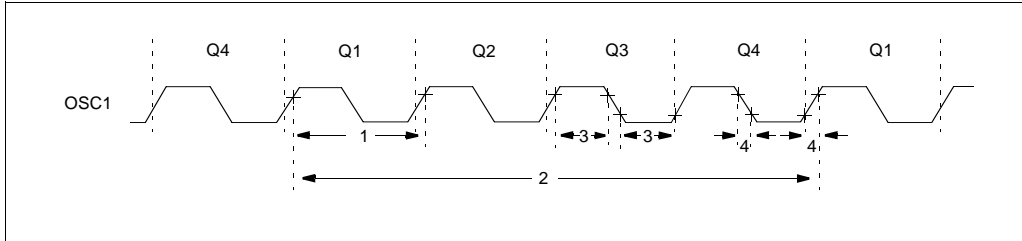**FIGURE 11-2:   EXTERNAL CLOCK TIMING - PIC12C508/C509**

TABLE 11-2:   EXTERNAL CLOCK TIMING REQUIREMENTS - PIC12C508/C509

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), −40°C ≤ TA ≤ +85°C (industrial), −40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 11.1					
Parameter No.	Sym	Characteristic	Min	Typ[1]	Max	Units	Conditions
	FOSC	External CLKIN Frequency[2]					
			DC	—	4	MHz	XT osc mode
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency[2]					
			0.1	—	4	MHz	XT osc mode
			DC	—	200	kHz	LP osc mode
1	TOSC	External CLKIN Period[2]	250	—	—	ns	EXTRC osc mode
			250	—	—	ns	XT osc mode
			5	—	—	ms	LP osc mode
		Oscillator Period[2]	250	—	—	ns	EXTRC osc mode
			250	—	10,000	ns	XT osc mode
			5	—	—	ms	LP osc mode
2	Tcy	Instruction Cycle Time[3]	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			2*	—	—	ms	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	50*	ns	LP oscillator

*   These parameters are characterized but not tested.

Note 1:   Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

   2:   All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
   When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

   3:   Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 11-5: TIMER0 CLOCK TIMINGS - PIC12C508/C509

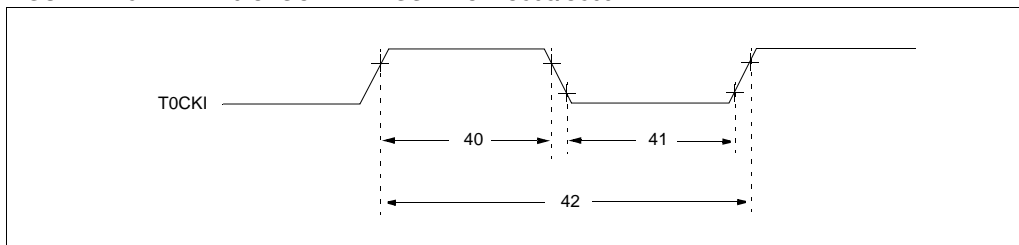**TABLE 11-7: TIMER0 CLOCK REQUIREMENTS - PIC12C508/C509**

AC Characteristics			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature $\quad 0°C \leq T_A \leq +70°C$ (commercial)				
			$\qquad\qquad\qquad\qquad -40°C \leq T_A \leq +85°C$ (industrial)				
			$\qquad\qquad\qquad\qquad -40°C \leq T_A \leq +125°C$ (extended)				
			Operating Voltage V_{DD} range is described in Section 11.1.				

Parameter No.	Sym	Characteristic		Min	Typ[1]	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	- No Prescaler	$0.5\ T_{CY} + 20^*$	—	—	ns	
			- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width	- No Prescaler	$0.5\ T_{CY} + 20^*$	—	—	ns	
			- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period		$\dfrac{20\ or\ \underline{T_{CY} + 40}^*}{N}$	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 12-5: Iₒₕ vs. Vₒₕ, Vᴅᴅ = 2.5 V

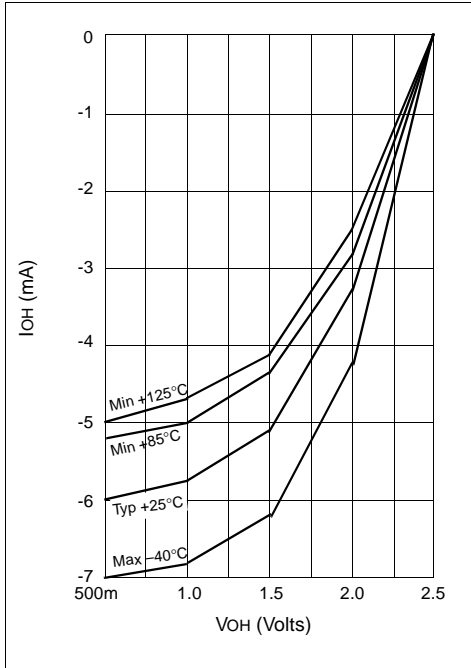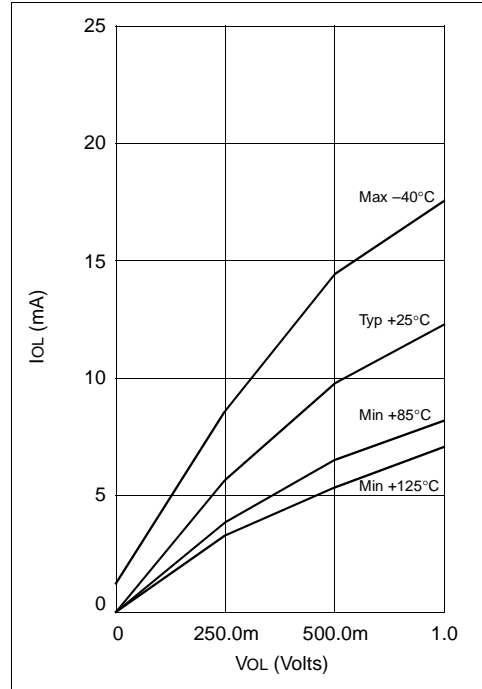**FIGURE 12-6:** Iₒₕ vs. Vₒₕ, Vᴅᴅ = 5.5 V

FIGURE 12-7: Iₒₗ vs. Vₒₗ, Vᴅᴅ = 2.5 V
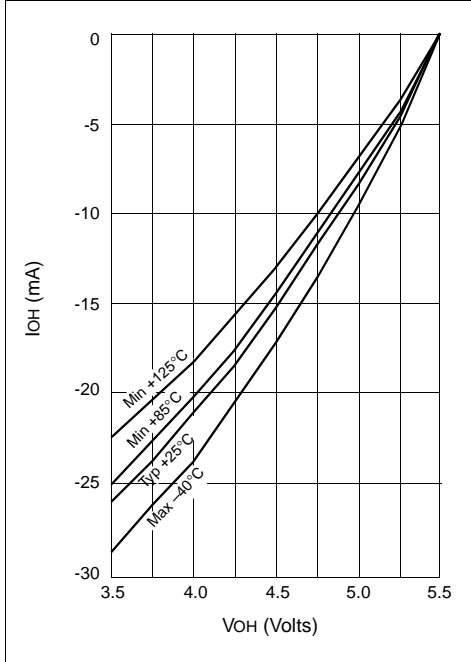
FIGURE 12-8: Iₒₗ vs. Vₒₗ, Vᴅᴅ = 5.5 V
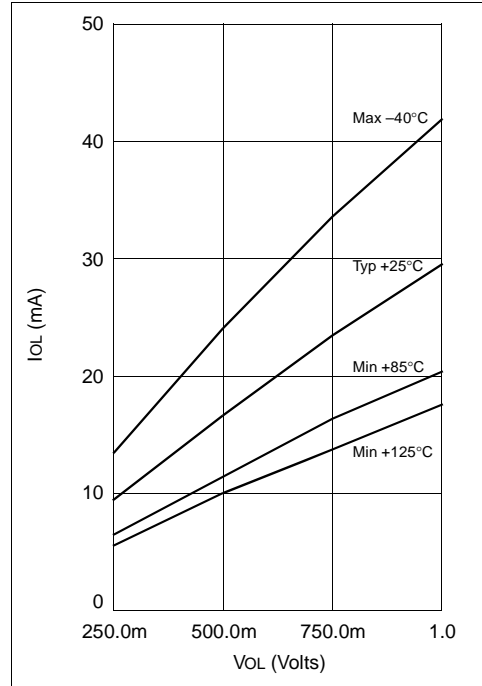
13.1   DC CHARACTERISTICS: PIC12C508A/509A (Commercial, Industrial, Extended)
PIC12CE518/519 (Commercial, Industrial, Extended)
PIC12CR509A (Commercial, Industrial, Extended)

Parm No.	Characteristic	Sym	Min	Typ(1)	Max	Units	Conditions
	DC Characteristics **Power Supply Pins**		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) −40°C ≤ TA ≤ +85°C (industrial) −40°C ≤ TA ≤ +125°C (extended)				
D001	**Supply Voltage**	VDD	3.0		5.5	V	FOSC = DC to 4 MHz (Commercial/Industrial, Extended)
D002	**RAM Data Retention Voltage(2)**	VDR		1.5*		V	Device in SLEEP mode
D003	**VDD Start Voltage to ensure Power-on Reset**	VPOR		VSS		V	See section on Power-on Reset for details
D004	**VDD Rise Rate to ensure Power-on Reset**	SVDD	0.05*			V/ms	See section on Power-on Reset for details
D010	**Supply Current(3)**	IDD	—	0.8	1.4	mA	XT and EXTRC options (Note 4) FOSC = 4 MHz, VDD = 5.5V
D010C			—	0.8	1.4	mA	INTRC Option FOSC = 4 MHz, VDD = 5.5V
D010A			—	19	27	μA	LP OPTION, Commercial Temperature FOSC = 32 kHz, VDD = 3.0V, WDT disabled
			—	19	35	μA	LP OPTION, Industrial Temperature FOSC = 32 kHz, VDD = 3.0V, WDT disabled
			—	30	55	μA	LP OPTION, Extended Temperature FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D020 D021 D021B	**Power-Down Current (5)**	IPD	— — —	0.25 0.25 2	4 5 12	μA μA μA	VDD = 3.0V, Commercial WDT disabled VDD = 3.0V, Industrial WDT disabled VDD = 3.0V, Extended WDT disabled
D022	**Power-Down Current**	ΔIWDT	— — —	2.2 2.2 4	5 6 11	μA μA μA	VDD = 3.0V, Commercial VDD = 3.0V, Industrial VDD = 3.0V, Extended
	Supply Current (3) During read/write to EEPROM peripheral	ΔIEE	—	0.1	0.2	mA	FOSC = 4 MHz, Vdd = 5.5V, SCL = 400kHz

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

    a) The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to
VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

    b) For standby current measurements, the conditions are the same, except that
the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kOhm.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

TABLE 13-1: **PULL-UP RESISTOR RANGES* - PIC12C508A, PIC12C509A, PIC12CR509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519**

V_{DD} (Volts)	Temperature (°C)	Min	Typ	Max	Units
GP0/GP1					
2.5	−40	38K	42K	63K	Ω
	25	42K	48K	63K	Ω
	85	42K	49K	63K	Ω
	125	50K	55K	63K	Ω
5.5	−40	15K	17K	20K	Ω
	25	18K	20K	23K	Ω
	85	19K	22K	25K	Ω
	125	22K	24K	28K	Ω
GP3					
2.5	−40	285K	346K	417K	Ω
	25	343K	414K	532K	Ω
	85	368K	457K	532K	Ω
	125	431K	504K	593K	Ω
5.5	−40	247K	292K	360K	Ω
	25	288K	341K	437K	Ω
	85	306K	371K	448K	Ω
	125	351K	407K	500K	Ω

* These parameters are characterized but not tested.

14.0 DC AND AC CHARACTERISTICS - PIC12C508A/PIC12C509A/ PIC12LC508A/PIC12LC509A, PIC12CE518/PIC12CE519/PIC12CR509A/ PIC12LCE518/PIC12LCE519/ PIC12LCR509A

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified V_{DD} range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean − 3σ) respectively, where σ is standard deviation.

FIGURE 14-1: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE (V_{DD} = 5.0V) (INTERNAL RC IS CALIBRATED TO 25°C, 5.0V)
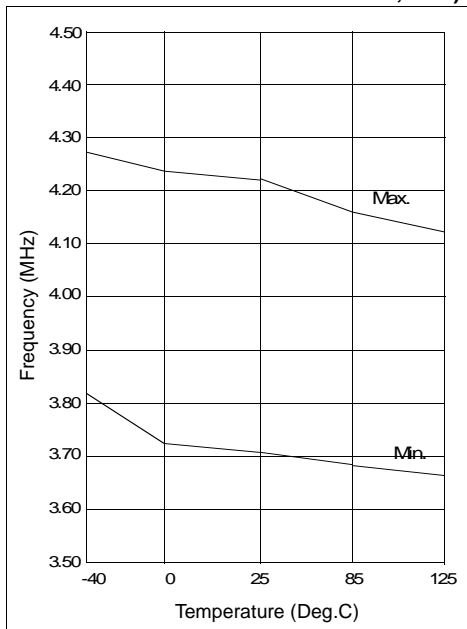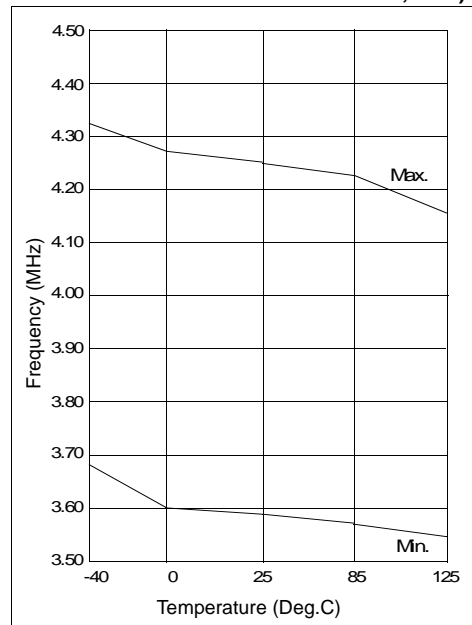

FIGURE 14-2: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE (V_{DD} = 2.5V) (INTERNAL RC IS CALIBRATED TO 25°C, 5.0V)

NOTES: