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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 5 |
| Program Memory Size | 768B (512 x 12) |
| Program Memory Type | OTP |
| EEPROM Size | 16 x 8 |
| RAM Size | 25 x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 8-SOIC (0.209", 5.30mm Width) |
| Supplier Device Package | 8-SOIJ |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic12ce518-04-sm |

### 4.4 OPTION Register

The OPTION register is a 8-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the `OPTION` instruction, the contents of the W register will be transferred to the OPTION register. A RESET sets the OPTION<7:0> bits.

| | |
|---|---|
| **Note:** | If TRIS bit is set to '0', the wake-up on change and pull-up functions are disabled for that pin; i.e., note that TRIS overrides OPTION control of $\overline{\text{GPPU}}$ and $\overline{\text{GPWU}}$. |
| **Note:** | If the T0CS bit is set to '1', GP2 is forced to be an input even if TRIS GP2 = '0'. |

**FIGURE 4-5: OPTION REGISTER**

| W-1 | W-1 | W-1 | W-1 | W-1 | W-1 | W-1 | W-1 |
|---|---|---|---|---|---|---|---|
| $\overline{\text{GPWU}}$ | $\overline{\text{GPPU}}$ | T0CS | T0SE | PSA | PS2 | PS1 | PS0 |
| bit7 | 6 | 5 | 4 | 3 | 2 | 1 | bit0 |

W = Writable bit
U = Unimplemented bit
- n = Value at POR reset
Reference Table 4-1 for other resets.

bit 7: **$\overline{\text{GPWU}}$:** Enable wake-up on pin change (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 6: **$\overline{\text{GPPU}}$**: Enable weak pull-ups (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 5: **T0CS**: Timer0 clock source select bit
1 = Transition on T0CKI pin
0 = Transition on internal instruction cycle clock, Fosc/4

bit 4: **T0SE**: Timer0 source edge select bit
1 = Increment on high to low transition on the T0CKI pin
0 = Increment on low to high transition on the T0CKI pin

bit 3: **PSA**: Prescaler assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0: **PS2:PS0**: Prescaler rate select bits

| Bit Value | Timer0 Rate | WDT Rate |
|---|---|---|
| 000 | 1 : 2 | 1 : 1 |
| 001 | 1 : 4 | 1 : 2 |
| 010 | 1 : 8 | 1 : 4 |
| 011 | 1 : 16 | 1 : 8 |
| 100 | 1 : 32 | 1 : 16 |
| 101 | 1 : 64 | 1 : 32 |
| 110 | 1 : 128 | 1 : 64 |
| 111 | 1 : 256 | 1 : 128 |

### 6.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (TOSC) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

#### 6.1.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-4). Therefore, it is necessary for T0CKI to be high for at least 2TOSC (and a small RC delay of 20 ns) and low for at least 2TOSC (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

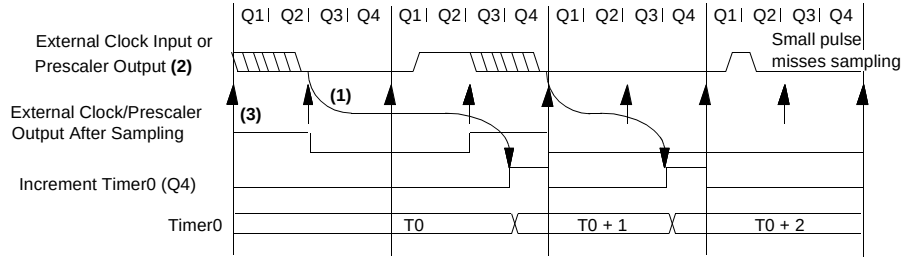
#### 6.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 6-4 shows the delay from the external clock edge to the timer incrementing.

#### 6.1.3 OPTION REGISTER EFFECT ON GP2 TRIS

If the option register is set to read TIMER0 from the pin, the port is forced to an input regardless of the TRIS register setting.

**FIGURE 6-4: TIMER0 TIMING WITH EXTERNAL CLOCK**




Note 1: Delay from clock input change to Timer0 increment is 3Tosc to 7Tosc. (Duration of Q = Tosc). Therefore, the error in measuring the interval between two edges on Timer0 input = ± 4Tosc max.
2: External clock if no prescaler selected, Prescaler output otherwise.
3: The arrows indicate the points in time where sampling occurs.

**FIGURE 7-3: DATA TRANSFER SEQUENCE ON THE SERIAL BUS**

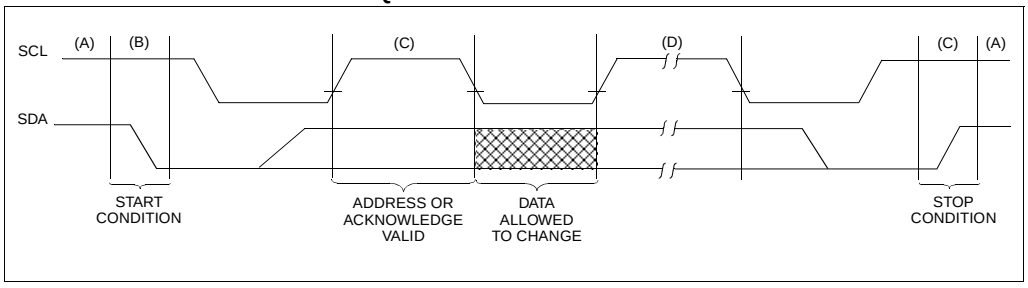
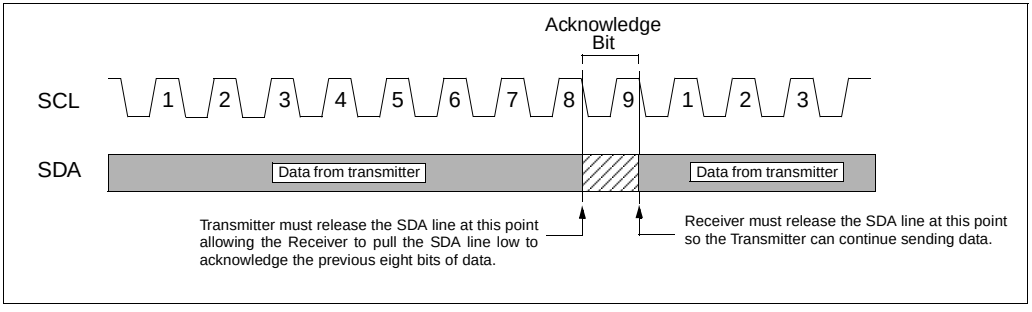



**FIGURE 7-4: ACKNOWLEDGE TIMING**

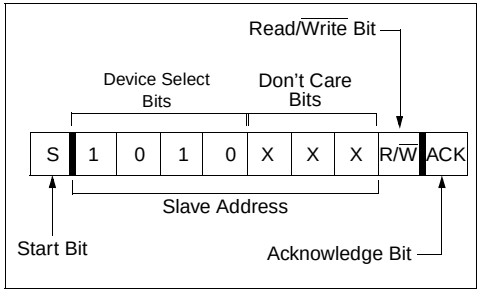



## 7.2 Device Addressing

After generating a START condition, the bus master transmits a control byte consisting of a slave address and a Read/$\overline{\text{Write}}$ bit that indicates what type of operation is to be performed. The slave address consists of a 4-bit device code (1010) followed by three don't care bits.

The last bit of the control byte determines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. (Figure 7-5). The bus is monitored for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

**FIGURE 7-5: CONTROL BYTE FORMAT**



## 7.5 READ OPERATIONS

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

### 7.5.1 CURRENT ADDRESS READ

It contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the device discontinues transmission (Figure 7-8).

### 7.5.2 RANDOM READ

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the device as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. It will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the device discontinues transmission (Figure 7-9). After this command, the internal address counter will point to the address location following the one that was just read.

### 7.5.3 SEQUENTIAL READ

Sequential reads are initiated in the same way as a random read except that after the device transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the device to transmit the next sequentially addressed 8-bit word (Figure 7-10).

To provide sequential reads, it contains an internal address pointer which is incremented by one at the completion of each read operation. This address pointer allows the entire memory contents to be serially read during one operation.

**FIGURE 7-8: CURRENT ADDRESS READ**

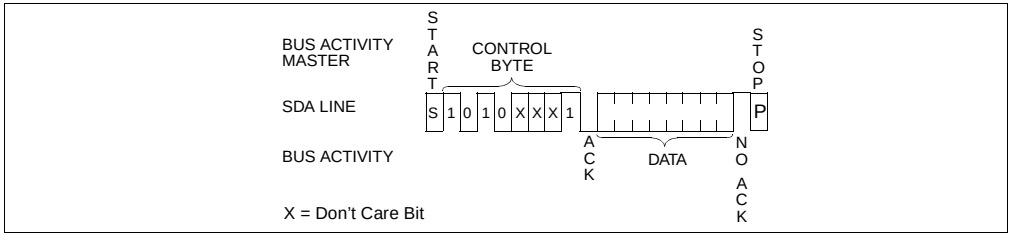



**FIGURE 7-9: RANDOM READ**

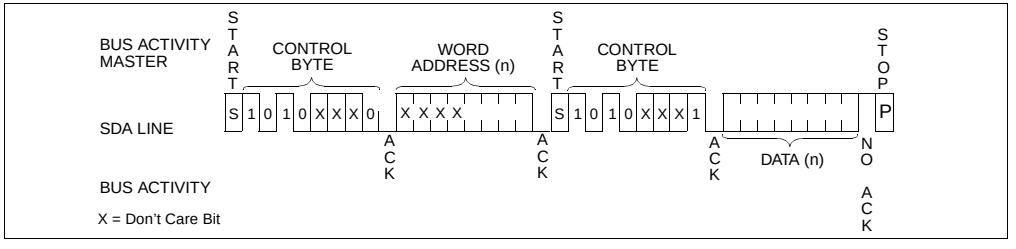
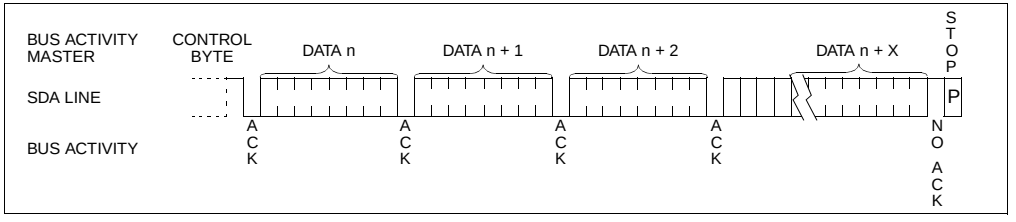



**FIGURE 7-10: SEQUENTIAL READ**



## 8.2 Oscillator Configurations

### 8.2.1 OSCILLATOR TYPES

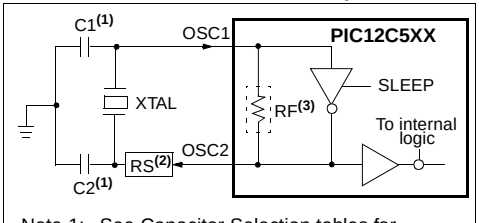
The PIC12C5XX can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

- LP: Low Power Crystal
- XT: Crystal/Resonator
- INTRC: Internal 4 MHz Oscillator
- EXTRC: External Resistor/Capacitor

### 8.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT or LP modes, a crystal or ceramic resonator is connected to the GP5/OSC1/CLKIN and GP4/OSC2 pins to establish oscillation (Figure 8-2). The PIC12C5XX oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT or LP modes, the device can have an external clock source drive the GP5/OSC1/CLKIN pin (Figure 8-3).

**FIGURE 8-2: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (XT OR LP OSC CONFIGURATION)**




Note 1: See Capacitor Selection tables for recommended values of C1 and C2.
2: A series resistor (RS) may be required for AT strip cut crystals.
3: RF approximate value = 10 MΩ.

**FIGURE 8-3: EXTERNAL CLOCK INPUT OPERATION (XT OR LP OSC CONFIGURATION)**

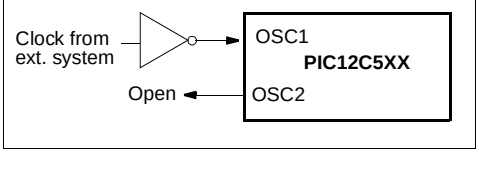



**TABLE 8-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS - PIC12C5XX**

| Osc Type | Resonator Freq | Cap. Range C1 | Cap. Range C2 |
|---|---|---|---|
| XT | 4.0 MHz | 30 pF | 30 pF |

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

**TABLE 8-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - PIC12C5XX**

| Osc Type | Resonator Freq | Cap.Range C1 | Cap. Range C2 |
|---|---|---|---|
| LP | 32 kHz(1) | 15 pF | 15 pF |
| XT | 200 kHz | 47-68 pF | 47-68 pF |
| | 1 MHz | 15 pF | 15 pF |
| | 4 MHz | 15 pF | 15 pF |

Note 1: For $V_{DD}$ > 4.5V, C1 = C2 ≈ 30 pF is recommended.

These values are for design guidance only. Rs may be required to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

**BSF** **Bit Set f**

Syntax: [ *label* ] BSF f,b

Operands: $0 \le f \le 31$
$0 \le b \le 7$

Operation: $1 \rightarrow (f<b>)$

Status Affected: None

Encoding:

| 0101 | bbbf | ffff |
|---|---|---|

Description: Bit 'b' in register 'f' is set.

Words: 1

Cycles: 1

Example:
```
BSF     FLAG_REG,   7
```
Before Instruction
FLAG_REG = 0x0A
After Instruction
FLAG_REG = 0x8A

**BTFSC** **Bit Test f, Skip if Clear**

Syntax: [ *label* ] BTFSC f,b

Operands: $0 \le f \le 31$
$0 \le b \le 7$

Operation: skip if (f<b>) = 0

Status Affected: None

Encoding:

| 0110 | bbbf | ffff |
|---|---|---|

Description: If bit 'b' in register 'f' is 0 then the next instruction is skipped.
If bit 'b' is 0 then the next instruction fetched during the current instruction execution is discarded, and an NOP is executed instead, making this a 2 cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE    BTFSC   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```
Before Instruction
PC = address (HERE)
After Instruction
if FLAG<1> = 0,
PC = address (TRUE);
if FLAG<1> = 1,
PC = address(FALSE)

**BTFSS** **Bit Test f, Skip if Set**

Syntax: [ *label* ] BTFSS f,b

Operands: $0 \le f \le 31$
$0 \le b < 7$

Operation: skip if (f<b>) = 1

Status Affected: None

Encoding:

| 0111 | bbbf | ffff |
|---|---|---|

Description: If bit 'b' in register 'f' is '1' then the next instruction is skipped.
If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and an NOP is executed instead, making this a 2 cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE    BTFSS   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```
Before Instruction
PC = address (HERE)
After Instruction
If FLAG<1> = 0,
PC = address (FALSE);
if FLAG<1> = 1,
PC = address (TRUE)

**MOVF** **Move f**

Syntax: [ *label* ] MOVF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) → (dest)

Status Affected: Z

Encoding:

| 0010 | 00df | ffff |
|---|---|---|

Description: The contents of register 'f' is moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' is 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example:
```
MOVF    FSR,    0
```
After Instruction
W = value in FSR register

**MOVLW** **Move Literal to W**

Syntax: [ *label* ] MOVLW k

Operands: $0 \le k \le 255$

Operation: k → (W)

Status Affected: None

Encoding:

| 1100 | kkkk | kkkk |
|---|---|---|

Description: The eight bit literal 'k' is loaded into the W register. The don't cares will assemble as 0s.

Words: 1

Cycles: 1

Example:
```
MOVLW   0x5A
```
After Instruction
W = 0x5A

**MOVWF** **Move W to f**

Syntax: [ *label* ] MOVWF f

Operands: $0 \le f \le 31$

Operation: (W) → (f)

Status Affected: None

Encoding:

| 0000 | 001f | ffff |
|---|---|---|

Description: Move data from the W register to register 'f'.

Words: 1

Cycles: 1

Example:
```
MOVWF   TEMP_REG
```
Before Instruction
TEMP_REG = 0xFF
W = 0x4F

After Instruction
TEMP_REG = 0x4F
W = 0x4F

**NOP** **No Operation**

Syntax: [ *label* ] NOP

Operands: None

Operation: No operation

Status Affected: None

Encoding:

| 0000 | 0000 | 0000 |
|---|---|---|

Description: No operation.

Words: 1

Cycles: 1

Example:
```
NOP
```

**OPTION** **Load OPTION Register**

Syntax: [ *label* ] OPTION

Operands: None

Operation: (W) → OPTION

Status Affected: None

Encoding:

| | | |
|---|---|---|
| 0000 | 0000 | 0010 |

Description: The content of the W register is loaded into the OPTION register.

Words: 1

Cycles: 1

Example

```
OPTION
```

Before Instruction
W = 0x07

After Instruction
OPTION = 0x07

**RETLW** **Return with Literal in W**

Syntax: [ *label* ] RETLW k

Operands: 0 ≤ k ≤ 255

Operation: k → (W);
TOS → PC

Status Affected: None

Encoding:

| | | |
|---|---|---|
| 1000 | kkkk | kkkk |

Description: The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

Words: 1

Cycles: 2

Example:

```
CALL TABLE ;W contains
           ;table offset
           ;value.
•          ;W now has table
•          ;value.
•
TABLE      ADDWF PC   ;W = offset
           RETLW k1   ;Begin table
           RETLW k2   ;
           •
           •
           •
           RETLW kn   ; End of table
```

Before Instruction
W = 0x07

After Instruction
W = value of k8

**RLF** **Rotate Left f through Carry**

Syntax: [ *label* ] RLF f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

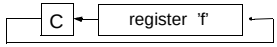
Operation: See description below

Status Affected: C

Encoding:

| | | |
|---|---|---|
| 0011 | 01df | ffff |

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.




Words: 1

Cycles: 1

Example:

```
RLF     REG1,0
```

Before Instruction
```
REG1    =   1110 0110
C       =   0
```

After Instruction
```
REG1    =   1110 0110
W       =   1100 1100
C       =   1
```

**RRF** **Rotate Right f through Carry**

Syntax: [ *label* ] RRF f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

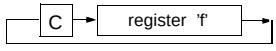
Operation: See description below

Status Affected: C

Encoding:

| | | |
|---|---|---|
| 0011 | 00df | ffff |

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.




Words: 1

Cycles: 1

Example:

```
RRF     REG1,0
```

Before Instruction
```
REG1    =   1110 0110
C       =   0
```

After Instruction
```
REG1    =   1110 0110
W       =   0111 0011
C       =   0
```

**SWAPF** **Swap Nibbles in f**

Syntax: [ *label* ] SWAPF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f<3:0>) → (dest<7:4>);
(f<7:4>) → (dest<3:0>)

Status Affected: None

Encoding:

| 0011 | 10df | ffff |
|---|---|---|

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.

Words: 1

Cycles: 1

Example
```
SWAPF   REG1,  0
```
Before Instruction
REG1 = 0xA5

After Instruction
REG1 = 0xA5
W = 0X5A

**TRIS** **Load TRIS Register**

Syntax: [ *label* ] TRIS f

Operands: f = 6

Operation: (W) → TRIS register f

Status Affected: None

Encoding:

| 0000 | 0000 | 0fff |
|---|---|---|

Description: TRIS register 'f' (f = 6) is loaded with the contents of the W register

Words: 1

Cycles: 1

Example
```
TRIS    GPIO
```
Before Instruction
W = 0XA5

After Instruction
TRIS = 0XA5

**Note:** f = 6 for PIC12C5XX only.

**XORLW** **Exclusive OR literal with W**

Syntax: [*label*] XORLW k

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Encoding:

| 1111 | kkkk | kkkk |
|---|---|---|

Description: The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example
```
XORLW  0xAF
```
Before Instruction
W = 0xB5

After Instruction
W = 0x1A

**XORWF** **Exclusive OR W with f**

Syntax: [ *label* ] XORWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (dest)

Status Affected: Z

Encoding:

| 0001 | 10df | ffff |
|---|---|---|

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example
```
XORWF  REG,1
```
Before Instruction
REG = 0xAF
W = 0xB5

After Instruction
REG = 0x1A
W = 0xB5

## 11.0 ELECTRICAL CHARACTERISTICS - PIC12C508/PIC12C509

### Absolute Maximum Ratings†

Ambient Temperature under bias ..... –40°C to +125°C
Storage Temperature ..... –65°C to +150°C
Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... 0 to +7.5 V
Voltage on $\overline{MCLR}$ with respect to $V_{SS}$ ..... 0 to +14 V
Voltage on all other pins with respect to $V_{SS}$ ..... –0.6 V to ($V_{DD}$ + 0.6 V)
Total Power Dissipation(1) ..... 700 mW
Max. Current out of $V_{SS}$ pin ..... 200 mA
Max. Current into $V_{DD}$ pin ..... 150 mA
Input Clamp Current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{DD}$) ..... ±20 mA
Output Clamp Current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{DD}$) ..... ±20 mA
Max. Output Current sunk by any I/O pin ..... 25 mA
Max. Output Current sourced by any I/O pin ..... 25 mA
Max. Output Current sourced by I/O port (GPIO) ..... 100 mA
Max. Output Current sunk by I/O port (GPIO ) ..... 100 mA

**Note 1:** Power Dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## 12.0 DC AND AC CHARACTERISTICS - PIC12C508/PIC12C509

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean – 3σ) respectively, where σ is standard deviation.

**FIGURE 12-1: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE (VDD = 2.5V)**

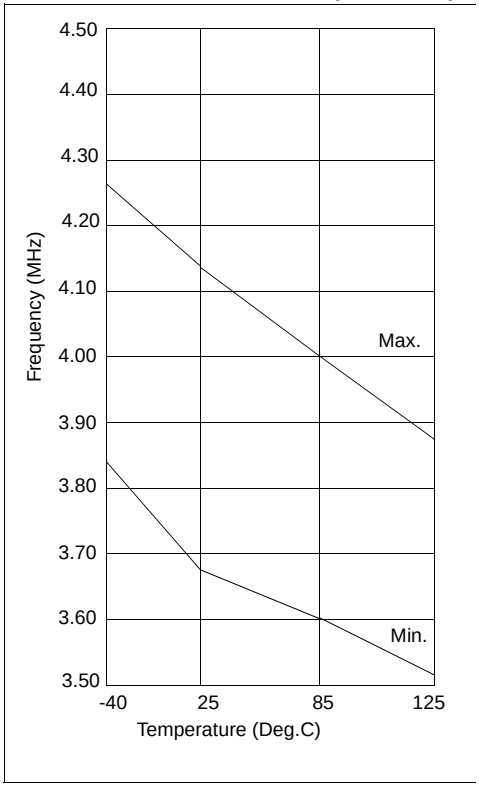



**FIGURE 12-2: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE (VDD = 5.0V)**

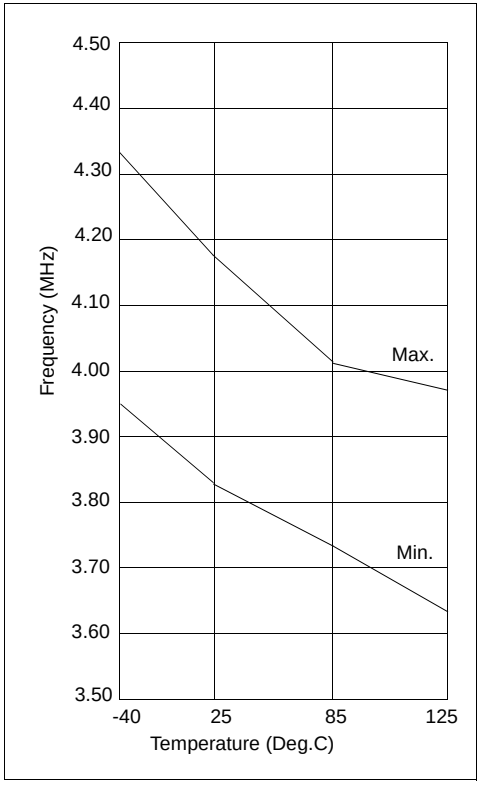


**TABLE 12-1: DYNAMIC IDD (TYPICAL) - WDT ENABLED, 25°C**

| Oscillator | Frequency | VDD = 2.5V | VDD = 5.5V |
|---|---|---|---|
| External RC | 4 MHz | 250 µA* | 780 µA* |
| Internal RC | 4 MHz | 420 µA | 1.1 mA |
| XT | 4 MHz | 251 µA | 780 µA |
| LP | 32 KHz | 15 µA | 37 µA |

*Does not include current through external R&C.

**FIGURE 12-3: WDT TIMER TIME-OUT PERIOD VS. VDD**

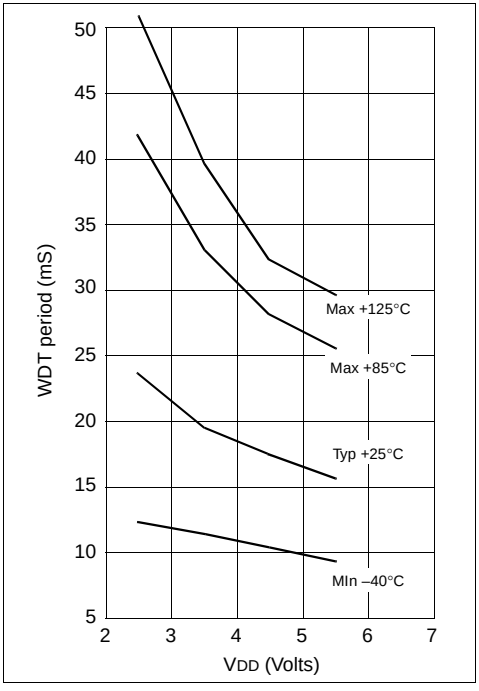
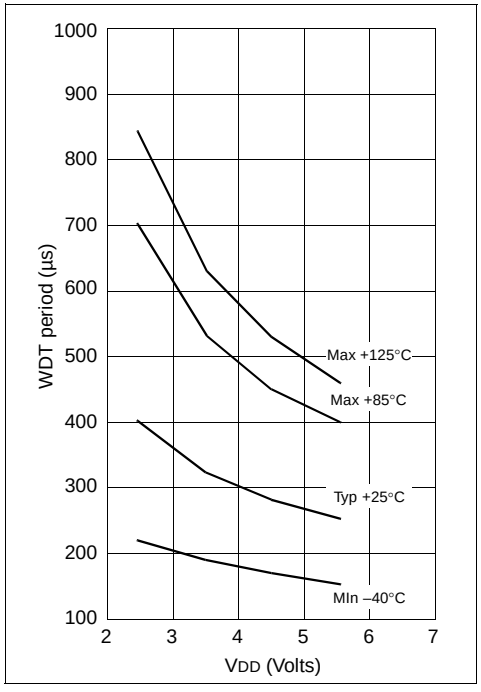



**FIGURE 12-4: SHORT DRT PERIOD VS. VDD**



## 13.4 DC CHARACTERISTICS: PIC12LC508A/509A (Commercial, Industrial) PIC12LC518/519 (Commercial, Industrial) PIC12LCR509A (Commercial, Industrial)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating temperature 0°C ≤ TA ≤ +70°C (commercial)<br>–40°C ≤ TA ≤ +85°C (industrial)<br>Operating voltage VDD range as described in DC spec Section 13.1 and Section 13.2. | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Sym** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | **Input Low Voltage** | | | | | | |
| | I/O ports | VIL | | | | | |
| D030 | with TTL buffer | | VSS | - | 0.8V | V | For 4.5V ≤ VDD ≤ 5.5V |
| | | | VSS | - | 0.15VDD | V | otherwise |
| D031 | with Schmitt Trigger buffer | | VSS | - | 0.2VDD | V | |
| D032 | $\overline{MCLR}$, GP2/T0CKI (in EXTRC mode) | | VSS | - | 0.2VDD | V | |
| D033 | OSC1 (in EXTRC mode) | | VSS | - | 0.2VDD | V | Note 1 |
| D033 | OSC1 (in XT and LP) | | VSS | - | 0.3VDD | V | Note 1 |
| | **Input High Voltage** | | | | | | |
| | I/O ports | VIH | | - | | | |
| D040 | with TTL buffer | | 0.25VDD + 0.8V | - | VDD | V | 4.5V ≤ VDD ≤ 5.5V |
| D040A | | | 2.0V | - | VDD | V | otherwise |
| D041 | with Schmitt Trigger buffer | | 0.8VDD | - | VDD | V | For entire VDD range |
| D042 | $\overline{MCLR}$, GP2/T0CKI | | 0.8VDD | - | VDD | V | |
| D042A | OSC1 (XT and LP) | | 0.7VDD | - | VDD | V | Note 1 |
| D043 | OSC1 (in EXTRC mode) | | 0.9VDD | - | VDD | V | |
| D070 | GPIO weak pull-up current (Note 4) | IPUR | 30 | 250 | 400 | µA | VDD = 5V, VPIN = VSS |
| | $\overline{MCLR}$ pull-up current | - | - | - | 30 | µA | VDD = 5V, VPIN = VSS |
| | **Input Leakage Current** (Notes 2, 3) | | | | | | |
| D060 | I/O ports | IIL | - | - | ±1 | µA | Vss ≤ VPIN ≤ VDD, Pin at hi-impedance |
| D061 | T0CKI | | - | - | ±5 | µA | Vss ≤ VPIN ≤ VDD |
| D063 | OSC1 | | - | - | ±5 | µA | Vss ≤ VPIN ≤ VDD, XT and LP osc configuration |
| | **Output Low Voltage** | | | | | | |
| D080 | I/O ports | VOL | - | - | 0.6 | V | IOL = 8.5 mA, VDD = 4.5V, –40°C to +85°C |
| D080A | | | - | - | 0.6 | V | IOL = 7.0 mA, VDD = 4.5V, –40°C to +125°C |
| | **Output High Voltage** | | | | | | |
| D090 | I/O ports (Note 3) | VOH | VDD - 0.7 | - | - | V | IOH = -3.0 mA, VDD = 4.5V, –40°C to +85°C |
| D090A | | | VDD - 0.7 | - | - | V | IOH = -2.5 mA, VDD = 4.5V, –40°C to +125°C |
| | **Capacitive Loading Specs on Output Pins** | | | | | | |
| D100 | OSC2 pin | COSC2 | - | - | 15 | pF | In XT and LP modes when external clock is used to drive OSC1. |
| D101 | All I/O pins | CIO | - | - | 50 | pF | |

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C5XX be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: This spec. applies when GP3/$\overline{MCLR}$ is configured as $\overline{MCLR}$. The leakage current of the $\overline{MCLR}$ circuit is higher than the standard I/O logic.

**TABLE 13-3: CALIBRATED INTERNAL RC FREQUENCIES - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519**

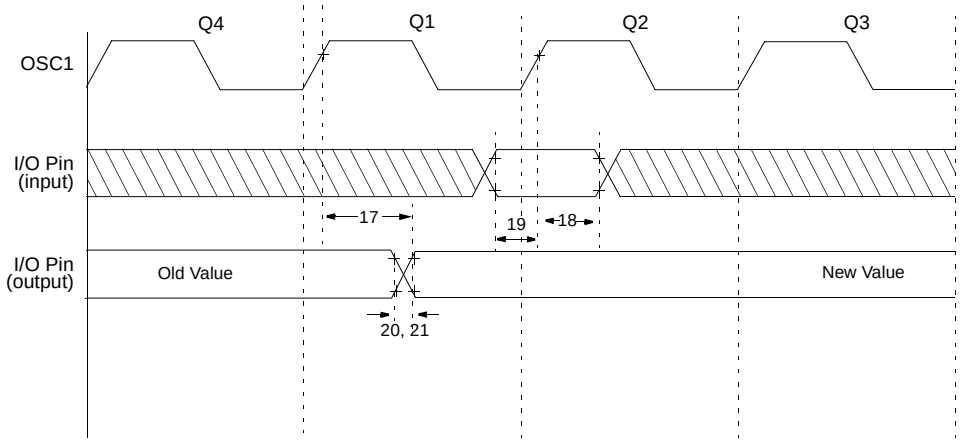
| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C (commercial),<br>–40°C ≤ TA ≤ +85°C (industrial),<br>–40°C ≤ TA ≤ +125°C (extended)<br>Operating Voltage VDD range is described in Section 10.1 |
|---|---|

| Parameter No. | Sym | Characteristic | Min* | Typ(1) | Max* | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | Internal Calibrated RC Frequency | 3.65 | 4.00 | 4.28 | MHz | VDD = 5.0V |
| | | Internal Calibrated RC Frequency | 3.55 | — | 4.31 | MHz | VDD = 2.5V |

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 13-3: I/O TIMING - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519**




Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

**TABLE 13-4: TIMING REQUIREMENTS - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519**

| **AC Characteristics** | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C (commercial)<br>–40°C ≤ TA ≤ +85°C (industrial)<br>–40°C ≤ TA ≤ +125°C (extended)<br>Operating Voltage VDD range is described in Section 13.1 | | | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Sym** | **Characteristic** | **Min** | **Typ(1)** | **Max** | **Units** |
| 17 | TosH2ioV | OSC1↑ (Q1 cycle) to Port out valid(3) | — | — | 100* | ns |
| 18 | TosH2ioI | OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time) | TBD | — | — | ns |
| 19 | TioV2osH | Port input valid to OSC1↑ (I/O in setup time) | TBD | — | — | ns |
| 20 | TioR | Port output rise time(2, 3) | — | 10 | 25** | ns |
| 21 | TioF | Port output fall time(2, 3) | — | 10 | 25** | ns |

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in EXTRC mode.

3: See Figure 13-1 for loading conditions.

**TABLE 13-8: EEPROM MEMORY BUS TIMING REQUIREMENTS - PIC12CE5XX ONLY.**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C, Vcc = 3.0V to 5.5V (commercial)<br>–40°C ≤ TA ≤ +85°C, Vcc = 3.0V to 5.5V (industrial)<br>–40°C ≤ TA ≤ +125°C, Vcc = 4.5V to 5.5V (extended)<br>Operating Voltage VDD range is described in Section 13.1 | | | | |
|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Units** | **Conditions** |
| Clock frequency | FCLK | —<br>—<br>— | 100<br>100<br>400 | kHz | 4.5V ≤ Vcc ≤ 5.5V (E Temp range)<br>3.0V ≤ Vcc ≤ 4.5V<br>4.5V ≤ Vcc ≤ 5.5V |
| Clock high time | THIGH | 4000<br>4000<br>600 | —<br>—<br>— | ns | 4.5V ≤ Vcc ≤ 5.5V (E Temp range)<br>3.0V ≤ Vcc ≤ 4.5V<br>4.5V ≤ Vcc ≤ 5.5V |
| Clock low time | TLOW | 4700<br>4700<br>1300 | —<br>—<br>— | ns | 4.5V ≤ Vcc ≤ 5.5V (E Temp range)<br>3.0V ≤ Vcc ≤ 4.5V<br>4.5V ≤ Vcc ≤ 5.5V |
| SDA and SCL rise time (Note 1) | TR | —<br>—<br>— | 1000<br>1000<br>300 | ns | 4.5V ≤ Vcc ≤ 5.5V (E Temp range)<br>3.0V ≤ Vcc ≤ 4.5V<br>4.5V ≤ Vcc ≤ 5.5V |
| SDA and SCL fall time | TF | — | 300 | ns | (Note 1) |
| START condition hold time | THD:STA | 4000<br>4000<br>600 | —<br>—<br>— | ns | 4.5V ≤ Vcc ≤ 5.5V (E Temp range)<br>3.0V ≤ Vcc ≤ 4.5V<br>4.5V ≤ Vcc ≤ 5.5V |
| START condition setup time | TSU:STA | 4700<br>4700<br>600 | —<br>—<br>— | ns | 4.5V ≤ Vcc ≤ 5.5V (E Temp range)<br>3.0V ≤ Vcc ≤ 4.5V<br>4.5V ≤ Vcc ≤ 5.5V |
| Data input hold time | THD:DAT | 0 | — | ns | (Note 2) |
| Data input setup time | TSU:DAT | 250<br>250<br>100 | —<br>—<br>— | ns | 4.5V ≤ Vcc ≤ 5.5V (E Temp range)<br>3.0V ≤ Vcc ≤ 4.5V<br>4.5V ≤ Vcc ≤ 5.5V |
| STOP condition setup time | TSU:STO | 4000<br>4000<br>600 | —<br>—<br>— | ns | 4.5V ≤ Vcc ≤ 5.5V (E Temp range)<br>3.0V ≤ Vcc ≤ 4.5V<br>4.5V ≤ Vcc ≤ 5.5V |
| Output valid from clock (Note 2) | TAA | —<br>—<br>— | 3500<br>3500<br>900 | ns | 4.5V ≤ Vcc ≤ 5.5V (E Temp range)<br>3.0V ≤ Vcc ≤ 4.5V<br>4.5V ≤ Vcc ≤ 5.5V |
| Bus free time: Time the bus must be free before a new transmission can start | TBUF | 4700<br>4700<br>1300 | —<br>—<br>— | ns | 4.5V ≤ Vcc ≤ 5.5V (E Temp range)<br>3.0V ≤ Vcc ≤ 4.5V<br>4.5V ≤ Vcc ≤ 5.5V |
| Output fall time from VIH minimum to VIL maximum | TOF | 20+0.1 CB | 250 | ns | (Note 1), CB ≤ 100 pF |
| Input filter spike suppression (SDA and SCL pins) | TSP | — | 50 | ns | (Notes 1, 3) |
| Write cycle time | TWC | — | 4 | ms | |
| Endurance | | 1M | — | cycles | 25°C, VCC = 5.0V, Block Mode (Note 4) |

**Note 1:** Not 100% tested. CB = total capacitance of one bus line in pF.

**2:** As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

**3:** The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

**4:** This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on Microchip's website.

**FIGURE 14-9: IOL vs. VOL, VDD = 2.5 V**

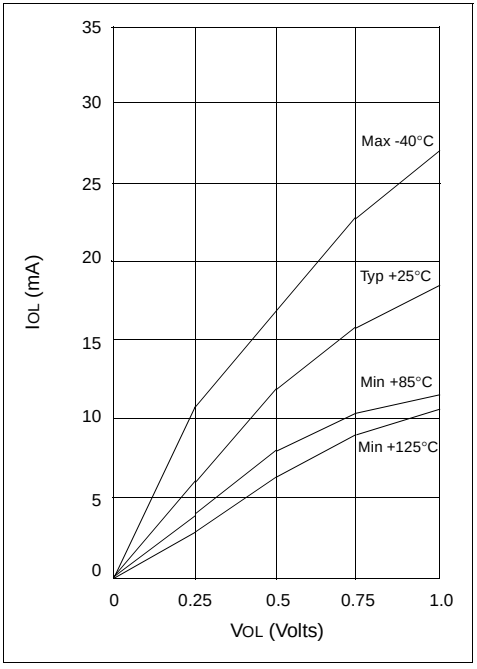



**FIGURE 14-10: IOL vs. VOL, VDD = 3.5 V**

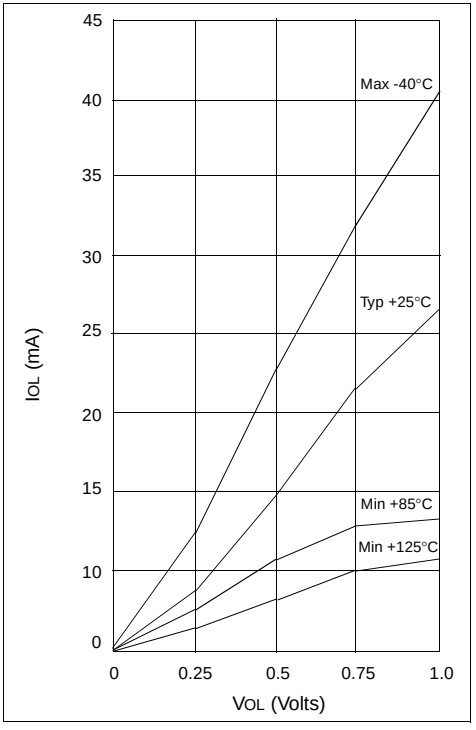



**FIGURE 14-11: IOH vs. VOH, VDD = 5.5 V**

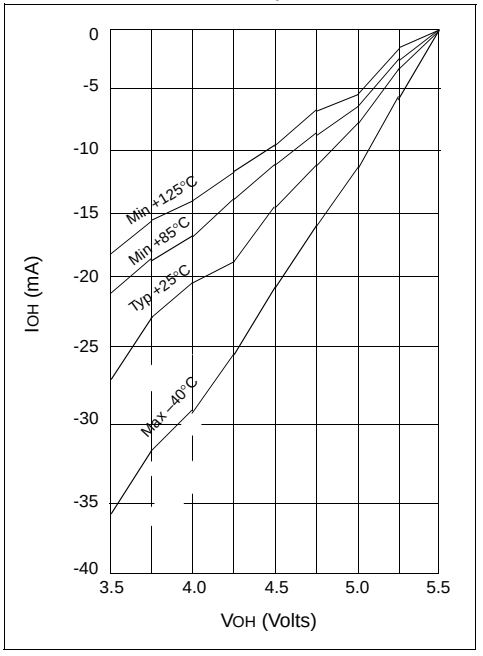
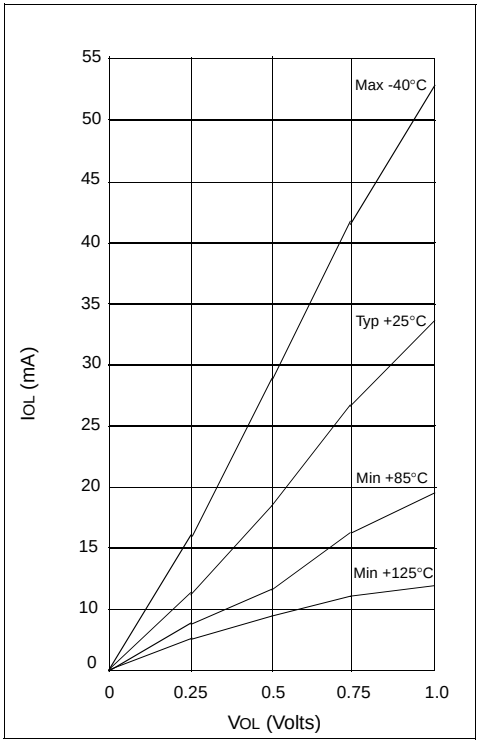
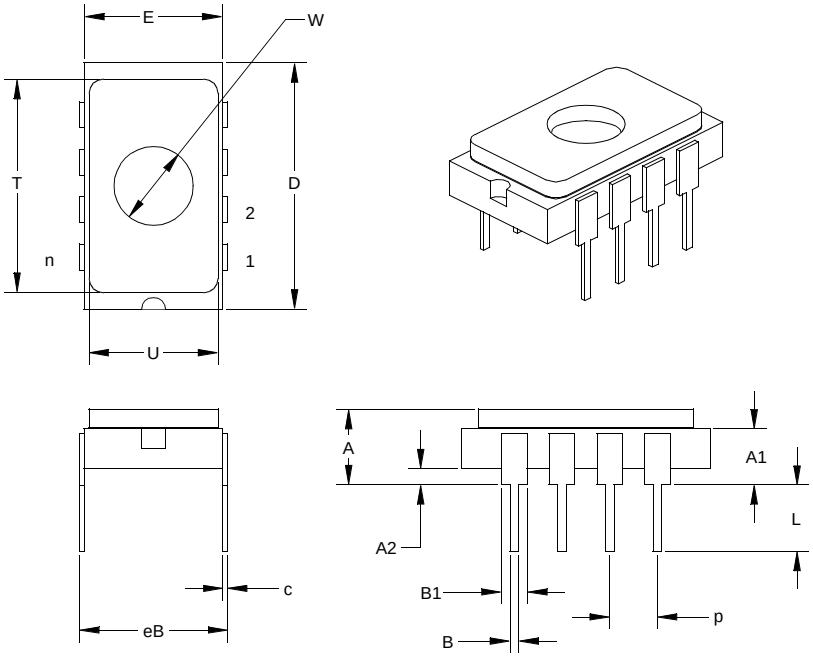



**FIGURE 14-12: IOL vs. VOL, VDD = 5.5 V**



**Package Type: K04-084 8-Lead Ceramic Side Brazed Dual In-line with Window (JW) – 300 mil**




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| PCB Row Spacing | | | 0.300 | | | 7.62 | |
| Number of Pins | n | | 8 | | | 8 | |
| Pitch | p | 0.098 | 0.100 | 0.102 | 2.49 | 2.54 | 2.59 |
| Lower Lead Width | B | 0.016 | 0.018 | 0.020 | 0.41 | 0.46 | 0.51 |
| Upper Lead Width | B1 | 0.050 | 0.055 | 0.060 | 1.27 | 1.40 | 1.52 |
| Lead Thickness | c | 0.008 | 0.010 | 0.012 | 0.20 | 0.25 | 0.30 |
| Top to Seating Plane | A | 0.145 | 0.165 | 0.185 | 3.68 | 4.19 | 4.70 |
| Top of Body to Seating Plane | A1 | 0.103 | 0.123 | 0.143 | 2.62 | 3.12 | 3.63 |
| Base to Seating Plane | A2 | 0.025 | 0.035 | 0.045 | 0.64 | 0.89 | 1.14 |
| Tip to Seating Plane | L | 0.130 | 0.140 | 0.150 | 3.30 | 3.56 | 3.81 |
| Package Length | D | 0.510 | 0.520 | 0.530 | 12.95 | 13.21 | 13.46 |
| Package Width | E | 0.280 | 0.290 | 0.300 | 7.11 | 7.37 | 7.62 |
| Overall Row Spacing | eB | 0.310 | 0.338 | 0.365 | 7.87 | 8.57 | 9.27 |
| Window Diameter | W | 0.161 | 0.166 | 0.171 | 4.09 | 4.22 | 4.34 |
| Lid Length | T | 0.440 | 0.450 | 0.460 | 11.18 | 11.43 | 11.68 |
| Lid Width | U | 0.260 | 0.270 | 0.280 | 6.60 | 6.86 | 7.11 |

* Controlling Parameter.

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**NOTES:**