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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

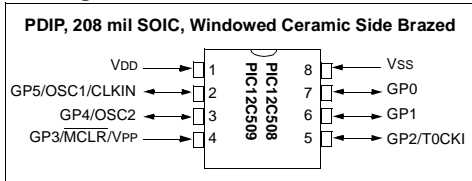
Applications of "[Embedded - Microcontrollers](#)"

Details

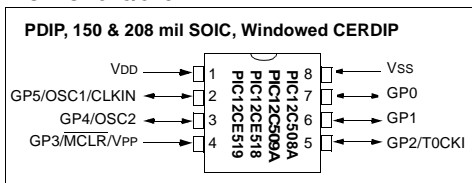
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	16 x 8
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12ce518-04-sn

PIC12C5XX

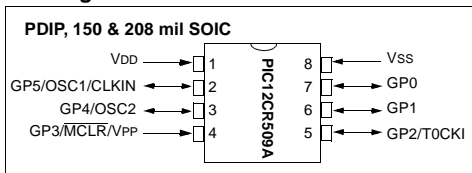
Pin Diagram - PIC12C508/509



Pin Diagram - PIC12C508A/509A, PIC12CE518/519



Pin Diagram - PIC12CR509A



Device Differences

Device	Voltage Range	Oscillator	Oscillator Calibration ² (Bits)	Process Technology (Microns)
PIC12C508A	3.0-5.5	See Note 1	6	0.7
PIC12LC508A	2.5-5.5	See Note 1	6	0.7
PIC12C508	2.5-5.5	See Note 1	4	0.9
PIC12C509A	3.0-5.5	See Note 1	6	0.7
PIC12LC509A	2.5-5.5	See Note 1	6	0.7
PIC12C509	2.5-5.5	See Note 1	4	0.9
PIC12CR509A	2.5-5.5	See Note 1	6	0.7
PIC12CE518	3.0-5.5	-	6	0.7
PIC12LCE518	2.5-5.5	-	6	0.7
PIC12CE519	3.0-5.5	-	6	0.7
PIC12LCE519	2.5-5.5	-	6	0.7

Note 1: If you change from the PIC12C50X to the PIC12C50XA or to the PIC12CR50XA, please verify oscillator characteristics in your application.

Note 2: See Section 7.2.5 for OSCCAL implementation differences.

1.0 GENERAL DESCRIPTION

The PIC12C5XX from Microchip Technology is a family of low-cost, high performance, 8-bit, fully static, EEPROM/EPROM/ROM-based CMOS microcontrollers. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle (1 μ s) except for program branches which take two cycles. The PIC12C5XX delivers performance an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC12C5XX products are equipped with special features that reduce system cost and power requirements. The Power-On Reset (POR) and Device Reset Timer (DRT) eliminate the need for external reset circuitry. There are four oscillator configurations to choose from, including INTRC internal oscillator mode and the power-saving LP (Low Power) oscillator mode. Power saving SLEEP mode, Watchdog Timer and code protection features also improve system cost, power and reliability.

The PIC12C5XX are available in the cost-effective One-Time-Programmable (OTP) versions which are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers while benefiting from the OTP's flexibility.

The PIC12C5XX products are supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a 'C' compiler, fuzzy logic support tools, a low-cost development programmer, and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

1.1 Applications

The PIC12C5XX series fits perfectly in applications ranging from personal care appliances and security systems to low-power remote transmitters/receivers. The EPROM technology makes customizing application programs (transmitter codes, appliance settings, receiver frequencies, etc.) extremely fast and convenient, while the EEPROM data memory technology allows for the changing of calibration factors and security codes. The small footprint packages, for through hole or surface mounting, make this microcontroller series perfect for applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the PIC12C5XX series very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic and PLD's in larger systems, coprocessor applications).

PIC12C5XX

NOTES:

NOTES:

TABLE 5-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	TRIS	—	—							--11 1111	--11 1111
N/A	OPTION	GPWU	GPPU	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
03H	STATUS	GPWUF	—	PAO	\overline{TO}	\overline{PD}	Z	DC	C	0001 1xxx	q00q quuu ⁽¹⁾
06h	GPIO (PIC12C508/ PIC12C509/ PIC12C508A/ PIC12C509A/ PIC12CR509A)	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	--uu uuuu
06h	GPIO (PIC12CE518/ PIC12CE519)	SCL	SDA	GP5	GP4	GP3	GP2	GP1	GP0	11xx xxxx	11uu uuuu

Legend: Shaded cells not used by Port Registers, read as '0', — = unimplemented, read as '0', x = unknown, u = unchanged, q = see tables in Section 8.7 for possible values.

Note 1: If reset was due to wake-up on change, then bit 7 = 1. All other resets will cause bit 7 = 0.

5.4 I/O Programming Considerations

5.4.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of GPIO will cause all eight bits of GPIO to be read into the CPU, bit5 to be set and the GPIO value to be written to the output latches. If another bit of GPIO is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial GPIO Settings
; GPIO<5:3> Inputs
; GPIO<2:0> Outputs
;
;
;          GPIO latch  GPIO pins
;          -----
BCF  GPIO, 5  ;--01 -ppp  --11 pppp
BCF  GPIO, 4  ;--10 -ppp  --11 pppp
MOVLW 007h    ;
TRIS  GPIO    ;--10 -ppp  --11 pppp
;
;Note that the user may have expected the pin
;values to be --00 pppp. The 2nd BCF caused
;GP5 to be latched as the pin value (High).
```

5.4.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

7.3 WRITE OPERATIONS

7.3.1 BYTE WRITE

Following the start signal from the master, the device code (4 bits), the don't care bits (3 bits), and the R/W bit (which is a logic low) are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer. Only the lower four address bits are used by the device, and the upper four bits are don't cares. The address byte is acknowledgeable and the master device will then transmit the data word to be written into the addressed memory location. The memory acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time will not generate acknowledge signals (Figure 7-7). After a byte write command, the internal address counter will not be incremented and will point to the same address location that was just written. If a stop bit is transmitted to the device at any point in the write command sequence before the entire sequence is complete, then the command will abort and no data will be written. If more than 8 data bits are transmitted before the stop bit is sent, then the device will clear the previously loaded byte and begin loading the data buffer again. If more than one data byte is transmitted to the device and a stop bit is sent before a full eight data bits have been transmitted, then the write command will abort and no data will be written. The EEPROM memory employs a VCC threshold detector circuit which disables the internal erase/write logic if the VCC is below minimum VDD.

Byte write operations must be preceded and immediately followed by a bus not busy bus cycle where both SDA and SCL are held high.

7.4 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/W = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the start bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-6 for flow diagram.

FIGURE 7-6: ACKNOWLEDGE POLLING FLOW

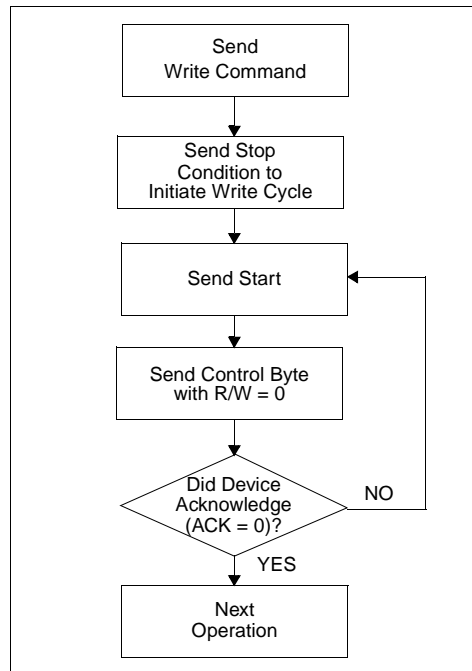
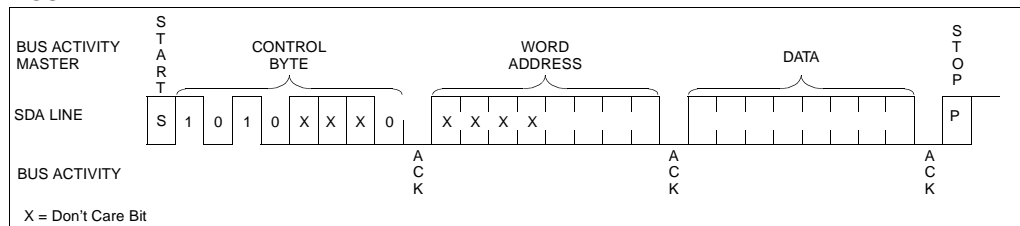


FIGURE 7-7: BYTE WRITE



8.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real-time applications. The PIC12C5XX family of microcontrollers has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- Oscillator selection
- Reset
 - Power-On Reset (POR)
 - Device Reset Timer (DRT)
 - Wake-up from SLEEP on pin change
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID locations
- In-circuit Serial Programming

The PIC12C5XX has a Watchdog Timer which can be shut off only through configuration bit WDTE. It runs off of its own RC oscillator for added reliability. If using XT or LP selectable oscillator options, there is always an 18 ms (nominal) delay provided by the Device Reset Timer (DRT), intended to keep the chip in reset until the crystal oscillator is stable. If using INTRC or EXTRC there is an 18 ms delay only on VDD power-up. With this timer on-chip, most applications need no external reset circuitry.

The SLEEP mode is designed to offer a very low current power-down mode. The user can wake-up from SLEEP through a change on input pins or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application, including an internal 4 MHz oscillator. The EXTRC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

8.1 Configuration Bits

The PIC12C5XX configuration word consists of 12 bits. Configuration bits can be programmed to select various device configurations. Two bits are for the selection of the oscillator type, one bit is the Watchdog Timer enable bit, and one bit is the MCLR enable bit.

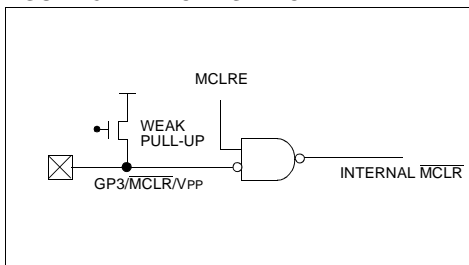
FIGURE 8-1: CONFIGURATION WORD FOR PIC12C5XX

—	—	—	—	—	—	—	MCLRE	CP	WDTE	FOSC1	FOSC0	Register: CONFIG
bit11	10	9	8	7	6	5	4	3	2	1	bit0	Address ⁽¹⁾ : FFFh
bit 11-5: Unimplemented												
bit 4: MCLRE: MCLR enable bit.												
1 = MCLR pin enabled												
0 = MCLR tied to VDD, (Internally)												
bit 3: CP: Code protection bit.												
1 = Code protection off												
0 = Code protection on												
bit 2: WDTE: Watchdog timer enable bit												
1 = WDT enabled												
0 = WDT disabled												
bit 1-0: FOSC1:FOSC0: Oscillator selection bits												
11 = EXTRC - external RC oscillator												
10 = INTRC - internal RC oscillator												
01 = XT oscillator												
00 = LP oscillator												
Note 1: Refer to the PIC12C5XX Programming Specifications to determine how to access the configuration word. This register is not user addressable during device operation.												

8.3.1 $\overline{\text{MCLR}}$ ENABLE

This configuration bit when unprogrammed (left in the '1' state) enables the external $\overline{\text{MCLR}}$ function. When programmed, the $\overline{\text{MCLR}}$ function is tied to the internal VDD , and the pin is assigned to be a GPIO. See Figure 8-7. When pin GP3/ $\overline{\text{MCLR}}$ / VPP is configured as $\overline{\text{MCLR}}$, the internal pull-up is always on.

FIGURE 8-7: $\overline{\text{MCLR}}$ SELECT



8.4 Power-On Reset (POR)

The PIC12C5XX family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip reset for most power-up situations.

The on-chip POR circuit holds the chip in reset until VDD has reached a high enough level for proper operation. To take advantage of the internal POR, program the GP3/ $\overline{\text{MCLR}}$ / VPP pin as $\overline{\text{MCLR}}$ and tie through a resistor to VDD or program the pin as GP3. An internal weak pull-up resistor is implemented using a transistor. Refer to Table 11-1 for the pull-up resistor ranges. This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified. See Electrical Specifications for details.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, ...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating parameters are met.

A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 8-8.

The Power-On Reset circuit and the Device Reset Timer (Section 8.5) circuit are closely related. On power-up, the reset latch is set and the DRT is reset. The DRT timer begins counting once it detects $\overline{\text{MCLR}}$ to be high. After the time-out period, which is typically 18 ms, it will reset the reset latch and thus end the on-chip reset signal.

A power-up example where $\overline{\text{MCLR}}$ is held low is shown in Figure 8-9. VDD is allowed to rise and stabilize before bringing $\overline{\text{MCLR}}$ high. The chip will actually come out of reset TDRT msec after $\overline{\text{MCLR}}$ goes high.

In Figure 8-10, the on-chip Power-On Reset feature is being used ($\overline{\text{MCLR}}$ and VDD are tied together or the pin is programmed to be GP3.). The VDD is stable before the start-up timer times out and there is no problem in getting a proper reset. However, Figure 8-11 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses that $\overline{\text{MCLR}}$ is high and when $\overline{\text{MCLR}}$ (and VDD) actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the $\text{VDD}(\text{min})$ value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 8-10).

Note: When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For additional information refer to Application Notes "Power-Up Considerations" - AN522 and "Power-up Trouble Shooting" - AN607.

FIGURE 8-8: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

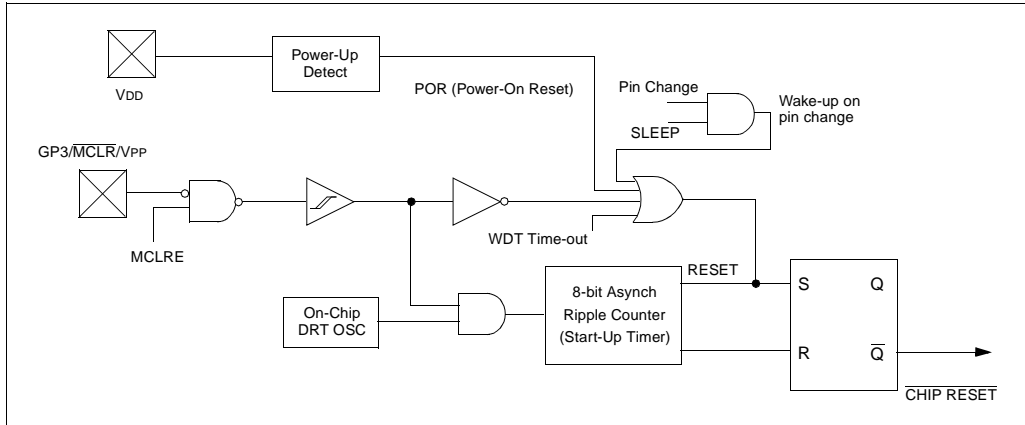


FIGURE 8-9: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ PULLED LOW)

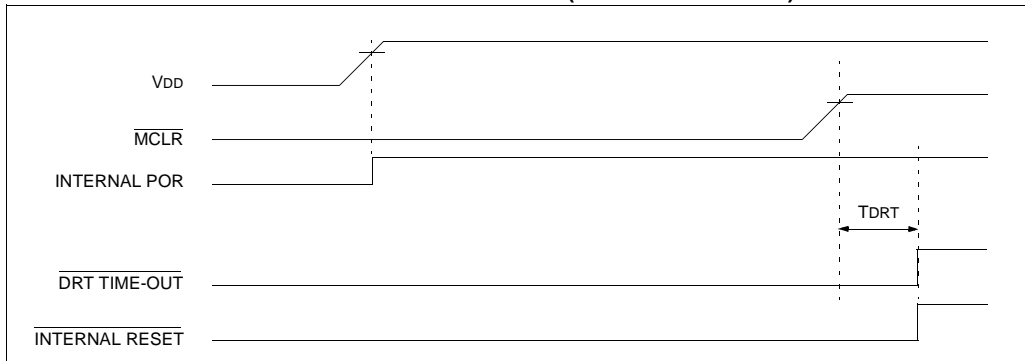
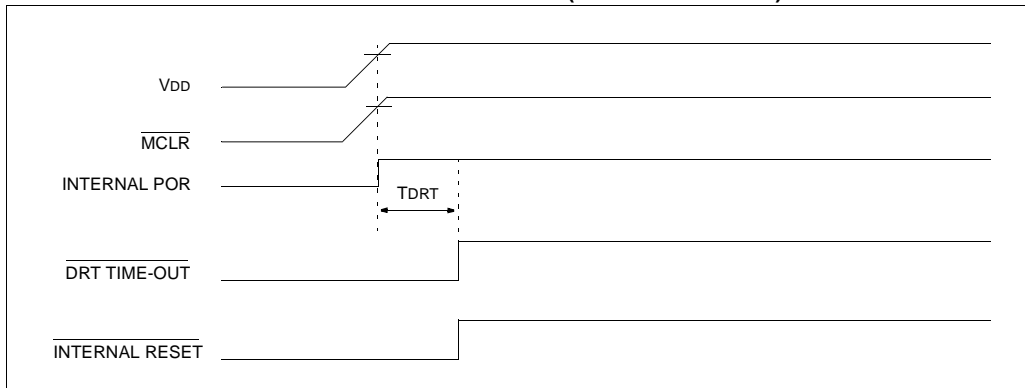


FIGURE 8-10: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD}): FAST V_{DD} RISE TIME



10.16 KEELOQ[®] Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.

11.0 ELECTRICAL CHARACTERISTICS - PIC12C508/PIC12C509

Absolute Maximum Ratings†

Ambient Temperature under bias	–40°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on VDD with respect to VSS	0 to +7.5 V
Voltage on MCLR with respect to VSS.....	0 to +14 V
Voltage on all other pins with respect to VSS	–0.6 V to (VDD + 0.6 V)
Total Power Dissipation ⁽¹⁾	700 mW
Max. Current out of VSS pin	200 mA
Max. Current into VDD pin	150 mA
Input Clamp Current, I _{IK} (V _I < 0 or V _I > VDD).....	±20 mA
Output Clamp Current, I _{OK} (V _O < 0 or V _O > VDD).....	±20 mA
Max. Output Current sunk by any I/O pin.....	25 mA
Max. Output Current sourced by any I/O pin.....	25 mA
Max. Output Current sourced by I/O port (GPIO)	100 mA
Max. Output Current sunk by I/O port (GPIO)	100 mA

Note 1: Power Dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIC12C5XX

TABLE 11-1: PULL-UP RESISTOR RANGES - PIC12C508/C509

V _{DD} (Volts)	Temperature (°C)	Min	Typ	Max	Units
GP0/GP1					
2.5	–40	38K	42K	63K	Ω
	25	42K	48K	63K	Ω
	85	42K	49K	63K	Ω
	125	50K	55K	63K	Ω
5.5	–40	15K	17K	20K	Ω
	25	18K	20K	23K	Ω
	85	19K	22K	25K	Ω
	125	22K	24K	28K	Ω
GP3					
2.5	–40	285K	346K	417K	Ω
	25	343K	414K	532K	Ω
	85	368K	457K	532K	Ω
	125	431K	504K	593K	Ω
5.5	–40	247K	292K	360K	Ω
	25	288K	341K	437K	Ω
	85	306K	371K	448K	Ω
	125	351K	407K	500K	Ω

* These parameters are characterized but not tested.

12.0 DC AND AC CHARACTERISTICS - PIC12C508/PIC12C509

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3 σ) and (mean - 3 σ) respectively, where σ is standard deviation.

FIGURE 12-1: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE (VDD = 2.5V)

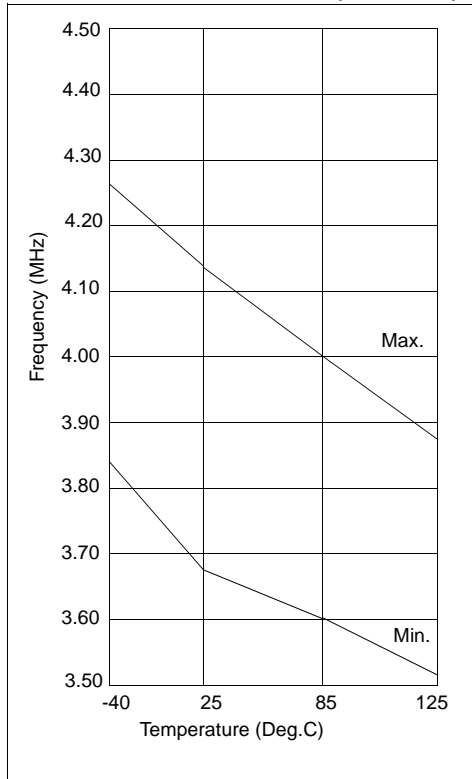
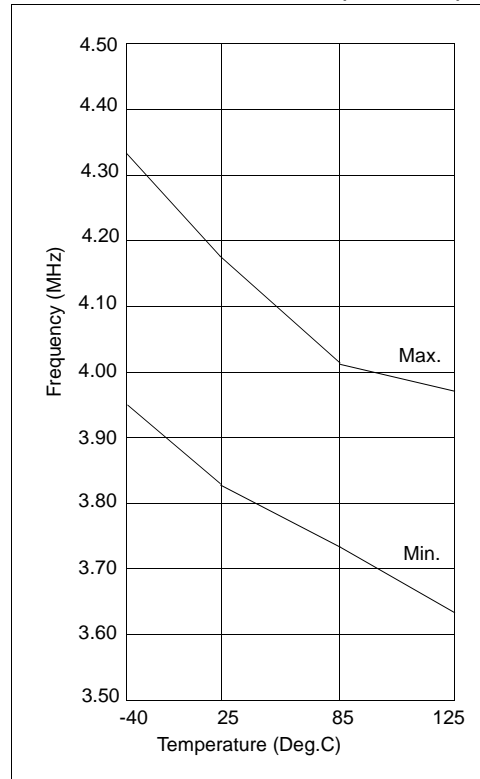


FIGURE 12-2: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE (VDD = 5.0V)



13.4 DC CHARACTERISTICS:

PIC12LC508A/509A (Commercial, Industrial)
PIC12LC518/519 (Commercial, Industrial)
PIC12LCR509A (Commercial, Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise specified)					
		Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)					
		Operating voltage VDD range as described in DC spec Section 13.1 and Section 13.2.					
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D030	Input Low Voltage I/O ports with TTL buffer	VIL	VSS	-	0.8V	V	For 4.5V ≤ VDD ≤ 5.5V otherwise
D031	with Schmitt Trigger buffer		VSS	-	0.15VDD	V	
D032	MCLR, GP2/T0CKI (in EXTRC mode)		VSS	-	0.2VDD	V	
D033	OSC1 (in EXTRC mode)		VSS	-	0.2VDD	V	
D033	OSC1 (in XT and LP)		VSS	-	0.3VDD	V	
D040	Input High Voltage I/O ports with TTL buffer	VIH	0.25VDD + 0.8V	-	VDD	V	4.5V ≤ VDD ≤ 5.5V otherwise For entire VDD range
D040A	with Schmitt Trigger buffer		2.0V	-	VDD	V	
D041	MCLR, GP2/T0CKI		0.8VDD	-	VDD	V	
D042	OSC1 (XT and LP)		0.8VDD	-	VDD	V	
D042A	OSC1 (in EXTRC mode)		0.7VDD	-	VDD	V	
D043	OSC1 (in EXTRC mode)		0.9VDD	-	VDD	V	Note 1
D070	GPIO weak pull-up current (Note 4)	IPUR	30	250	400	μA	VDD = 5V, VPIN = VSS
	MCLR pull-up current	-	-	-	30	μA	VDD = 5V, VPIN = VSS
D060	Input Leakage Current (Notes 2, 3) I/O ports	IIL	-	-	±1	μA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
D061	T0CKI		-	-	±5	μA	VSS ≤ VPIN ≤ VDD
D063	OSC1		-	-	±5	μA	VSS ≤ VPIN ≤ VDD, XT and LP osc configuration
D080	Output Low Voltage I/O ports	VOL	-	-	0.6	V	IoL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D080A			-	-	0.6	V	IoL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
D090	Output High Voltage I/O ports (Note 3)	VOH	VDD - 0.7	-	-	V	IoH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D090A			VDD - 0.7	-	-	V	IoH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
D100	Capacitive Loading Specs on Output Pins OSC2 pin	COSC2	-	-	15	pF	In XT and LP modes when external clock is used to drive OSC1.
D101	All I/O pins	CIO	-	-	50	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

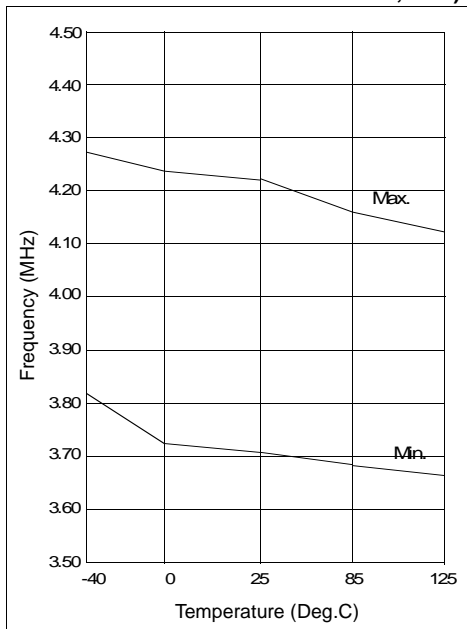
- Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C5XX be driven with external clock in RC mode.
- Note 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- Note 3: Negative current is defined as coming out of the pin.
- Note 4: This spec. applies when GP3/MCLR is configured as MCLR. The leakage current of the MCLR circuit is higher than the standard I/O logic.

14.0 DC AND AC CHARACTERISTICS - PIC12C508A/PIC12C509A/ PIC12LC508A/PIC12LC509A, PIC12CE518/PIC12CE519/PIC12CR509A/ PIC12LCE518/PIC12LCE519/ PIC12LCR509A

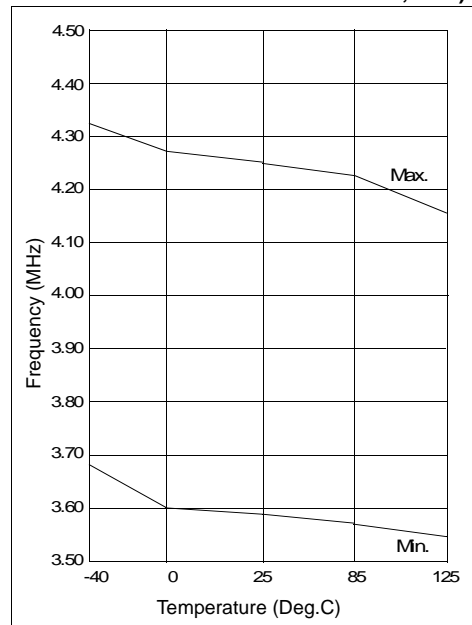
The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified V_{DD} range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean - 3σ) respectively, where σ is standard deviation.

**FIGURE 14-1: CALIBRATED INTERNAL RC
FREQUENCY RANGE VS.
TEMPERATURE ($V_{DD} = 5.0V$)
(INTERNAL RC IS
CALIBRATED TO 25°C, 5.0V)**

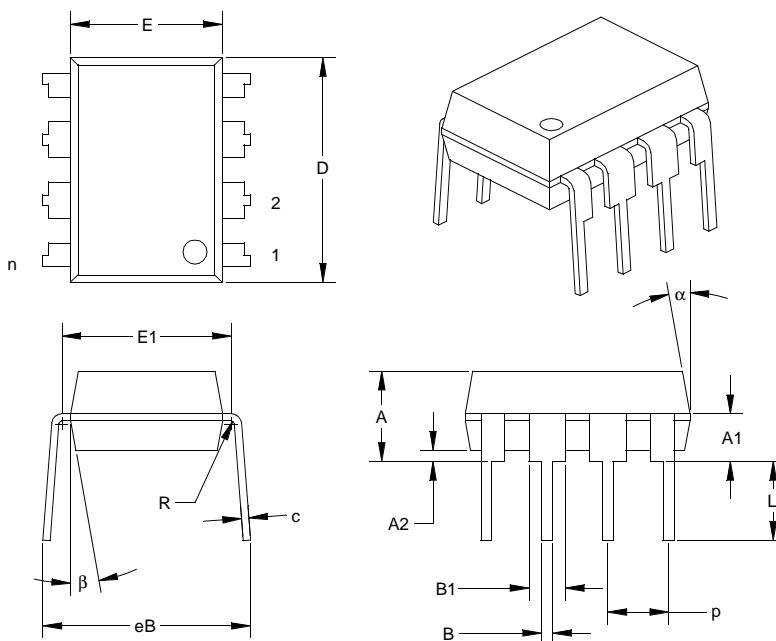


**FIGURE 14-2: CALIBRATED INTERNAL RC
FREQUENCY RANGE VS.
TEMPERATURE ($V_{DD} = 2.5V$)
(INTERNAL RC IS
CALIBRATED TO 25°C, 5.0V)**



PIC12C5XX

Package Type: K04-018 8-Lead Plastic Dual In-line (P) – 300 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		8			8	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.014	0.018	0.022	0.36	0.46	0.56
Upper Lead Width	B1†	0.055	0.060	0.065	1.40	1.52	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.006	0.012	0.015	0.20	0.29	0.38
Top to Seating Plane	A	0.140	0.150	0.160	3.56	3.81	4.06
Top of Lead to Seating Plane	A1	0.060	0.080	0.100	1.52	2.03	2.54
Base to Seating Plane	A2	0.005	0.020	0.035	0.13	0.51	0.89
Tip to Seating Plane	L	0.120	0.130	0.140	3.05	3.30	3.56
Package Length	D‡	0.355	0.370	0.385	9.02	9.40	9.78
Molded Package Width	E‡	0.245	0.250	0.260	6.22	6.35	6.60
Radius to Radius Width	E1	0.267	0.280	0.292	6.78	7.10	7.42
Overall Row Spacing	eB	0.310	0.342	0.380	7.87	8.67	9.65
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

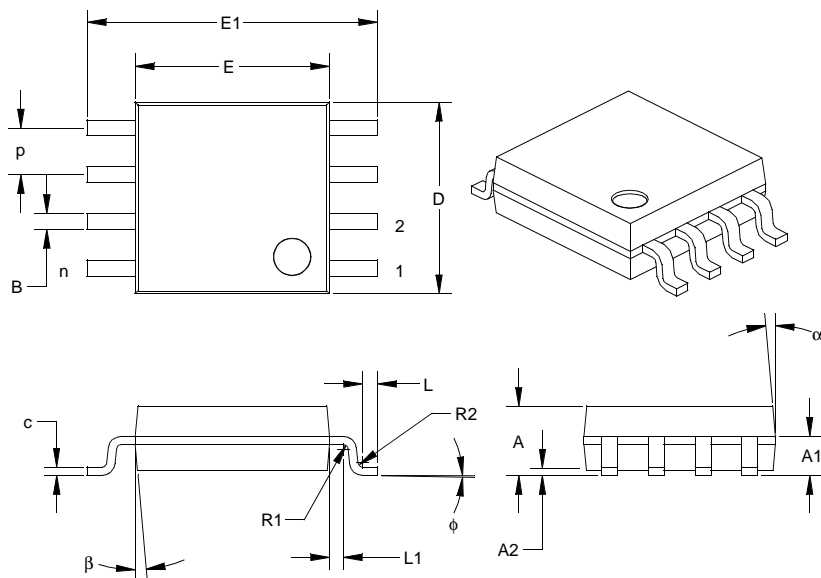
* Controlling Parameter.

† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

PIC12C5XX

Package Type: K04-056 8-Lead Plastic Small Outline (SM) – Medium, 208 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.050			1.27	
Number of Pins	n		8			8	
Overall Pack. Height	A	0.070	0.074	0.079	1.78	1.89	2.00
Shoulder Height	A1	0.037	0.042	0.048	0.94	1.08	1.21
Standoff	A2	0.002	0.005	0.009	0.05	0.14	0.22
Molded Package Length	D [†]	0.200	0.205	0.210	5.08	5.21	5.33
Molded Package Width	E [‡]	0.203	0.208	0.213	5.16	5.28	5.41
Outside Dimension	E1	0.300	0.313	0.325	7.62	7.94	8.26
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	φ	0	4	8	0	4	8
Radius Centerline	L1	0.010	0.015	0.020	0.25	0.38	0.51
Lead Thickness	c	0.008	0.009	0.010	0.19	0.22	0.25
Lower Lead Width	B [†]	0.014	0.017	0.020	0.36	0.43	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter.

† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

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