Microchip Technology - PIC12CE518-04E/SM Datasheet

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	16 x 8
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.209", 5.30mm Width)
Supplier Device Package	8-SOIJ
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12ce518-04e-sm

2.0 PIC12C5XX DEVICE VARIETIES

A variety of packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC12C5XX Product Identification System at the back of this data sheet to specify the correct part number.

2.1 UV Erasable Devices

The UV erasable version, offered in ceramic side brazed package, is optimal for prototype development and pilot programs.

The UV erasable version can be erased and reprogrammed to any of the configuration modes.

Note:	Please note that erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be saved prior to erasing the part.

Microchip's PICSTART® PLUS and PRO MATE® programmers all support programming of the PIC12C5XX. Third party programmers also are available; refer to the *Microchip Third Party Guide* for a list of sources.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates or small volume applications.

The OTP devices, packaged in plastic packages permit the user to program them once. In addition to the program memory, the configuration bits must also be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround Production (SQTP℠) Devices

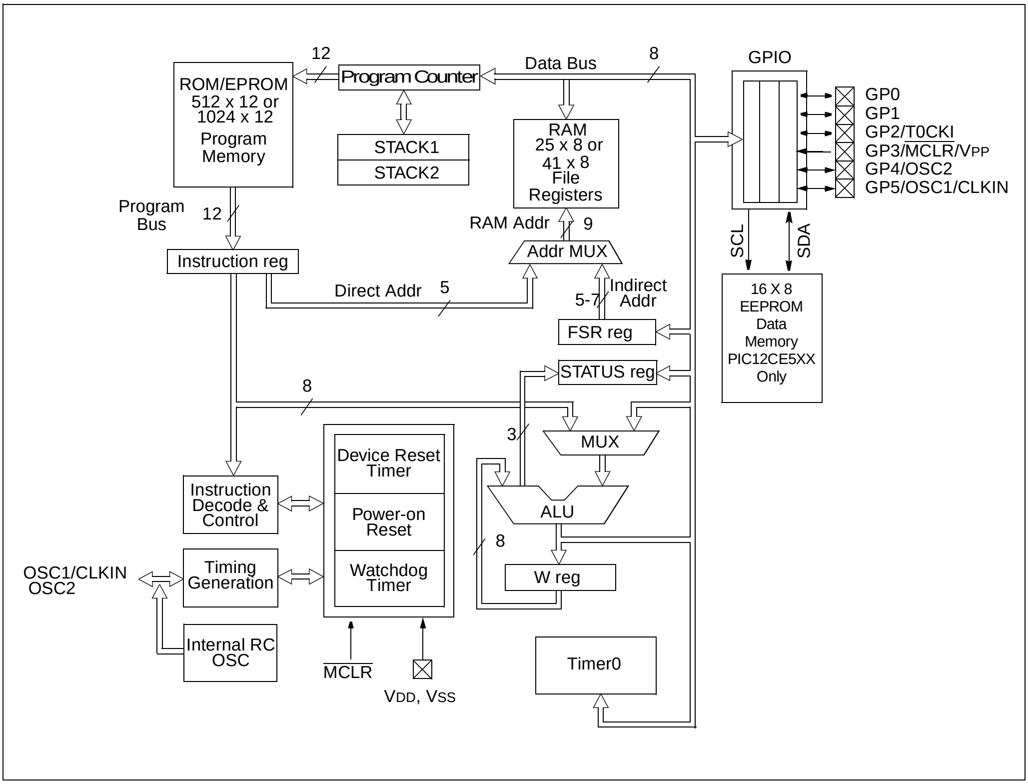
Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

2.5 Read Only Memory (ROM) Device

Microchip offers masked ROM to give the customer a low cost option for high volume, mature products.

FIGURE 3-1: PIC12C5XX BLOCK DIAGRAM



4.4 OPTION Register

The OPTION register is a 8-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the `OPTION` instruction, the contents of the W register will be transferred to the OPTION register. A RESET sets the OPTION<7:0> bits.

Note:	If TRIS bit is set to ‘0’, the wake-up on change and pull-up functions are disabled for that pin; i.e., note that TRIS overrides OPTION control of $\overline{\text{GPPU}}$ and $\overline{\text{GPWU}}$.
Note:	If the T0CS bit is set to ‘1’, GP2 is forced to be an input even if TRIS GP2 = ‘0’.

FIGURE 4-5: OPTION REGISTER

W-1	W-1	W-1	W-1	W-1	W-1	W-1	W-1
$\overline{\text{GPWU}}$	$\overline{\text{GPPU}}$	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7	6	5	4	3	2	1	bit0

W = Writable bit
U = Unimplemented bit
- n = Value at POR reset
Reference Table 4-1 for other resets.

bit 7: **$\overline{\text{GPWU}}$:** Enable wake-up on pin change (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 6: **$\overline{\text{GPPU}}$**: Enable weak pull-ups (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 5: **T0CS**: Timer0 clock source select bit
1 = Transition on T0CKI pin
0 = Transition on internal instruction cycle clock, Fosc/4

bit 4: **T0SE**: Timer0 source edge select bit
1 = Increment on high to low transition on the T0CKI pin
0 = Increment on low to high transition on the T0CKI pin

bit 3: **PSA**: Prescaler assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0: **PS2:PS0**: Prescaler rate select bits

Bit Value	Timer0 Rate	WDT Rate
`000`	1 : 2	1 : 1
`001`	1 : 4	1 : 2
`010`	1 : 8	1 : 4
`011`	1 : 16	1 : 8
`100`	1 : 32	1 : 16
`101`	1 : 64	1 : 32
`110`	1 : 128	1 : 64
`111`	1 : 256	1 : 128

4.5 OSCCAL Register

The Oscillator Calibration (OSCCAL) register is used to calibrate the internal 4 MHz oscillator. It contains four to six bits for calibration. Increasing the cal value increases the frequency. See Section 7.2.5 for more information on the internal oscillator.

FIGURE 4-6: OSCCAL REGISTER (ADDRESS 05h) FOR PIC12C508 AND PIC12C509

R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	U-0	U-0
CAL3	CAL2	CAL1	CAL0	—	—	—	—
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
- n = Value at POR reset

bit 7-4: **CAL<3:0>:** Calibration

bit 3-0: **Unimplemented:** Read as ’0’

FIGURE 4-7: OSCCAL REGISTER (ADDRESS 05h) FOR PIC12C508A/C509A/CR509A/12CE518/12CE519

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	—
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
- n = Value at POR reset

bit 7-2: **CAL<5:0>:** Calibration

bit 1-0: **Unimplemented:** Read as ’0’

4.6 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

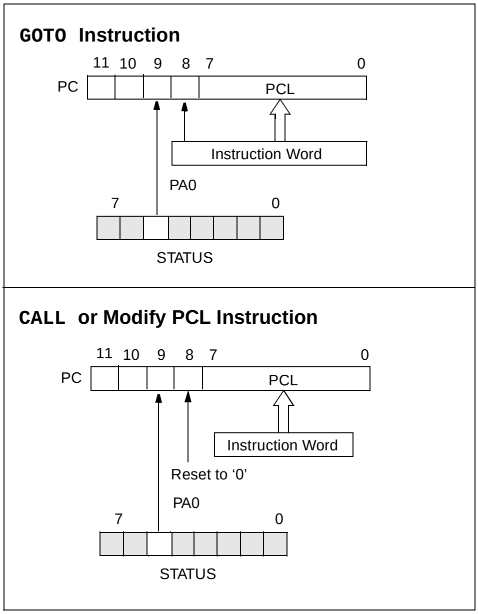
For a `GOTO` instruction, bits 8:0 of the PC are provided by the `GOTO` instruction word. The PC Latch (PCL) is mapped to PC<7:0>. Bit 5 of the STATUS register provides page information to bit 9 of the PC (Figure 4-8).

For a `CALL` instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-8).

Instructions where the PCL is the destination, or Modify PCL instructions, include `MOVWF PC`, `ADDWF PC`, and `BSF PC,5`.

Note: Because PC<8> is cleared in the `CALL` instruction, or any Modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-8: LOADING OF PC BRANCH INSTRUCTIONS - PIC12C5XX



4.6.1 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page i.e., the oscillator calibration instruction. After executing MOVLW XX, the PC will roll over to location 00h, and begin executing user code.

The STATUS register page preselect bits are cleared upon a RESET, which means that page 0 is pre-selected.

Therefore, upon a RESET, a `GOTO` instruction will automatically cause the program to jump to page 0 until the value of the page bits is altered.

4.7 Stack

PIC12C5XX devices have a 12-bit wide L.I.F.O. hardware push/pop stack.

A `CALL` instruction will *push* the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential `CALL`'s are executed, only the most recent two return addresses are stored.

A `RETLW` instruction will *pop* the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential `RETLW`'s are executed, the stack will be filled with the address previously stored in level 2. Note that the W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

Upon any reset, the contents of the stack remain unchanged, however the program counter (PCL) will also be reset to 0.

Note 1: There are no STATUS bits to indicate stack overflows or stack underflow conditions.

Note 2: There are no instructions mnemonics called PUSH or POP. These are actions that occur from the execution of the `CALL` and `RETLW` instructions.

FIGURE 6-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE

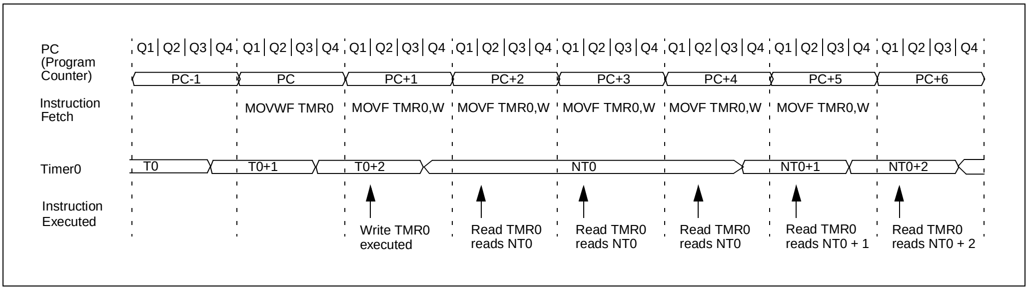


FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

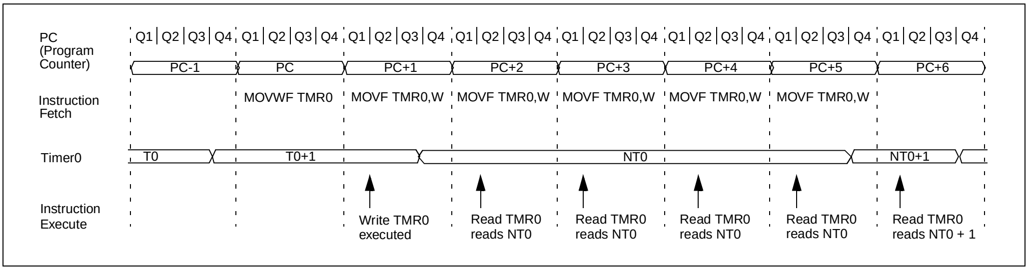


TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
01h	TMR0	Timer0 - 8-bit real-time clock/counter								`xxxx xxxx`	`uuuu uuuu`
N/A	OPTION	$\overline{\text{GPWU}}$	$\overline{\text{GPPU}}$	T0CS	T0SE	PSA	PS2	PS1	PS0	`1111 1111`	`1111 1111`
N/A	TRIS	—	—	GP5	GP4	GP3	GP2	GP1	GP0	`--11 1111`	`--11 1111`

Legend: Shaded cells not used by Timer0, - = unimplemented, x = unknown, u = unchanged,

7.0 EEPROM PERIPHERAL OPERATION

This section applies to PIC12CE518 and PIC12CE519 only.

The PIC12CE518 and PIC12CE519 each have 16 bytes of EEPROM data memory. The EEPROM memory has an endurance of 1,000,000 erase/write cycles and a data retention of greater than 40 years. The EEPROM data memory supports a bi-directional 2-wire bus and data transmission protocol. These two-wires are serial data (SDA) and serial clock (SCL), that are mapped to bit6 and bit7, respectively, of the GPIO register (SFR 06h). Unlike the GP0-GP5 that are connected to the I/O pins, SDA and SCL are only connected to the internal EEPROM peripheral. For most applications, all that is required is calls to the following functions:

```
; Byte_Write: Byte write routine
;      Inputs: EEPROM Address     EEADDR
;              EEPROM Data        EEDATA
;      Outputs:   Return 01 in W if OK, else
;                 return 00 in W
;
; Read_Current: Read EEPROM at address
currently held by EE device.
;      Inputs: NONE
;      Outputs:   EEPROM Data    EEDATA
;                 Return 01 in W if OK, else
;                 return 00 in W
;
; Read_Random: Read EEPROM byte at supplied
address
;      Inputs: EEPROM Address     EEADDR
;      Outputs:   EEPROM Data    EEDATA
;                 Return 01 in W if OK,
;                 else return 00 in W
```

The code for these functions is available on our website www.microchip.com. The code will be accessed by either including the source code FL51XINC.ASM or by linking FLASH5IX.ASM.

It is very important to check the return codes when using these calls, and retry the operation if unsuccessful. Unsuccessful return codes occur when the EE data memory is busy with the previous write, which can take up to 4 mS.

7.0.1 SERIAL DATA

SDA is a bi-directional pin used to transfer addresses and data into and data out of the device.

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

The EEPROM interface is a 2-wire bus protocol consisting of data (SDA) and a clock (SCL). Although these lines are mapped into the GPIO register, they are not accessible as external pins; only to the internal EEPROM peripheral. SDA and SCL operation is also slightly different than GPO-GP5 as listed below. Namely, to avoid code overhead in modifying the TRIS register, both SDA and SCL are always outputs. To read data from the EEPROM peripheral requires outputting a ‘1’ on SDA placing it in high-Z state, where only the internal 100K pull-up is active on the SDA line.

SDA:
  Built-in 100K (typical) pull-up to VDD
  Open-drain (pull-down only)
  Always an output
  Outputs a ‘1’ on reset
SCL:
  Full CMOS output
  Always an output
  Outputs a ‘1’ on reset

The following example requires:

- Code Space: 77 words
- RAM Space: 5 bytes (4 are overlayable)
- Stack Levels:1 (The call to the function itself. The functions do not call any lower level functions.)
- Timing:
  - WRITE_BYTE takes 328 cycles
  - READ_CURRENT takes 212 cycles
  - READ_RANDOM takes 416 cycles.
- IO Pins: 0 (No external IO pins are used)

This code must reside in the lower half of a page. The code achieves it’s small size without additional calls through the use of a sequencing table. The table is a list of procedures that must be called in order. The table uses an ADDWF PCL,F instruction, effectively a computed goto, to sequence to the next procedure. However the ADDWF PCL,F instruction yields an 8 bit address, forcing the code to reside in the first 256 addresses of a page.

8.2 Oscillator Configurations

8.2.1 OSCILLATOR TYPES

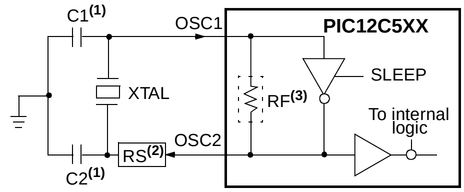
The PIC12C5XX can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

- LP: Low Power Crystal
- XT: Crystal/Resonator
- INTRC: Internal 4 MHz Oscillator
- EXTRC: External Resistor/Capacitor

8.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT or LP modes, a crystal or ceramic resonator is connected to the GP5/OSC1/CLKIN and GP4/OSC2 pins to establish oscillation (Figure 8-2). The PIC12C5XX oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT or LP modes, the device can have an external clock source drive the GP5/OSC1/CLKIN pin (Figure 8-3).

FIGURE 8-2: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (XT OR LP OSC CONFIGURATION)



Note 1: See Capacitor Selection tables for recommended values of C1 and C2.
2: A series resistor (RS) may be required for AT strip cut crystals.
3: RF approximate value = 10 MΩ.

FIGURE 8-3: EXTERNAL CLOCK INPUT OPERATION (XT OR LP OSC CONFIGURATION)

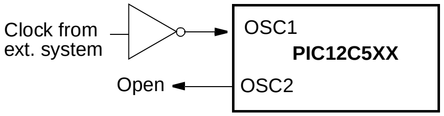


TABLE 8-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS - PIC12C5XX

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
XT	4.0 MHz	30 pF	30 pF

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 8-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - PIC12C5XX

Osc Type	Resonator Freq	Cap.Range C1	Cap. Range C2
LP	32 kHz[1]	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF

Note 1: For $V_{DD} > 4.5V$, $C1 = C2 \approx 30$ pF is recommended.

These values are for design guidance only. Rs may be required to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

8.2.5 INTERNAL 4 MHz RC OSCILLATOR

The internal RC oscillator provides a fixed 4 MHz (nominal) system clock at VDD = 5V and 25°C, see "Electrical Specifications" section for information on variation over voltage and temperature.

In addition, a calibration instruction is programmed into the top of memory which contains the calibration value for the internal RC oscillator. This location is never code protected regardless of the code protect settings. This value is programmed as a `MOVLW XX` instruction where XX is the calibration value, and is placed at the reset vector. This will load the W register with the calibration value upon reset and the PC will then roll over to the users program at address 0x000. The user then has the option of writing the value to the OSCCAL Register (05h) or ignoring it.

OSCCAL, when written to with the calibration value, will "trim" the internal oscillator to remove process variation from the oscillator frequency. .

> **Note:** Please note that erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be read prior to erasing the part. so it can be reprogrammed correctly later.

For the PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, and PIC12CR509A, bits <7:2>, CAL5-CAL0 are used for calibration. Adjusting CAL5-0 from 000000 to 111111 yields a higher clock speed. Note that bits 1 and 0 of OSCCAL are unimplemented and should be written as 0 when modifying OSCCAL for compatibility with future devices.

For the PIC12C508 and PIC12C509, the upper 4 bits of the register are used. Writing a larger value in this location yields a higher clock speed.

8.3 RESET

The device differentiates between various kinds of reset:

a) Power on reset (POR)

b) $\overline{\text{MCLR}}$ reset during normal operation

c) $\overline{\text{MCLR}}$ reset during SLEEP

d) WDT time-out reset during normal operation

e) WDT time-out reset during SLEEP

f) Wake-up from SLEEP on pin change

Some registers are not reset in any way; they are unknown on POR and unchanged in any other reset. Most other registers are reset to "reset state" on power-on reset (POR), $\overline{\text{MCLR}}$, WDT or wake-up on pin change reset during normal operation. They are not affected by a WDT reset during SLEEP or $\overline{\text{MCLR}}$ reset during SLEEP, since these resets are viewed as resumption of normal operation. The exceptions to this are $\overline{\text{TO}}$, $\overline{\text{PD}}$, and GPWUF bits. They are set or cleared differently in different reset situations. These bits are used in software to determine the nature of reset. See Table 8-3 for a full description of reset states of all registers.

TABLE 8-3: RESET CONDITIONS FOR REGISTERS

Register	Address	Power-on Reset	$\overline{\text{MCLR}}$ Reset WDT time-out Wake-up on Pin Change
W (PIC12C508/509)	—	`qqqq xxxx` (1)	`qqqq uuuu` (1)
W (PIC12C508A/509A/ PIC12CE518/519/ PIC12CE509A)	—	`qqqq qqxx` (1)	`qqqq qquu` (1)
INDF	00h	`xxxx xxxx`	`uuuu uuuu`
TMR0	01h	`xxxx xxxx`	`uuuu uuuu`
PC	02h	`1111 1111`	`1111 1111`
STATUS	03h	`0001 1xxx`	`q00q quuu` (2,3)
FSR (PIC12C508/ PIC12C508A/ PIC12CE518)	04h	`111x xxxx`	`111u uuuu`
FSR (PIC12C509/ PIC12C509A/ PIC12CE519/ PIC12CR509A)	04h	`110x xxxx`	`11uu uuuu`
OSCCAL (PIC12C508/509)	05h	`0111 ----`	`uuuu ----`
OSCCAL (PIC12C508A/509A/ PIC12CE518/512/ PIC12CR509A)	05h	`1000 00--`	`uuuu uu--`
GPIO (PIC12C508/PIC12C509/ PIC12C508A/ PIC12C509A/ PIC12CR509A)	06h	`--xx xxxx`	`--uu uuuu`
GPIO (PIC12CE518/ PIC12CE519)	06h	`11xx xxxx`	`11uu uuuu`
OPTION	—	`1111 1111`	`1111 1111`
TRIS	—	`--11 1111`	`--11 1111`

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as ‘0’, q = value depends on condition.

Note 1: Bits <7:2> of W register contain oscillator calibration values due to `MOVLW XX` instruction at top of memory.

Note 2: See Table 8-7 for reset value for specific conditions

Note 3: If reset was due to wake-up on pin change, then bit 7 = 1. All other resets will cause bit 7 = 0.

TABLE 8-4: RESET CONDITION FOR SPECIAL REGISTERS

	STATUS Addr: 03h	PCL Addr: 02h
Power on reset	`0001 1xxx`	`1111 1111`
$\overline{\text{MCLR}}$ reset during normal operation	`000u uuuu`	`1111 1111`
$\overline{\text{MCLR}}$ reset during SLEEP	`0001 0uuu`	`1111 1111`
WDT reset during SLEEP	`0000 0uuu`	`1111 1111`
WDT reset normal operation	`0000 uuuu`	`1111 1111`
Wake-up from SLEEP on pin change	`1001 0uuu`	`1111 1111`

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as ‘0’.

SLEEP	**Enter SLEEP Mode**
Syntax:	[*label*] SLEEP
Operands:	None
Operation:	00h → WDT; 0 → WDT prescaler; 1 → $\overline{\text{TO}}$; 0 → $\overline{\text{PD}}$
Status Affected:	$\overline{\text{TO}}$, $\overline{\text{PD}}$, GPWUF
Encoding:	`0000` `0000` `0011`
Description:	Time-out status bit ($\overline{\text{TO}}$) is set. The power down status bit ($\overline{\text{PD}}$) is cleared. GPWUF is unaffected. The WDT and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP for more details.
Words:	1
Cycles:	1
Example:	`SLEEP`

SUBWF	**Subtract W from f**
Syntax:	[*label*] SUBWF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(f) – (W) → (dest)
Status Affected:	C, DC, Z
Encoding:	`0000` `10df` `ffff`
Description:	Subtract (2’s complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.
Words:	1
Cycles:	1

<u>Example 1</u>: `SUBWF REG1, 1`

Before Instruction
REG1 = 3
W = 2
C = ?

After Instruction
REG1 = 1
W = 2
C = 1 ; result is positive

<u>Example 2</u>:

Before Instruction
REG1 = 2
W = 2
C = ?

After Instruction
REG1 = 0
W = 2
C = 1 ; result is zero

<u>Example 3</u>:

Before Instruction
REG1 = 1
W = 2
C = ?

After Instruction
REG1 = FF
W = 2
C = 0 ; result is negative

SWAPF Swap Nibbles in f

Syntax:	[*label*] SWAPF f,d
Operands:	0 ≤ f ≤ 31 d ∈ [0,1]
Operation:	(f<3:0>) → (dest<7:4>); (f<7:4>) → (dest<3:0>)
Status Affected:	None
Encoding:	`0011` | `10df` | `ffff`
Description:	The upper and lower nibbles of register ’f’ are exchanged. If ’d’ is 0 the result is placed in W register. If ’d’ is 1 the result is placed in register ’f’.
Words:	1
Cycles:	1
Example	`SWAPF REG1, 0`

Before Instruction
REG1 = 0xA5

After Instruction
REG1 = 0xA5
W = 0X5A

TRIS Load TRIS Register

Syntax:	[*label*] TRIS f
Operands:	f = 6
Operation:	(W) → TRIS register f
Status Affected:	None
Encoding:	`0000` | `0000` | `0fff`
Description:	TRIS register 'f' (f = 6) is loaded with the contents of the W register
Words:	1
Cycles:	1
Example	`TRIS GPIO`

Before Instruction
W = 0XA5

After Instruction
TRIS = 0XA5

Note: f = 6 for PIC12C5XX only.

XORLW Exclusive OR literal with W

Syntax:	[*label*] XORLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) .XOR. k → (W)
Status Affected:	Z
Encoding:	`1111` | `kkkk` | `kkkk`
Description:	The contents of the W register are XOR’ed with the eight bit literal 'k'. The result is placed in the W register.
Words:	1
Cycles:	1
Example:	`XORLW 0xAF`

Before Instruction
W = 0xB5

After Instruction
W = 0x1A

XORWF Exclusive OR W with f

Syntax:	[*label*] XORWF f,d
Operands:	0 ≤ f ≤ 31 d ∈ [0,1]
Operation:	(W) .XOR. (f) → (dest)
Status Affected:	Z
Encoding:	`0001` | `10df` | `ffff`
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example	`XORWF REG,1`

Before Instruction
REG = 0xAF
W = 0xB5

After Instruction
REG = 0x1A
W = 0xB5

TABLE 10-1: DEVELOPMENT TOOLS FROM MICROCHIP

		PIC12C5XX	PIC14000	PIC16C5X	PIC16CXXX	PIC16C6X	PIC16C7XX	PIC16C8X	PIC16C9XX	PIC17C4X	PIC17C7XX	24CXX 25CXX 93CXX	HCS200 HCS300 HCS301
Emulator Products	**MPLAB™-ICE**	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	ICEPIC™ Low-Cost In-Circuit Emulator			✓	✓	✓	✓	✓	✓				
Software Tools	**MPLAB™ Integrated Development Environment**	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	MPLAB™ C17* Compiler									✓	✓		
	***fuzzy*TECH®-MP Explorer/Edition Fuzzy Logic Dev. Tool**	✓	✓	✓	✓	✓	✓	✓	✓	✓			
	Total Endurance™ Software Model											✓	
Programmers	**PICSTART® Plus Low-Cost Universal Dev. Kit**	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	PRO MATE® II Universal Programmer	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	KEELOQ® Programmer												✓
Demo Boards	**SEEVAL® Designers Kit**											✓	
	SIMICE	✓		✓									
	PICDEM-14A		✓										
	PICDEM-1			✓	✓			✓		✓			
	PICDEM-2					✓	✓						
	PICDEM-3								✓				
	KEELOQ® Evaluation Kit												✓
	KEELOQ Transponder Kit												✓

11.3 Timing Parameter Symbology and Load Conditions - PIC12C508/C509

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

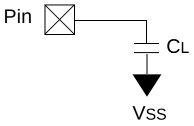
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 11-1: LOAD CONDITIONS - PIC12C508/C509



C_L = 50 pF for all pins except OSC2

15 pF for OSC2 in XT or LP modes when external clock is used to drive OSC1

13.1 DC CHARACTERISTICS: PIC12C508A/509A (Commercial, Industrial, Extended)
PIC12CE518/519 (Commercial, Industrial, Extended)
PIC12CR509A (Commercial, Industrial, Extended)

<table>
<tr><td colspan="2">DC Characteristics
Power Supply Pins</td><td colspan="6">Standard Operating Conditions (unless otherwise specified)
Operating Temperature 0°C ≤ TA ≤ +70°C (commercial)
–40°C ≤ TA ≤ +85°C (industrial)
–40°C ≤ TA ≤ +125°C (extended)</td></tr>
<tr><th>Parm No.</th><th>Characteristic</th><th>Sym</th><th>Min</th><th>Typ(1)</th><th>Max</th><th>Units</th><th>Conditions</th></tr>
<tr><td>D001</td><td>Supply Voltage</td><td>VDD</td><td>3.0</td><td></td><td>5.5</td><td>V</td><td>FOSC = DC to 4 MHz (Commercial/ Industrial, Extended)</td></tr>
<tr><td>D002</td><td>RAM Data Retention Voltage(2)</td><td>VDR</td><td></td><td>1.5*</td><td></td><td>V</td><td>Device in SLEEP mode</td></tr>
<tr><td>D003</td><td>VDD Start Voltage to ensure Power-on Reset</td><td>VPOR</td><td></td><td>VSS</td><td></td><td>V</td><td>See section on Power-on Reset for details</td></tr>
<tr><td>D004</td><td>VDD Rise Rate to ensure Power-on Reset</td><td>SVDD</td><td>0.05*</td><td></td><td></td><td>V/ms</td><td>See section on Power-on Reset for details</td></tr>
<tr><td>D010</td><td>Supply Current(3)</td><td>IDD</td><td>—</td><td>0.8</td><td>1.4</td><td>mA</td><td>XT and EXTRC options (Note 4)
FOSC = 4 MHz, VDD = 5.5V</td></tr>
<tr><td>D010C</td><td></td><td></td><td>—</td><td>0.8</td><td>1.4</td><td>mA</td><td>INTRC Option
FOSC = 4 MHz, VDD = 5.5V</td></tr>
<tr><td>D010A</td><td></td><td></td><td>—</td><td>19</td><td>27</td><td>µA</td><td>LP OPTION, Commercial Temperature
FOSC = 32 kHz, VDD = 3.0V, WDT disabled</td></tr>
<tr><td></td><td></td><td></td><td>—</td><td>19</td><td>35</td><td>µA</td><td>LP OPTION, Industrial Temperature
FOSC = 32 kHz, VDD = 3.0V, WDT disabled</td></tr>
<tr><td></td><td></td><td></td><td>—</td><td>30</td><td>55</td><td>µA</td><td>LP OPTION, Extended Temperature
FOSC = 32 kHz, VDD = 3.0V, WDT disabled</td></tr>
<tr><td>D020</td><td>Power-Down Current (5)</td><td>IPD</td><td>—</td><td>0.25</td><td>4</td><td>µA</td><td>VDD = 3.0V, Commercial WDT disabled</td></tr>
<tr><td>D021</td><td></td><td></td><td>—</td><td>0.25</td><td>5</td><td>µA</td><td>VDD = 3.0V, Industrial WDT disabled</td></tr>
<tr><td>D021B</td><td></td><td></td><td>—</td><td>2</td><td>12</td><td>µA</td><td>VDD = 3.0V, Extended WDT disabled</td></tr>
<tr><td>D022</td><td>Power-Down Current</td><td>ΔIWDT</td><td>—</td><td>2.2</td><td>5</td><td>µA</td><td>VDD = 3.0V, Commercial</td></tr>
<tr><td></td><td></td><td></td><td>—</td><td>2.2</td><td>6</td><td>µA</td><td>VDD = 3.0V, Industrial</td></tr>
<tr><td></td><td></td><td></td><td>—</td><td>4</td><td>11</td><td>µA</td><td>VDD = 3.0V, Extended</td></tr>
<tr><td></td><td>Supply Current (3)
During read/write to EEPROM peripheral</td><td>ΔIEE</td><td>—</td><td>0.1</td><td>0.2</td><td>mA</td><td>FOSC = 4 MHz, Vdd = 5.5V,
SCL = 400kHz</td></tr>
</table>

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to
Vss, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that
the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kOhm.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

15.0 PACKAGING INFORMATION

15.1 Package Marking Information

8-Lead PDIP (300 mil)

```
XXXXXXXX
XXXXXCDE
  AABB
```

Example

```
12C508A
04I/PSAZ
  9825
```

8-Lead SOIC (150 mil)

```
XXXXXXX

   AABB
```

Example

```
C508A

   9825
```

8-Lead SOIC (208 mil)

```
XXXXXXX
XXXXXXX
AABBCDE
```

Example

```
12C508A
04I/SM
9824SAZ
```

8-Lead Windowed Ceramic Side Brazed (300 mil)

```
  XXX

XXXXXX
```

Example

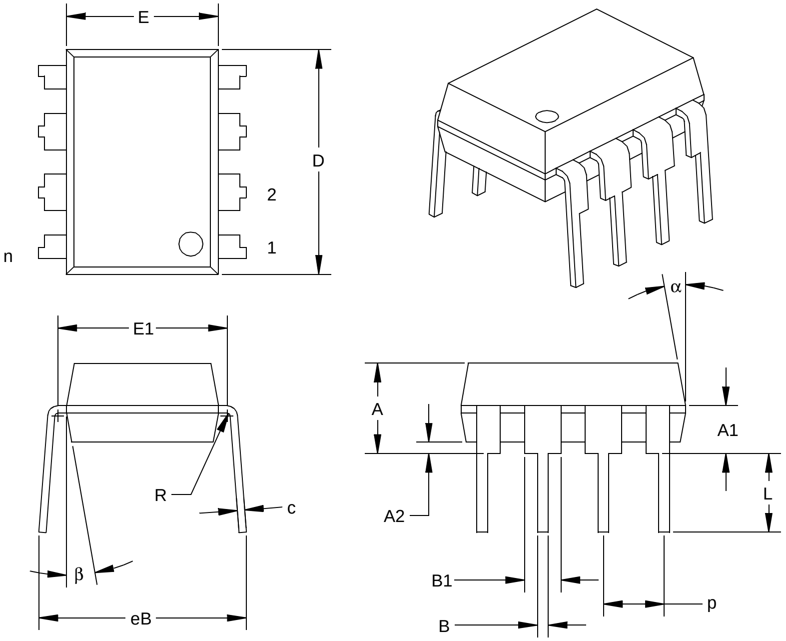
```
  JW

12C508A
```

Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured O = Outside Vendor C = 5" Line S = 6" Line H = 8" Line
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

Package Type: K04-018 8-Lead Plastic Dual In-line (P) – 300 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		8			8	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.014	0.018	0.022	0.36	0.46	0.56
Upper Lead Width	B1[†]	0.055	0.060	0.065	1.40	1.52	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.006	0.012	0.015	0.20	0.29	0.38
Top to Seating Plane	A	0.140	0.150	0.160	3.56	3.81	4.06
Top of Lead to Seating Plane	A1	0.060	0.080	0.100	1.52	2.03	2.54
Base to Seating Plane	A2	0.005	0.020	0.035	0.13	0.51	0.89
Tip to Seating Plane	L	0.120	0.130	0.140	3.05	3.30	3.56
Package Length	D[‡]	0.355	0.370	0.385	9.02	9.40	9.78
Molded Package Width	E[‡]	0.245	0.250	0.260	6.22	6.35	6.60
Radius to Radius Width	E1	0.267	0.280	0.292	6.78	7.10	7.42
Overall Row Spacing	eB	0.310	0.342	0.380	7.87	8.67	9.65
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

[†] Dimension “B1” does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003” (0.076 mm) per side or 0.006” (0.152 mm) more than dimension “B1.”

[‡] Dimensions “D” and “E” do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010” (0.254 mm) per side or 0.020” (0.508 mm) more than dimensions “D” or “E.”

NOTES:

Note the following details of the code protection feature on PICmicro® MCUs.

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable”.
- Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our product.

If you have any further questions about this matter, please contact the local sales office nearest to you.

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip’s products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, FilterLab, KEELOQ, microID, MPLAB, PIC, PICmicro, PICMASTER, PICSTART, PRO MATE, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

dsPIC, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, MXDEV, PICC, PICDEM, PICDEM.net, rfPIC, Select Mode and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A.

Serialized Quick Turn Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2002, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

DNV Certification, Inc.
USA

ANSI • RAB
QMS
ACCREDITED

DNV

DNV MSC
The Netherlands
Accredited by the RvA

ISO 9001 / QS-9000
REGISTERED FIRM

Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999. The Company’s quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs and microperipheral products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001 certified.