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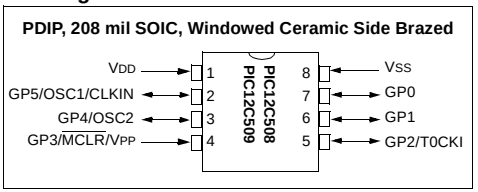
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

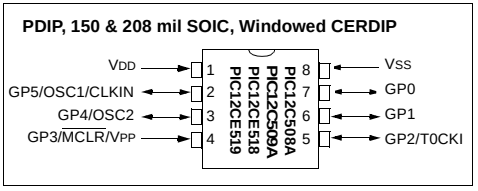
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	16 x 8
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.209", 5.30mm Width)
Supplier Device Package	8-SOIJ
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12ce518-04i-sm

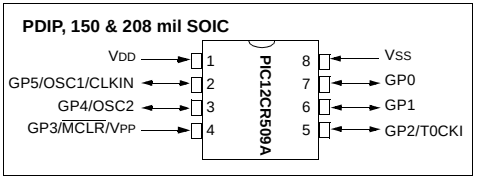
Pin Diagram - PIC12C508/509



Pin Diagram - PIC12C508A/509A, PIC12CE518/519



Pin Diagram - PIC12CR509A



Device Differences

Device	Voltage Range	Oscillator	Oscillator Calibration[2] (Bits)	Process Technology (Microns)
PIC12C508A	3.0-5.5	See Note 1	6	0.7
PIC12LC508A	2.5-5.5	See Note 1	6	0.7
PIC12C508	2.5-5.5	See Note 1	4	0.9
PIC12C509A	3.0-5.5	See Note 1	6	0.7
PIC12LC509A	2.5-5.5	See Note 1	6	0.7
PIC12C509	2.5-5.5	See Note 1	4	0.9
PIC12CR509A	2.5-5.5	See Note 1	6	0.7
PIC12CE518	3.0-5.5	-	6	0.7
PIC12LCE518	2.5-5.5	-	6	0.7
PIC12CE519	3.0-5.5	-	6	0.7
PIC12LCE519	2.5-5.5	-	6	0.7

Note 1: If you change from the PIC12C50X to the PIC12C50XA or to the PIC12CR50XA, please verify oscillator characteristics in your application.

Note 2: See Section 7.2.5 for OSCCAL implementation differences.

TABLE 1-1: PIC12CXXX & PIC12CEXXX FAMILY OF DEVICES

		PIC12C508(A)	PIC12C509(A)	PIC12CR509A	PIC12CE518	PIC12CE519	PIC12C671	PIC12C672	PIC12CE673	PIC12CE674
Clock	Maximum Frequency of Operation (MHz)	4	4	4	4	4	10	10	10	10
Memory	EPROM Program Memory	512 x 12	1024 x 12	1024 x 12 (ROM)	512 x 12	1024 x 12	1024 x 14	2048 x 14	1024 x 14	2048 x 14
	RAM Data Memory (bytes)	25	41	41	25	41	128	128	128	128
Peripherals	EEPROM Data Memory (bytes)	—	—	—	16	16	—	—	16	16
	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0
	A/D Converter (8-bit) Channels	—	—	—	—	—	4	4	4	4
Features	Wake-up from SLEEP on pin change	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Interrupt Sources	—	—	—			4	4	4	4
	I/O Pins	5	5	5	5	5	5	5	5	5
	Input Pins	1	1	1	1	1	1	1	1	1
	Internal Pull-ups	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	In-Circuit Serial Programming	Yes	Yes	—	Yes	Yes	Yes	Yes	Yes	Yes
	Number of Instructions	33	33	33	33	33	35	35	35	35
	Packages	8-pin DIP, JW, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, JW	8-pin DIP, JW

All PIC12CXXX & PIC12CEXXX devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.
All PIC12CXXX & PIC12CEXXX devices use serial programming with data pin GP0 and clock pin GP1.

NOTES:

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC12C5XX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC12C5XX uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12-bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (1µs @ 4MHz) except for program branches.

The table below lists program memory (EPROM), data memory (RAM), ROM memory, and non-volatile (EEPROM) for each device.

Device	Memory			
	EPROM Program	ROM Program	RAM Data	EEPROM Data
PIC12C508	512 x 12		25	
PIC12C509	1024 x 12		41	
PIC12C508A	512 x 12		25	
PIC12C509A	1024 x 12		41	
PIC12CR509A		1024 x 12	41	
PIC12CE518	512 x 12		25 x 8	16 x 8
PIC12CE519	1024 x 12		41 x 8	16 x 8

The PIC12C5XX can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC12C5XX has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC12C5XX simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC12C5XX device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit borrow}}$ out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1.

3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1, and the instruction is fetched from program memory and latched into instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2 and Example 3-1.

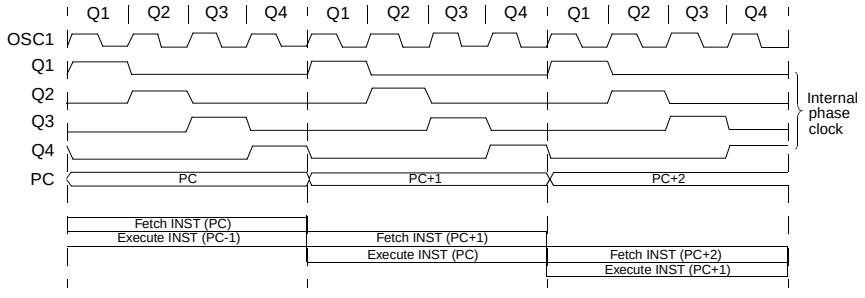
3.2 Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW

```
1. MOVLW 03H
2. MOVWF GPIO
3. CALL  SUB_1
4. BSF   GPIO, BIT1
```

Fetch 1	Execute 1					
	Fetch 2	Execute 2				
		Fetch 3	Execute 3			
			Fetch 4	Flush		
				Fetch SUB_1	Execute SUB_1	

All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is “flushed” from the pipeline while the new instruction is being fetched and then executed.

4.2 Data Memory Organization

Data memory is composed of registers, or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: special function registers and general purpose registers.

The special function registers include the TMR0 register, the Program Counter (PC), the Status Register, the I/O registers (ports), and the File Select Register (FSR). In addition, special purpose registers are used to control the I/O port configuration and prescaler options.

The general purpose registers are used for data and control information under command of the instructions.

For the PIC12C508, PIC12C508A and PIC12CE518, the register file is composed of 7 special function registers and 25 general purpose registers (Figure 4-2).

For the PIC12C509, PIC12C509A, PIC12CR509A, and PIC12CE519 the register file is composed of 7 special function registers, 25 general purpose registers, and 16 general purpose registers that may be addressed using a banking scheme (Figure 4-3).

4.2.1 GENERAL PURPOSE REGISTER FILE

The general purpose register file is accessed either directly or indirectly through the file select register FSR (Section 4.8).

FIGURE 4-2: PIC12C508, PIC12C508A AND PIC12CE518 REGISTER FILE MAP

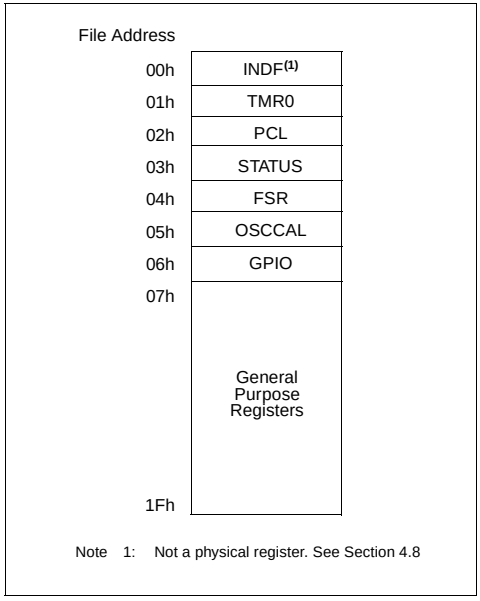
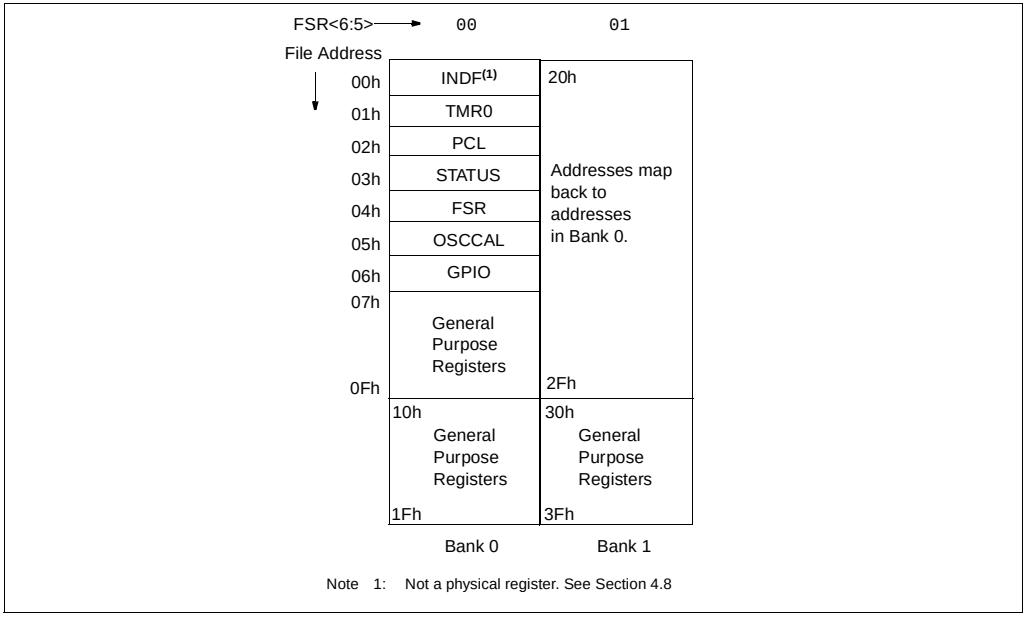


FIGURE 4-3: PIC12C509, PIC12C509A, PIC12CR509A AND PIC12CE519 REGISTER FILE MAP



8.2 Oscillator Configurations

8.2.1 OSCILLATOR TYPES

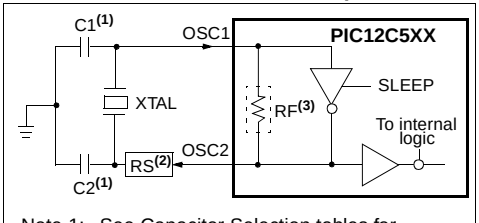
The PIC12C5XX can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

- LP: Low Power Crystal
- XT: Crystal/Resonator
- INTRC: Internal 4 MHz Oscillator
- EXTRC: External Resistor/Capacitor

8.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT or LP modes, a crystal or ceramic resonator is connected to the GP5/OSC1/CLKIN and GP4/OSC2 pins to establish oscillation (Figure 8-2). The PIC12C5XX oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT or LP modes, the device can have an external clock source drive the GP5/OSC1/CLKIN pin (Figure 8-3).

FIGURE 8-2: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (XT OR LP OSC CONFIGURATION)



Note 1: See Capacitor Selection tables for recommended values of C1 and C2.
2: A series resistor (RS) may be required for AT strip cut crystals.
3: RF approximate value = 10 MΩ.

FIGURE 8-3: EXTERNAL CLOCK INPUT OPERATION (XT OR LP OSC CONFIGURATION)

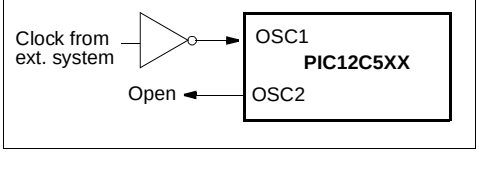


TABLE 8-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS - PIC12C5XX

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
XT	4.0 MHz	30 pF	30 pF

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 8-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - PIC12C5XX

Osc Type	Resonator Freq	Cap.Range C1	Cap. Range C2
LP	32 kHz(1)	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF

Note 1: For V_{DD} > 4.5V, C1 = C2 ≈ 30 pF is recommended.

These values are for design guidance only. Rs may be required to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

ADDWF **Add W and f**

Syntax: [*label*] ADDWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W) + (f) → (dest)

Status Affected: C, DC, Z

Encoding:

0001	11df	ffff

Description: Add the contents of the W register and register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
ADDWF   FSR, 0
```
Before Instruction
W = 0x17
FSR = 0xC2

After Instruction
W = 0xD9
FSR = 0xC2

ANDWF **AND W with f**

Syntax: [*label*] ANDWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W) .AND. (f) → (dest)

Status Affected: Z

Encoding:

0001	01df	ffff

Description: The contents of the W register are AND'ed with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
ANDWF   FSR,    1
```
Before Instruction
W = 0x17
FSR = 0xC2

After Instruction
W = 0x17
FSR = 0x02

ANDLW **And literal with W**

Syntax: [*label*] ANDLW k

Operands: $0 \le k \le 255$

Operation: (W).AND. (k) → (W)

Status Affected: Z

Encoding:

1110	kkkk	kkkk

Description: The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
ANDLW   0x5F
```
Before Instruction
W = 0xA3

After Instruction
W = 0x03

BCF **Bit Clear f**

Syntax: [*label*] BCF f,b

Operands: $0 \le f \le 31$
$0 \le b \le 7$

Operation: 0 → (f<b>)

Status Affected: None

Encoding:

0100	bbbf	ffff

Description: Bit 'b' in register 'f' is cleared.

Words: 1

Cycles: 1

Example:
```
BCF     FLAG_REG,  7
```
Before Instruction
FLAG_REG = 0xC7

After Instruction
FLAG_REG = 0x47

CALL **Subroutine Call**

Syntax: [*label*] CALL k

Operands: 0 ≤ k ≤ 255

Operation: (PC) + 1→ Top of Stack;
k → PC<7:0>;
(STATUS<6:5>) → PC<10:9>;
0 → PC<8>

Status Affected: None

Encoding:

1001	kkkk	kkkk

Description: Subroutine call. First, return address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two cycle instruction.

Words: 1

Cycles: 2

Example:
```
HERE    CALL    THERE
```
Before Instruction
PC = address (HERE)
After Instruction
PC = address (THERE)
TOS = address (HERE + 1)

CLRF **Clear f**

Syntax: [*label*] CLRF f

Operands: 0 ≤ f ≤ 31

Operation: 00h → (f);
1 → Z

Status Affected: Z

Encoding:

0000	011f	ffff

Description: The contents of register 'f' are cleared and the Z bit is set.

Words: 1

Cycles: 1

Example:
```
CLRF    FLAG_REG
```
Before Instruction
FLAG_REG = 0x5A
After Instruction
FLAG_REG = 0x00
Z = 1

CLRW **Clear W**

Syntax: [*label*] CLRW

Operands: None

Operation: 00h → (W);
1 → Z

Status Affected: Z

Encoding:

0000	0100	0000

Description: The W register is cleared. Zero bit (Z) is set.

Words: 1

Cycles: 1

Example:
```
CLRW
```
Before Instruction
W = 0x5A
After Instruction
W = 0x00
Z = 1

CLRWDT **Clear Watchdog Timer**

Syntax: [*label*] CLRWDT

Operands: None

Operation: 00h → WDT;
0 → WDT prescaler (if assigned);
1 → $\overline{TO}$;
1 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

0000	0000	0100

Description: The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

Words: 1

Cycles: 1

Example:
```
CLRWDT
```
Before Instruction
WDT counter = ?
After Instruction
WDT counter = 0x00
WDT prescale = 0
$\overline{TO}$ = 1
$\overline{PD}$ = 1

OPTION **Load OPTION Register**

Syntax: [*label*] OPTION

Operands: None

Operation: (W) → OPTION

Status Affected: None

Encoding:

0000	0000	0010

Description: The content of the W register is loaded into the OPTION register.

Words: 1

Cycles: 1

Example

```
OPTION
```

Before Instruction
W = 0x07

After Instruction
OPTION = 0x07

RETLW **Return with Literal in W**

Syntax: [*label*] RETLW k

Operands: 0 ≤ k ≤ 255

Operation: k → (W);
TOS → PC

Status Affected: None

Encoding:

1000	kkkk	kkkk

Description: The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

Words: 1

Cycles: 2

Example:

```
CALL TABLE ;W contains
           ;table offset
           ;value.
•          ;W now has table
•          ;value.
•
TABLE      ADDWF PC   ;W = offset
           RETLW k1   ;Begin table
           RETLW k2   ;
           •
           •
           •
           RETLW kn   ; End of table
```

Before Instruction
W = 0x07

After Instruction
W = value of k8

RLF **Rotate Left f through Carry**

Syntax: [*label*] RLF f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

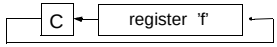
Operation: See description below

Status Affected: C

Encoding:

0011	01df	ffff

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example:

```
RLF     REG1,0
```

Before Instruction
```
REG1    =   1110 0110
C       =   0
```

After Instruction
```
REG1    =   1110 0110
W       =   1100 1100
C       =   1
```

RRF **Rotate Right f through Carry**

Syntax: [*label*] RRF f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

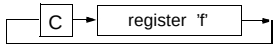
Operation: See description below

Status Affected: C

Encoding:

0011	00df	ffff

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.



Words: 1

Cycles: 1

Example:

```
RRF     REG1,0
```

Before Instruction
```
REG1    =   1110 0110
C       =   0
```

After Instruction
```
REG1    =   1110 0110
W       =   0111 0011
C       =   0
```

SLEEP **Enter SLEEP Mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT;
0 → WDT prescaler;
1 → $\overline{TO}$;
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$, GPWUF

Encoding:

0000	0000	0011

Description: Time-out status bit ($\overline{TO}$) is set. The power down status bit ($\overline{PD}$) is cleared.
GPWUF is unaffected.
The WDT and its prescaler are cleared.
The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP for more details.

Words: 1

Cycles: 1

Example: SLEEP

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) – (W) → (dest)

Status Affected: C, DC, Z

Encoding:

0000	10df	ffff

Description: Subtract (2's complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example 1:

```
SUBWF   REG1, 1
```

Before Instruction
```
REG1    =   3
W       =   2
C       =   ?
```
After Instruction
```
REG1    =   1
W       =   2
C       =   1     ; result is positive
```

Example 2:

Before Instruction
```
REG1    =   2
W       =   2
C       =   ?
```
After Instruction
```
REG1    =   0
W       =   2
C       =   1     ; result is zero
```

Example 3:

Before Instruction
```
REG1    =   1
W       =   2
C       =   ?
```
After Instruction
```
REG1    =   FF
W       =   2
C       =   0     ; result is negative
```

11.2 DC CHARACTERISTICS: PIC12C508/509 (Commercial, Industrial, Extended)

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise specified)** Operating temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating voltage VDD range as described in DC spec Section 11.1 and Section 11.2.				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	Input Low Voltage						
	I/O ports	VIL		-			
D030	with TTL buffer		VSS	-	0.8V	V	4.5 < VDD ≤ 5.5V
				-	0.15VDD	V	otherwise
D031	with Schmitt Trigger buffer		VSS	-	0.15VDD	V	
D032	MCLR, GP2/T0CKI (in EXTRC mode)		VSS	-	0.15VDD	V	
D033	OSC1 (EXTRC) (1)		VSS	-	0.15VDD		
D033	OSC1 (in XT and LP)		VSS	-	0.3VDD	V	Note1
	Input High Voltage						
	I/O ports	VIH		-			
D040	with TTL buffer	VSS	2.0V	-	VDD	V	4.5 ≤ VDD ≤ 5.5V
D040A			0.25VDD + 0.8V	-	VDD	V	otherwise
D041	with Schmitt Trigger buffer		0.85VDD	-	VDD	V	For entire VDD range
D042	MCLR/GP2/T0CKI		0.85VDD	-	VDD	V	
D042A	OSC1 (XT and LP)		0.7VDD	-	VDD	V	Note1
D043	OSC1 (in EXTRC mode)		0.85VDD	-	VDD	V	
D070	GPIO weak pull-up current	IPUR	50	250	400	µA	VDD = 5V, VPIN = VSS
	Input Leakage Current (2, 3)						For VDD ≤5.5V
D060	I/O ports	IIL	-1	0.5	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061	MCLR, GP2/T0CKI		20	130	250	µA	VPIN = VSS + 0.25V(2)
				0.5	+5	µA	VPIN = VDD
D063	OSC1		-3	0.5	+3	µA	Vss ≤ VPIN ≤ VDD, XT and LP options
	Output Low Voltage						
D080	I/O ports/CLKOUT	VOL	-	-	0.6	V	IOL = 8.7 mA, VDD = 4.5V
	Output High Voltage						
D090	I/O ports/CLKOUT (3)	VOH	VDD - 0.7	-	-	V	IOH = -5.4 mA, VDD = 4.5V
	Capacitive Loading Specs on Output Pins						
D100	OSC2 pin	COSC2	-	-	15	pF	In XT and LP modes when external clock is used to drive OSC1.
D101	All I/O pins	CIO	-	-	50	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C5XX be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

TABLE 11-5: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC12C508/C509

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 11.1						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
30	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	2000*	—	—	ns	VDD = 5 V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9*	18*	30*	ms	VDD = 5 V (Commercial)
32	TDRT	Device Reset Timer Period(2)	9*	18*	30*	ms	VDD = 5 V (Commercial)
34	TioZ	I/O Hi-impedance from $\overline{\text{MCLR}}$ Low	—	—	2000*	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 2: See Table 11-6.

TABLE 11-6: DRT (DEVICE RESET TIMER PERIOD - PIC12C508/C509)

Oscillator Configuration	POR Reset	Subsequent Resets
IntRC & ExtRC	18 ms (typical)	300 µs (typical)
XT & LP	18 ms (typical)	18 ms (typical)

FIGURE 11-5: TIMER0 CLOCK TIMINGS - PIC12C508/C509

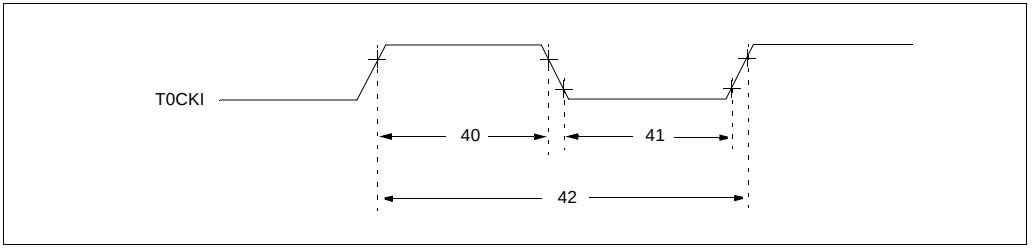


TABLE 11-7: TIMER0 CLOCK REQUIREMENTS - PIC12C508/C509

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 11.1.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{T_{CY} + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

12.0 DC AND AC CHARACTERISTICS - PIC12C508/PIC12C509

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean – 3σ) respectively, where σ is standard deviation.

FIGURE 12-1: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE (VDD = 2.5V)

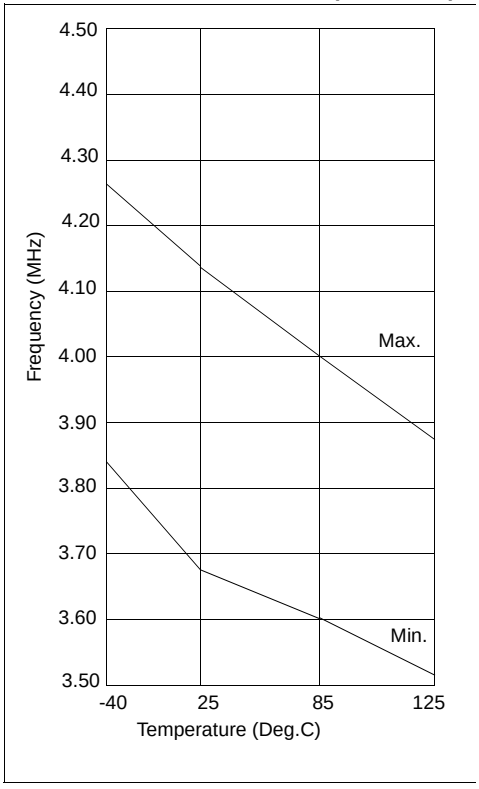
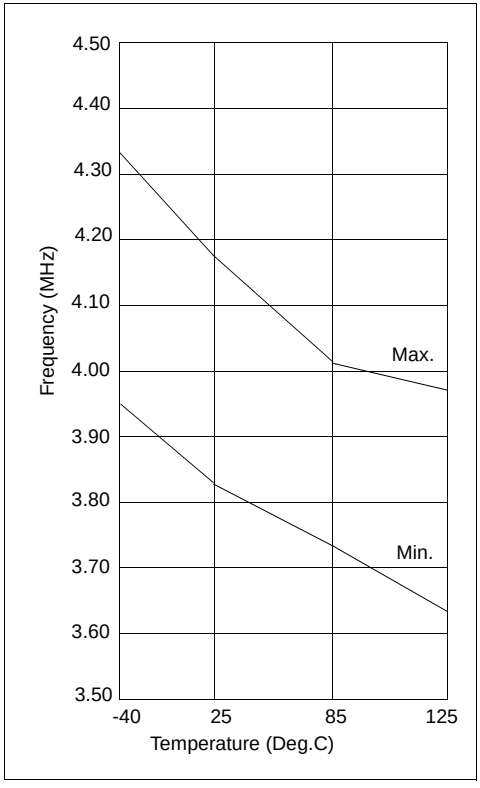


FIGURE 12-2: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE (VDD = 5.0V)



13.3 DC CHARACTERISTICS: PIC12C508A/509A (Commercial, Industrial, Extended) PIC12C518/519 (Commercial, Industrial, Extended) PIC12CR509A (Commercial, Industrial, Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating voltage VDD range as described in DC spec Section 13.1 and Section 13.2.				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	Input Low Voltage						
	I/O ports	VIL					
D030	with TTL buffer		VSS	-	0.8V	V	For 4.5V ≤ VDD ≤ 5.5V
			VSS	-	0.15VDD	V	otherwise
D031	with Schmitt Trigger buffer		VSS	-	0.2VDD	V	
D032	$\overline{MCLR}$, GP2/T0CKI (in EXTRC mode)		VSS	-	0.2VDD	V	
D033	OSC1 (in EXTRC mode)		VSS	-	0.2VDD		Note 1
D033	OSC1 (in XT and LP)		VSS	-	0.3VDD	V	Note 1
	Input High Voltage						
	I/O ports	VIH		-			
D040	with TTL buffer		0.25VDD + 0.8V	-	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			2.0V	-	VDD	V	otherwise
D041	with Schmitt Trigger buffer		0.8VDD	-	VDD	V	For entire VDD range
D042	$\overline{MCLR}$, GP2/T0CKI		0.8VDD	-	VDD	V	
D042A	OSC1 (XT and LP)		0.7VDD	-	VDD	V	Note 1
D043	OSC1 (in EXTRC mode)		0.9VDD	-	VDD	V	
D070	GPIO weak pull-up current (Note 4)	IPUR	30	250	400	µA	VDD = 5V, VPIN = VSS
	$\overline{MCLR}$ pull-up current	-	-	-	30	µA	VDD = 5V, VPIN = VSS
	Input Leakage Current (Notes 2, 3)						
D060	I/O ports	IIL	-	-	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061	T0CKI		-	-	±5	µA	Vss ≤ VPIN ≤ VDD
D063	OSC1		-	-	±5	µA	Vss ≤ VPIN ≤ VDD, XT and LP osc configuration
	Output Low Voltage						
D080	I/O ports	VOL	-	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V, –40°C to +85°C
D080A			-	-	0.6	V	IOL = 7.0 mA, VDD = 4.5V, –40°C to +125°C
	Output High Voltage						
D090	I/O ports (Note 3)	VOH	VDD - 0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, –40°C to +85°C
D090A			VDD - 0.7	-	-	V	IOH = -2.5 mA, VDD = 4.5V, –40°C to +125°C
	Capacitive Loading Specs on Output Pins						
D100	OSC2 pin	COSC2	-	-	15	pF	In XT and LP modes when external clock is used to drive OSC1.
D101	All I/O pins	CIO	-	-	50	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C5XX be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: This spec. applies when GP3/$\overline{MCLR}$ is configured as $\overline{MCLR}$. The leakage current of the $\overline{MCLR}$ circuit is higher than the standard I/O logic.

TABLE 13-1: PULL-UP RESISTOR RANGES* - PIC12C508A, PIC12C509A, PIC12CR509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519

VDD (Volts)	Temperature (°C)	Min	Typ	Max	Units
GP0/GP1					
2.5	–40	38K	42K	63K	Ω
	25	42K	48K	63K	Ω
	85	42K	49K	63K	Ω
	125	50K	55K	63K	Ω
5.5	–40	15K	17K	20K	Ω
	25	18K	20K	23K	Ω
	85	19K	22K	25K	Ω
	125	22K	24K	28K	Ω
GP3					
2.5	–40	285K	346K	417K	Ω
	25	343K	414K	532K	Ω
	85	368K	457K	532K	Ω
	125	431K	504K	593K	Ω
5.5	–40	247K	292K	360K	Ω
	25	288K	341K	437K	Ω
	85	306K	371K	448K	Ω
	125	351K	407K	500K	Ω

***** These parameters are characterized but not tested.

TABLE 13-6: DRT (DEVICE RESET TIMER PERIOD) - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519

Oscillator Configuration	POR Reset	Subsequent Resets
IntRC & ExtRC	18 ms (typical)(1)	300 µs (typical)(1)
XT & LP	18 ms (typical)(1)	18 ms (typical)(1)

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 13-5: TIMER0 CLOCK TIMINGS - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519

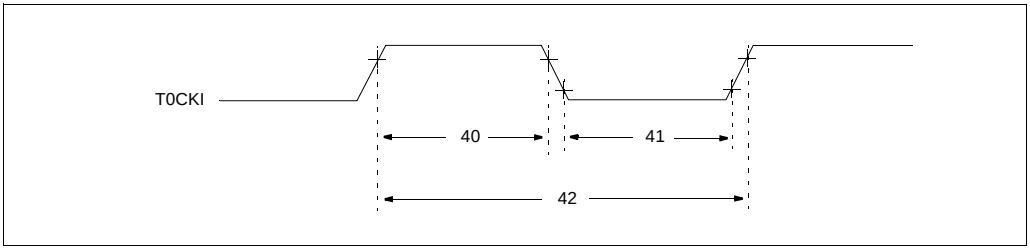


TABLE 13-7: TIMER0 CLOCK REQUIREMENTS - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 13.1.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{T_{CY} + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 13-8: EEPROM MEMORY BUS TIMING REQUIREMENTS - PIC12CE5XX ONLY.

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C, Vcc = 3.0V to 5.5V (commercial) –40°C ≤ TA ≤ +85°C, Vcc = 3.0V to 5.5V (industrial) –40°C ≤ TA ≤ +125°C, Vcc = 4.5V to 5.5V (extended) Operating Voltage VDD range is described in Section 13.1				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Clock frequency	FCLK	— — —	100 100 400	kHz	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 3.0V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Clock high time	THIGH	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 3.0V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Clock low time	TLOW	4700 4700 1300	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 3.0V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
SDA and SCL rise time (Note 1)	TR	— — —	1000 1000 300	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 3.0V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
SDA and SCL fall time	TF	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 3.0V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
START condition setup time	TSU:STA	4700 4700 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 3.0V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Data input hold time	THD:DAT	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250 250 100	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 3.0V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
STOP condition setup time	TSU:STO	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 3.0V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Output valid from clock (Note 2)	TAA	— — —	3500 3500 900	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 3.0V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Bus free time: Time the bus must be free before a new transmission can start	TBUF	4700 4700 1300	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 3.0V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Output fall time from VIH minimum to VIL maximum	TOF	20+0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	ns	(Notes 1, 3)
Write cycle time	TWC	—	4	ms	
Endurance		1M	—	cycles	25°C, VCC = 5.0V, Block Mode (Note 4)

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on Microchip's website.

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