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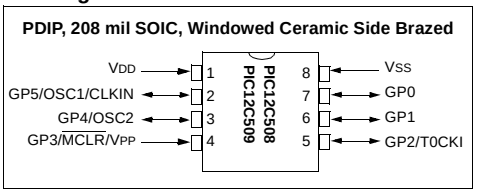
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

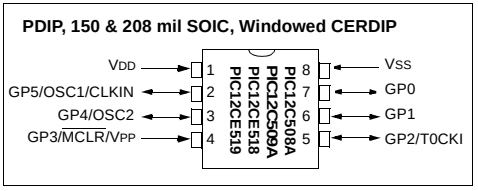
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 5 |
| Program Memory Size | 1.5KB (1K x 12) |
| Program Memory Type | OTP |
| EEPROM Size | 16 x 8 |
| RAM Size | 41 x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 8-SOIC (0.209", 5.30mm Width) |
| Supplier Device Package | 8-SOIJ |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic12ce519-04-sm |

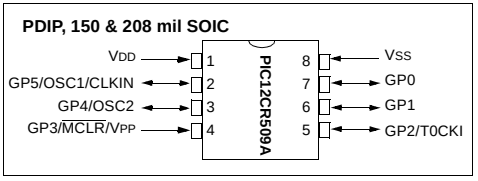
### Pin Diagram - PIC12C508/509




### Pin Diagram - PIC12C508A/509A, PIC12CE518/519




### Pin Diagram - PIC12CR509A




### Device Differences

| Device | Voltage Range | Oscillator | Oscillator Calibration[2] (Bits) | Process Technology (Microns) |
|---|---|---|---|---|
| PIC12C508A | 3.0-5.5 | See Note 1 | 6 | 0.7 |
| PIC12LC508A | 2.5-5.5 | See Note 1 | 6 | 0.7 |
| PIC12C508 | 2.5-5.5 | See Note 1 | 4 | 0.9 |
| PIC12C509A | 3.0-5.5 | See Note 1 | 6 | 0.7 |
| PIC12LC509A | 2.5-5.5 | See Note 1 | 6 | 0.7 |
| PIC12C509 | 2.5-5.5 | See Note 1 | 4 | 0.9 |
| PIC12CR509A | 2.5-5.5 | See Note 1 | 6 | 0.7 |
| PIC12CE518 | 3.0-5.5 | - | 6 | 0.7 |
| PIC12LCE518 | 2.5-5.5 | - | 6 | 0.7 |
| PIC12CE519 | 3.0-5.5 | - | 6 | 0.7 |
| PIC12LCE519 | 2.5-5.5 | - | 6 | 0.7 |

**Note 1:** If you change from the PIC12C50X to the PIC12C50XA or to the PIC12CR50XA, please verify oscillator characteristics in your application.

**Note 2:** See Section 7.2.5 for OSCCAL implementation differences.

**NOTES:**

**NOTES:**

## 6.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
  - Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
  - Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module.

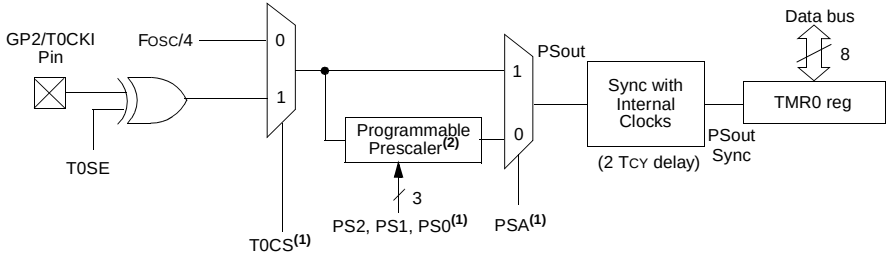
Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two instruction cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The T0SE bit (OPTION<4>) determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.1.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. Section 6.2 details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 6-1.

**FIGURE 6-1: TIMER0 BLOCK DIAGRAM**




Note 1: Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in the OPTION register.
2: The prescaler is shared with the Watchdog Timer (Figure 6-5).

## 6.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer (WDT), respectively (Section 8.6). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1,x`, etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '0's.

### 6.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on the fly” during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

**EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)**

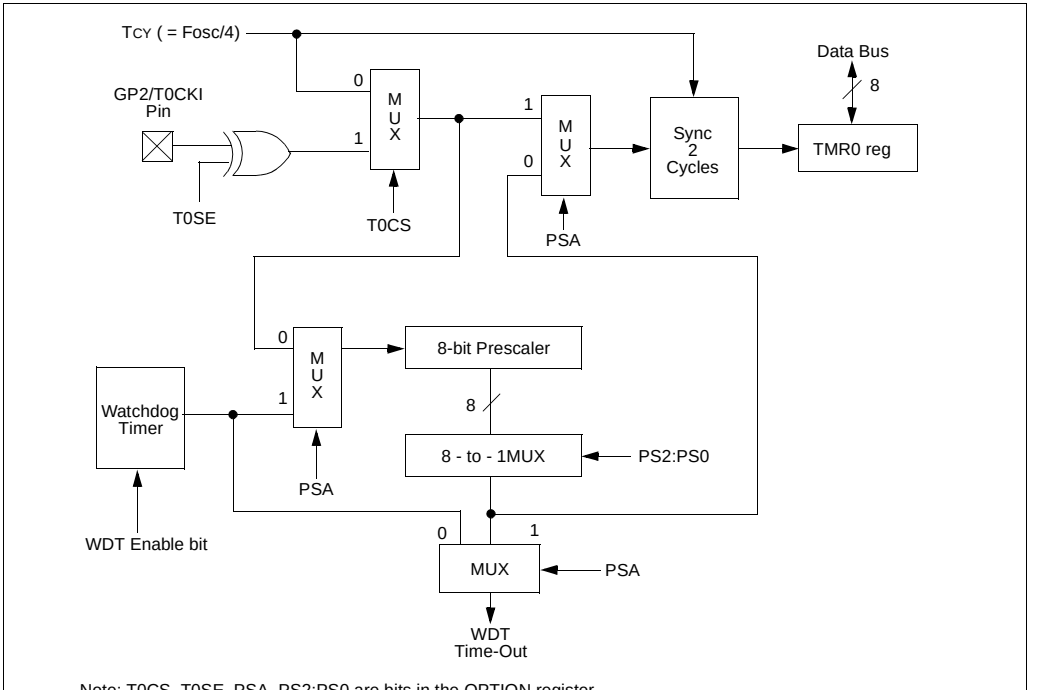
```
1.CLRWDT              ;Clear WDT
2.CLRF   TMR0         ;Clear TMR0 & Prescaler
3.MOVLW  '00xx1111'b  ;These 3 lines (5, 6, 7)
4.OPTION              ; are required only if
                      ; desired
5.CLRWDT              ;PS<2:0> are 000 or 001
6.MOVLW  '00xx1xxx'b  ;Set Postscaler to
7.OPTION              ; desired WDT rate
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 6-2. This sequence must be used even if the WDT is disabled. A `CLRWDT` instruction should be executed before switching the prescaler.

**EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)**

```
CLRWDT                ;Clear WDT and
                      ;prescaler
MOVLW   'xxxx0xxx'    ;Select TMR0, new
                      ;prescale value and
                      ;clock source
OPTION
```

**FIGURE 6-5: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER**




Note: T0CS, T0SE, PSA, PS2:PS0 are bits in the OPTION register.

## 7.0 EEPROM PERIPHERAL OPERATION

**This section applies to PIC12CE518 and PIC12CE519 only.**

The PIC12CE518 and PIC12CE519 each have 16 bytes of EEPROM data memory. The EEPROM memory has an endurance of 1,000,000 erase/write cycles and a data retention of greater than 40 years. The EEPROM data memory supports a bi-directional 2-wire bus and data transmission protocol. These two-wires are serial data (SDA) and serial clock (SCL), that are mapped to bit6 and bit7, respectively, of the GPIO register (SFR 06h). Unlike the GP0-GP5 that are connected to the I/O pins, SDA and SCL are only connected to the internal EEPROM peripheral. For most applications, all that is required is calls to the following functions:

```
; Byte_Write: Byte write routine
;       Inputs: EEPROM Address     EEADDR
;               EEPROM Data        EEDATA
;       Outputs:    Return 01 in W if OK, else
                    return 00 in W
;
; Read_Current: Read EEPROM at address
currently held by EE device.
;       Inputs: NONE
;       Outputs:    EEPROM Data    EEDATA
;                   Return 01 in W if OK, else
                    return 00 in W
;
; Read_Random: Read EEPROM byte at supplied
address
;       Inputs: EEPROM Address     EEADDR
;       Outputs:    EEPROM Data    EEDATA
;                   Return 01 in W if OK,
                    else return 00 in W
```

The code for these functions is available on our website www.microchip.com. The code will be accessed by either including the source code FL51XINC.ASM or by linking FLASH5IX.ASM.

It is very important to check the return codes when using these calls, and retry the operation if unsuccessful. Unsuccessful return codes occur when the EE data memory is busy with the previous write, which can take up to 4 mS.

### 7.0.1 SERIAL DATA

SDA is a bi-directional pin used to transfer addresses and data into and data out of the device.

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

The EEPROM interface is a 2-wire bus protocol consisting of data (SDA) and a clock (SCL). Although these lines are mapped into the GPIO register, they are not accessible as external pins; only to the internal EEPROM peripheral. SDA and SCL operation is also slightly different than GPO-GP5 as listed below. Namely, to avoid code overhead in modifying the TRIS register, both SDA and SCL are always outputs. To read data from the EEPROM peripheral requires outputting a ‘1’ on SDA placing it in high-Z state, where only the internal 100K pull-up is active on the SDA line.

SDA:
- Built-in 100K (typical) pull-up to VDD
- Open-drain (pull-down only)
- Always an output
- Outputs a ‘1’ on reset

SCL:
- Full CMOS output
- Always an output
- Outputs a ‘1’ on reset

The following example requires:

- Code Space: 77 words
- RAM Space: 5 bytes (4 are overlayable)
- Stack Levels:1 (The call to the function itself. The functions do not call any lower level functions.)
- Timing:
  - WRITE_BYTE takes 328 cycles
  - READ_CURRENT takes 212 cycles
  - READ_RANDOM takes 416 cycles.
- IO Pins: 0 (No external IO pins are used)

This code must reside in the lower half of a page. The code achieves it's small size without additional calls through the use of a sequencing table. The table is a list of procedures that must be called in order. The table uses an ADDWF PCL,F instruction, effectively a computed goto, to sequence to the next procedure. However the ADDWF PCL,F instruction yields an 8 bit address, forcing the code to reside in the first 256 addresses of a page.

### 8.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance, or one with series resonance.

Figure 8-4 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

**FIGURE 8-4: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT**

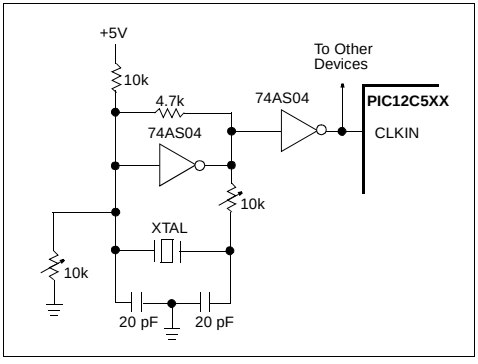
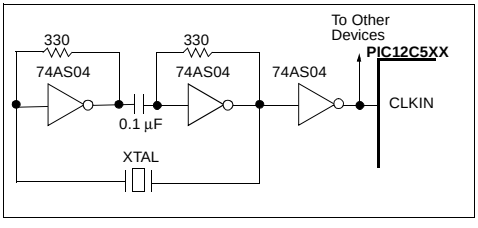



Figure 8-5 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 Ω resistors provide the negative feedback to bias the inverters in their linear region.

**FIGURE 8-5: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT**




### 8.2.4 EXTERNAL RC OSCILLATOR

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used.

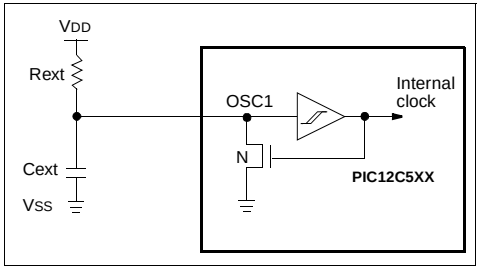
Figure 8-6 shows how the R/C combination is connected to the PIC12C5XX. For Rext values below 2.2 kΩ, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g., 1 MΩ) the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping Rext between 3 kΩ and 100 kΩ.

Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

The Electrical Specifications sections show RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

Also, see the Electrical Specifications sections for variation of oscillator frequency due to $V_{DD}$ for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and $V_{DD}$ values.

**FIGURE 8-6: EXTERNAL RC OSCILLATOR MODE**



**SWAPF** **Swap Nibbles in f**

Syntax: [ *label* ] SWAPF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f<3:0>) → (dest<7:4>);
(f<7:4>) → (dest<3:0>)

Status Affected: None

Encoding:

| 0011 | 10df | ffff |
|---|---|---|

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.

Words: 1

Cycles: 1

Example
```
SWAPF   REG1,  0
```
Before Instruction
REG1 = 0xA5

After Instruction
REG1 = 0xA5
W = 0X5A

**TRIS** **Load TRIS Register**

Syntax: [ *label* ] TRIS f

Operands: f = 6

Operation: (W) → TRIS register f

Status Affected: None

Encoding:

| 0000 | 0000 | 0fff |
|---|---|---|

Description: TRIS register 'f' (f = 6) is loaded with the contents of the W register

Words: 1

Cycles: 1

Example
```
TRIS    GPIO
```
Before Instruction
W = 0XA5

After Instruction
TRIS = 0XA5

**Note:** f = 6 for PIC12C5XX only.

**XORLW** **Exclusive OR literal with W**

Syntax: [*label*] XORLW k

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Encoding:

| 1111 | kkkk | kkkk |
|---|---|---|

Description: The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example
```
XORLW  0xAF
```
Before Instruction
W = 0xB5

After Instruction
W = 0x1A

**XORWF** **Exclusive OR W with f**

Syntax: [ *label* ] XORWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (dest)

Status Affected: Z

Encoding:

| 0001 | 10df | ffff |
|---|---|---|

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example
```
XORWF  REG,1
```
Before Instruction
REG = 0xAF
W = 0xB5

After Instruction
REG = 0x1A
W = 0xB5

# 10.0 DEVELOPMENT SUPPORT

## 10.1 Development Tools

The PICmicro® microcontrollers are supported with a full range of hardware and software development tools:

- MPLAB™-ICE Real-Time In-Circuit Emulator
- ICEPIC™ Low-Cost PIC16C5X and PIC16CXXX In-Circuit Emulator
- PRO MATE® II Universal Programmer
- PICSTART® Plus Entry-Level Prototype Programmer
- SIMICE
- PICDEM-1 Low-Cost Demonstration Board
- PICDEM-2 Low-Cost Demonstration Board
- PICDEM-3 Low-Cost Demonstration Board
- MPASM Assembler
- MPLAB™ SIM Software Simulator
- MPLAB-C17 (C Compiler)
- Fuzzy Logic Development System (*fuzzy*TECH®–MP)
- KEELOQ® Evaluation Kits and Programmer

## 10.2 MPLAB-ICE: High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB-ICE Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro® microcontrollers (MCUs). MPLAB-ICE is supplied with the MPLAB Integrated Development Environment (IDE), which allows editing, “make” and download, and source debugging from a single environment.

Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB-ICE allows expansion to support all new Microchip microcontrollers.

The MPLAB-ICE Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC compatible 386 (and higher) machine platform and Microsoft Windows® 3.x or Windows 95 environment were chosen to best make these features available to you, the end user.

MPLAB-ICE is available in two versions. MPLAB-ICE 1000 is a basic, low-cost emulator system with simple trace capabilities. It shares processor modules with the MPLAB-ICE 2000. This is a full-featured emulator system with enhanced trace, trigger, and data monitoring features. Both systems will operate across the entire operating speed range of the PICmicro® MCU.

## 10.3 ICEPIC: Low-Cost PICmicro® In-Circuit Emulator

ICEPIC is a low-cost in-circuit emulator solution for the Microchip PIC12CXXX, PIC16C5X and PIC16CXXX families of 8-bit OTP microcontrollers.

ICEPIC is designed to operate on PC-compatible machines ranging from 386 through Pentium™ based machines under Windows 3.x, Windows 95, or Windows NT environment. ICEPIC features real time, non-intrusive emulation.

## 10.4 PRO MATE II: Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode. PRO MATE II is CE compliant.

The PRO MATE II has programmable $V_{DD}$ and $V_{PP}$ supplies which allows it to verify programmed memory at $V_{DD}$ min and $V_{DD}$ max for maximum reliability. It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode the PRO MATE II can read, verify or program PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices. It can also set configuration and code-protect bits in this mode.

## 10.5 PICSTART Plus Entry Level Development System

The PICSTART programmer is an easy-to-use, low-cost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. PICSTART Plus is not recommended for production programming.

PICSTART Plus supports all PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices with up to 40 pins. Larger pin count devices such as the PIC16C923, PIC16C924 and PIC17C756 may be supported with an adapter socket. PICSTART Plus is CE compliant.

### 10.6 SIMICE Entry-Level Hardware Simulator

SIMICE is an entry-level hardware development system designed to operate in a PC-based environment with Microchip's simulator MPLAB™-SIM. Both SIMICE and MPLAB-SIM run under Microchip Technology's MPLAB Integrated Development Environment (IDE) software. Specifically, SIMICE provides hardware simulation for Microchip's PIC12C5XX, PIC12CE5XX, and PIC16C5X families of PICmicro® 8-bit microcontrollers. SIMICE works in conjunction with MPLAB-SIM to provide non-real-time I/O port emulation. SIMICE enables a developer to run simulator code for driving the target system. In addition, the target system can provide input to the simulator code. This capability allows for simple and interactive debugging without having to manually generate MPLAB-SIM stimulus files. SIMICE is a valuable debugging tool for entry-level system development.

### 10.7 PICDEM-1 Low-Cost PICmicro® Demonstration Board

The PICDEM-1 is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The users can program the sample microcontrollers provided with the PICDEM-1 board, on a PRO MATE II or PICSTART-Plus programmer, and easily test firmware. The user can also connect the PICDEM-1 board to the MPLAB-ICE emulator and download the firmware to the emulator for testing. Additional prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push-button switches and eight LEDs connected to PORTB.

### 10.8 PICDEM-2 Low-Cost PIC16CXX Demonstration Board

The PICDEM-2 is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-2 board, on a PRO MATE II programmer or PICSTART-Plus, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-2 board to test firmware. Additional prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push-button switches, a potentiometer for simulated analog input, a Serial EEPROM to demonstrate usage of the $I^2C$ bus and separate headers for connection to an LCD module and a keypad.

### 10.9 PICDEM-3 Low-Cost PIC16CXXX Demonstration Board

The PICDEM-3 is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with a LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-3 board, on a PRO MATE II programmer or PICSTART Plus with an adapter socket, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-3 board to test firmware. Additional prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include an RS-232 interface, push-button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM-3 board is an LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM-3 provides an additional RS-232 interface and Windows 3.1 software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

**NOTES:**

## 11.2 DC CHARACTERISTICS: PIC12C508/509 (Commercial, Industrial, Extended)

| DC CHARACTERISTICS | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating temperature 0°C ≤ TA ≤ +70°C (commercial)<br>–40°C ≤ TA ≤ +85°C (industrial)<br>–40°C ≤ TA ≤ +125°C (extended)<br>Operating voltage VDD range as described in DC spec Section 11.1 and Section 11.2. | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Sym** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | **Input Low Voltage** | | | | | | |
| | I/O ports | VIL | | - | | | |
| D030 | with TTL buffer | | VSS | - | 0.8V | V | 4.5 < VDD ≤ 5.5V |
| | | | | - | 0.15VDD | V | otherwise |
| D031 | with Schmitt Trigger buffer | | VSS | - | 0.15VDD | V | |
| D032 | MCLR, GP2/T0CKI (in EXTRC mode) | | VSS | - | 0.15VDD | V | |
| D033 | OSC1 (EXTRC) (1) | | VSS | - | 0.15VDD | | |
| D033 | OSC1 (in XT and LP) | | VSS | - | 0.3VDD | V | Note1 |
| | **Input High Voltage** | | | | | | |
| | I/O ports | VIH | | - | | | |
| D040 | with TTL buffer | VSS | 2.0V | - | VDD | V | 4.5 ≤ VDD ≤ 5.5V |
| D040A | | | 0.25VDD + 0.8V | - | VDD | V | otherwise |
| D041 | with Schmitt Trigger buffer | | 0.85VDD | - | VDD | V | For entire VDD range |
| D042 | MCLR/GP2/T0CKI | | 0.85VDD | - | VDD | V | |
| D042A | OSC1 (XT and LP) | | 0.7VDD | - | VDD | V | Note1 |
| D043 | OSC1 (in EXTRC mode) | | 0.85VDD | - | VDD | V | |
| D070 | GPIO weak pull-up current | IPUR | 50 | 250 | 400 | µA | VDD = 5V, VPIN = VSS |
| | **Input Leakage Current (2, 3)** | | | | | | For VDD ≤5.5V |
| D060 | I/O ports | IIL | -1 | 0.5 | ±1 | µA | Vss ≤ VPIN ≤ VDD,<br>Pin at hi-impedance |
| D061 | MCLR, GP2/T0CKI | | 20 | 130 | 250 | µA | VPIN = VSS + 0.25V(2) |
| | | | | 0.5 | +5 | µA | VPIN = VDD |
| D063 | OSC1 | | -3 | 0.5 | +3 | µA | Vss ≤ VPIN ≤ VDD,<br>XT and LP options |
| | **Output Low Voltage** | | | | | | |
| D080 | I/O ports/CLKOUT | VOL | - | - | 0.6 | V | IOL = 8.7 mA, VDD = 4.5V |
| | **Output High Voltage** | | | | | | |
| D090 | I/O ports/CLKOUT (3) | VOH | VDD - 0.7 | - | - | V | IOH = -5.4 mA, VDD = 4.5V |
| | **Capacitive Loading Specs on Output Pins** | | | | | | |
| D100 | OSC2 pin | COSC2 | - | - | 15 | pF | In XT and LP modes when external clock is used to drive OSC1. |
| D101 | All I/O pins | CIO | - | - | 50 | pF | |

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C5XX be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

### 11.3 Timing Parameter Symbology and Load Conditions - PIC12C508/C509

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

| | | | |
|---|---|---|---|
| **T** | | | |
| F | Frequency | T | Time |

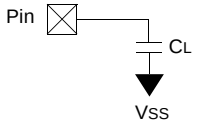
Lowercase subscripts (pp) and their meanings:

| | | | |
|---|---|---|---|
| **pp** | | | |
| 2 | to | mc | $\overline{\text{MCLR}}$ |
| ck | CLKOUT | osc | oscillator |
| cy | cycle time | os | OSC1 |
| drt | device reset timer | t0 | T0CKI |
| io | I/O port | wdt | watchdog timer |

Uppercase letters and their meanings:

| | | | |
|---|---|---|---|
| **S** | | | |
| F | Fall | P | Period |
| H | High | R | Rise |
| I | Invalid (Hi-impedance) | V | Valid |
| L | Low | Z | Hi-impedance |

**FIGURE 11-1: LOAD CONDITIONS - PIC12C508/C509**




$C_L$ = 50 pF for all pins except OSC2
15 pF for OSC2 in XT or LP modes when external clock is used to drive OSC1

## 11.4 Timing Diagrams and Specifications

**FIGURE 11-2: EXTERNAL CLOCK TIMING - PIC12C508/C509**

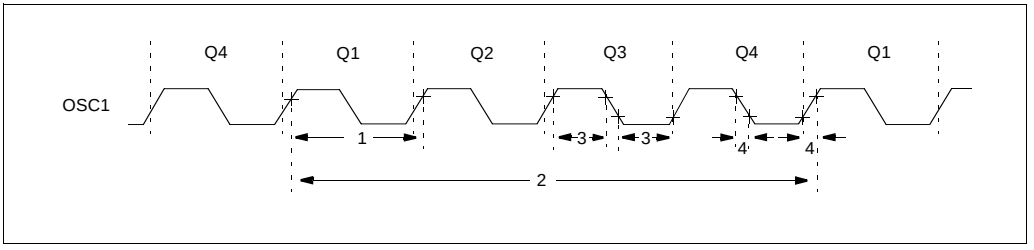



**TABLE 11-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC12C508/C509**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C (commercial),<br>–40°C ≤ TA ≤ +85°C (industrial),<br>–40°C ≤ TA ≤ +125°C (extended)<br>Operating Voltage VDD range is described in Section 11.1 | | | | | |
|---|---|---|---|---|---|---|

| Parameter No. | Sym | Characteristic | Min | Typ(1) | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | FOSC | External CLKIN Frequency(2) | | | | | |
| | | | DC | — | 4 | MHz | XT osc mode |
| | | | DC | — | 200 | kHz | LP osc mode |
| | | Oscillator Frequency(2) | | | | | |
| | | | 0.1 | — | 4 | MHz | XT osc mode |
| | | | DC | — | 200 | kHz | LP osc mode |
| 1 | TOSC | External CLKIN Period(2) | 250 | — | — | ns | EXTRC osc mode |
| | | | 250 | — | — | ns | XT osc mode |
| | | | 5 | — | — | ms | LP osc mode |
| | | Oscillator Period(2) | 250 | — | — | ns | EXTRC osc mode |
| | | | 250 | — | 10,000 | ns | XT osc mode |
| | | | 5 | — | — | ms | LP osc mode |
| 2 | Tcy | Instruction Cycle Time(3) | — | 4/FOSC | — | — | |
| 3 | TosL, TosH | Clock in (OSC1) Low or High Time | 50* | — | — | ns | XT oscillator |
| | | | 2* | — | — | ms | LP oscillator |
| 4 | TosR, TosF | Clock in (OSC1) Rise or Fall Time | — | — | 25* | ns | XT oscillator |
| | | | — | — | 50* | ns | LP oscillator |

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

**TABLE 11-5: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC12C508/C509**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C (commercial)<br>–40°C ≤ TA ≤ +85°C (industrial)<br>–40°C ≤ TA ≤ +125°C (extended)<br>Operating Voltage VDD range is described in Section 11.1 | | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter No.** | **Sym** | **Characteristic** | **Min** | **Typ(1)** | **Max** | **Units** | **Conditions** |
| 30 | TmcL | $\overline{\text{MCLR}}$ Pulse Width (low) | 2000* | — | — | ns | VDD = 5 V |
| 31 | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 9* | 18* | 30* | ms | VDD = 5 V (Commercial) |
| 32 | TDRT | Device Reset Timer Period(2) | 9* | 18* | 30* | ms | VDD = 5 V (Commercial) |
| 34 | TioZ | I/O Hi-impedance from $\overline{\text{MCLR}}$ Low | — | — | 2000* | ns | |

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 2: See Table 11-6.

**TABLE 11-6: DRT (DEVICE RESET TIMER PERIOD - PIC12C508/C509)**

| Oscillator Configuration | POR Reset | Subsequent Resets |
|---|---|---|
| IntRC & ExtRC | 18 ms (typical) | 300 µs (typical) |
| XT & LP | 18 ms (typical) | 18 ms (typical) |

**TABLE 12-1: DYNAMIC IDD (TYPICAL) - WDT ENABLED, 25°C**

| Oscillator | Frequency | VDD = 2.5V | VDD = 5.5V |
|---|---|---|---|
| External RC | 4 MHz | 250 µA* | 780 µA* |
| Internal RC | 4 MHz | 420 µA | 1.1 mA |
| XT | 4 MHz | 251 µA | 780 µA |
| LP | 32 KHz | 15 µA | 37 µA |

*Does not include current through external R&C.

**FIGURE 12-3: WDT TIMER TIME-OUT PERIOD VS. VDD**

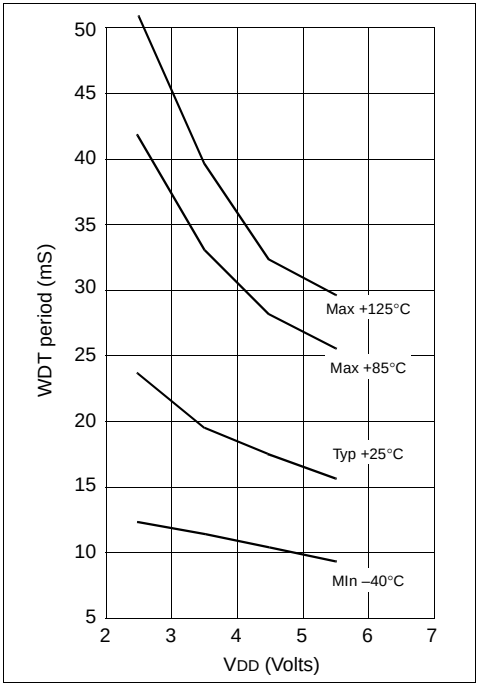



**FIGURE 12-4: SHORT DRT PERIOD VS. VDD**

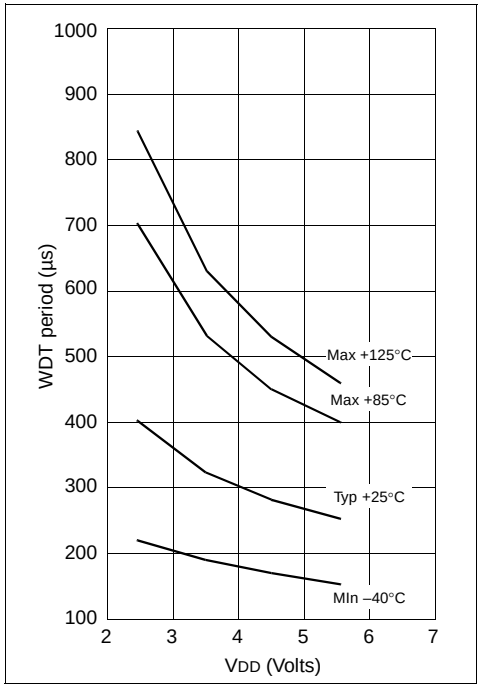


**FIGURE 14-5: WDT TIMER TIME-OUT PERIOD vs. VDD**

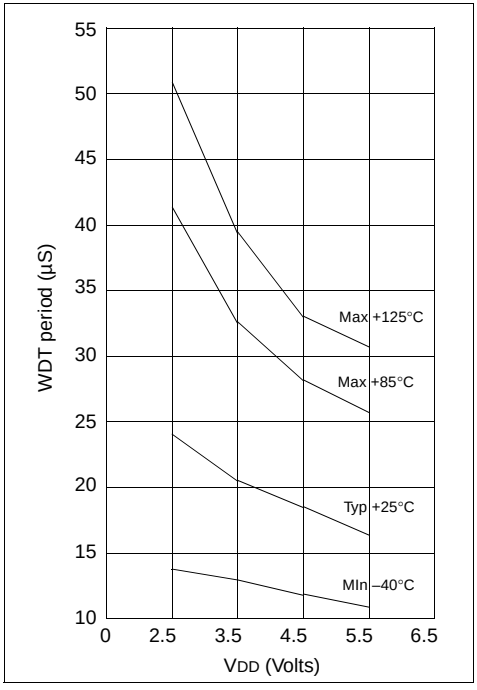



**FIGURE 14-6: SHORT DRT PERIOD VS. VDD**

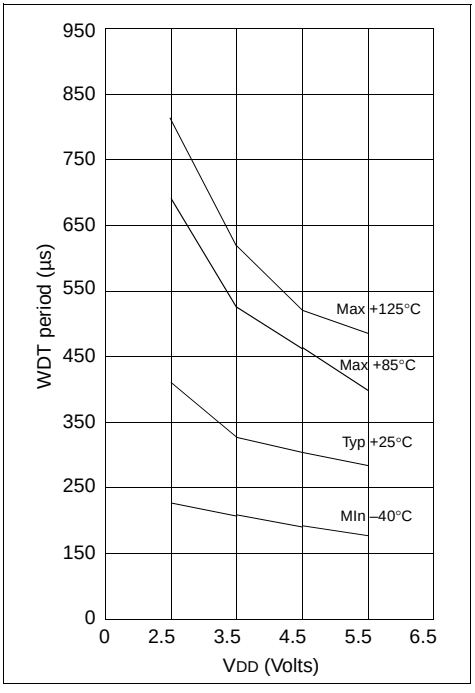



**FIGURE 14-7: IOH vs. VOH, VDD = 2.5 V**

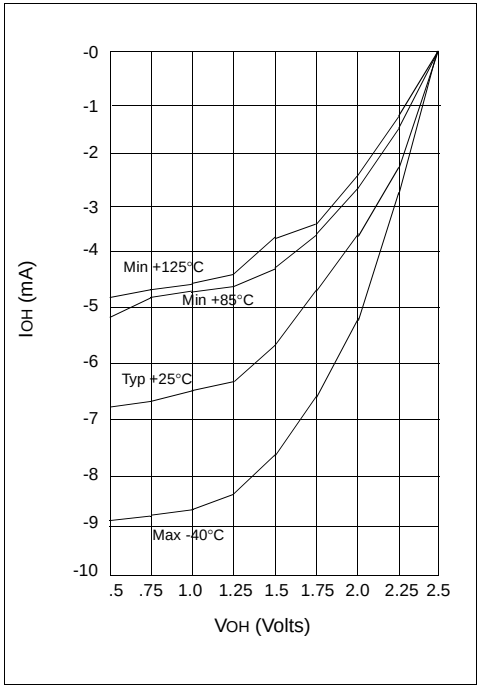
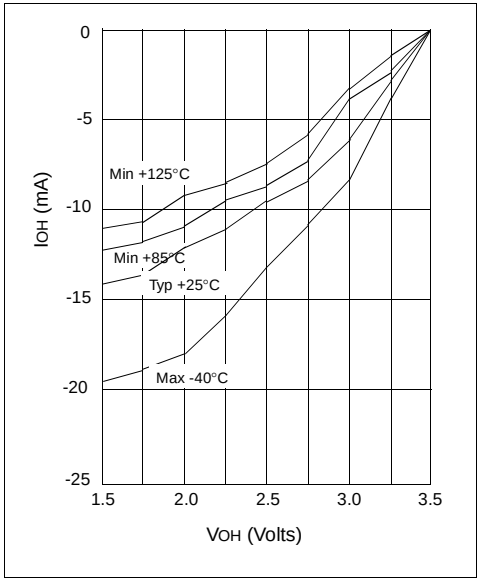


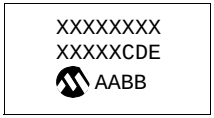

**FIGURE 14-8: IOH vs. VOH, VDD = 3.5 V**



## 15.0 PACKAGING INFORMATION

### 15.1 Package Marking Information

8-Lead PDIP (300 mil)

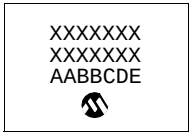



Example


8-Lead SOIC (150 mil)

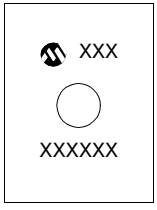

Example


8-Lead SOIC (208 mil)

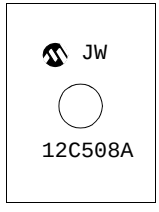



Example


8-Lead Windowed Ceramic Side Brazed (300 mil)



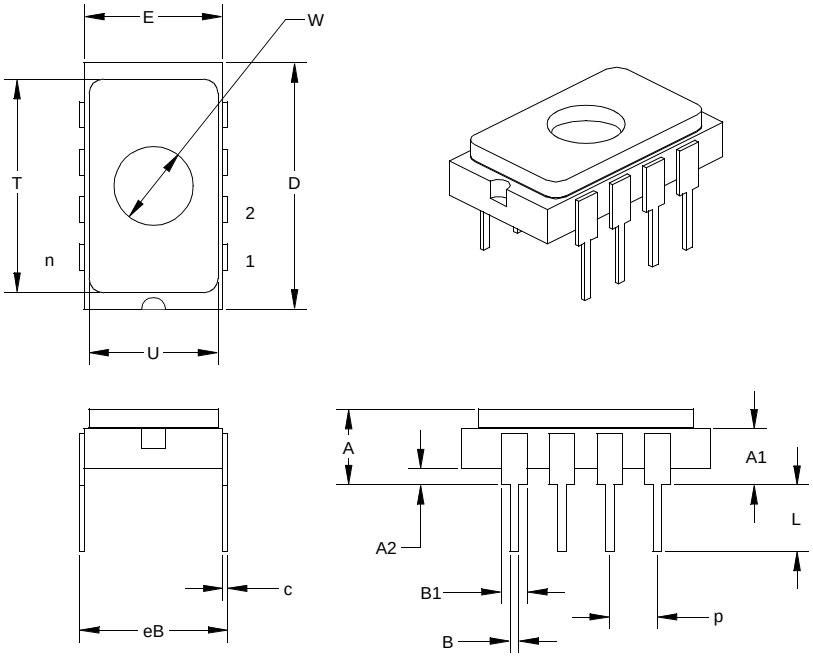

Example




| | | |
|---|---|---|
| **Legend:** | MM...M | Microchip part number information |
| | XX...X | Customer specific information* |
| | AA | Year code (last 2 digits of calendar year) |
| | BB | Week code (week of January 1 is week ‘01’) |
| | C | Facility code of the plant at which wafer is manufactured<br>O = Outside Vendor<br>C = 5” Line<br>S = 6” Line<br>H = 8” Line |
| | D | Mask revision number |
| | E | Assembly code of the plant or country of origin in which part was assembled |
| **Note**: | | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information. |

***** Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

**Package Type: K04-084 8-Lead Ceramic Side Brazed Dual In-line with Window (JW) – 300 mil**




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| PCB Row Spacing | | | 0.300 | | | 7.62 | |
| Number of Pins | n | | 8 | | | 8 | |
| Pitch | p | 0.098 | 0.100 | 0.102 | 2.49 | 2.54 | 2.59 |
| Lower Lead Width | B | 0.016 | 0.018 | 0.020 | 0.41 | 0.46 | 0.51 |
| Upper Lead Width | B1 | 0.050 | 0.055 | 0.060 | 1.27 | 1.40 | 1.52 |
| Lead Thickness | c | 0.008 | 0.010 | 0.012 | 0.20 | 0.25 | 0.30 |
| Top to Seating Plane | A | 0.145 | 0.165 | 0.185 | 3.68 | 4.19 | 4.70 |
| Top of Body to Seating Plane | A1 | 0.103 | 0.123 | 0.143 | 2.62 | 3.12 | 3.63 |
| Base to Seating Plane | A2 | 0.025 | 0.035 | 0.045 | 0.64 | 0.89 | 1.14 |
| Tip to Seating Plane | L | 0.130 | 0.140 | 0.150 | 3.30 | 3.56 | 3.81 |
| Package Length | D | 0.510 | 0.520 | 0.530 | 12.95 | 13.21 | 13.46 |
| Package Width | E | 0.280 | 0.290 | 0.300 | 7.11 | 7.37 | 7.62 |
| Overall Row Spacing | eB | 0.310 | 0.338 | 0.365 | 7.87 | 8.57 | 9.27 |
| Window Diameter | W | 0.161 | 0.166 | 0.171 | 4.09 | 4.22 | 4.34 |
| Lid Length | T | 0.440 | 0.450 | 0.460 | 11.18 | 11.43 | 11.68 |
| Lid Width | U | 0.260 | 0.270 | 0.280 | 6.60 | 6.86 | 7.11 |

* Controlling Parameter.

**Note the following details of the code protection feature on PICmicro® MCUs.**

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable”.
- Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our product.

If you have any further questions about this matter, please contact the local sales office nearest to you.



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