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Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	OTP
EEPROM Size	16 x 8
RAM Size	41 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12ce519-04-sn

PIC12C5XX

NOTES:

PIC12C5XX

3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1, and the instruction is fetched from program memory and latched into instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2 and Example 3-1.

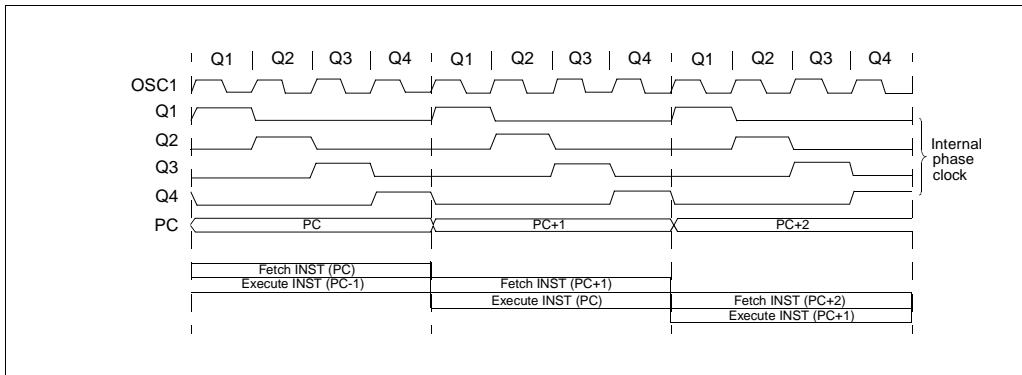
3.2 Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 3-1).

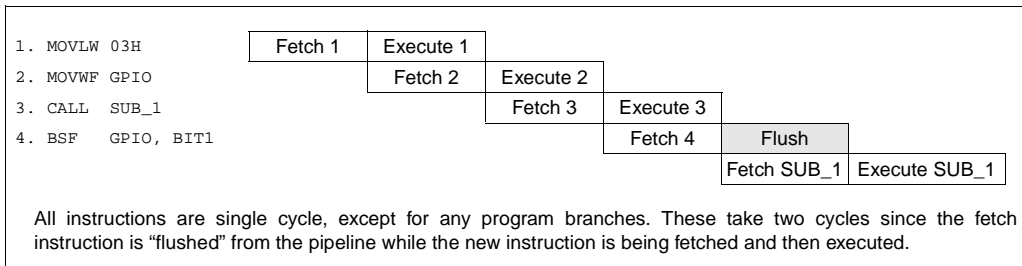
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



4.6 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

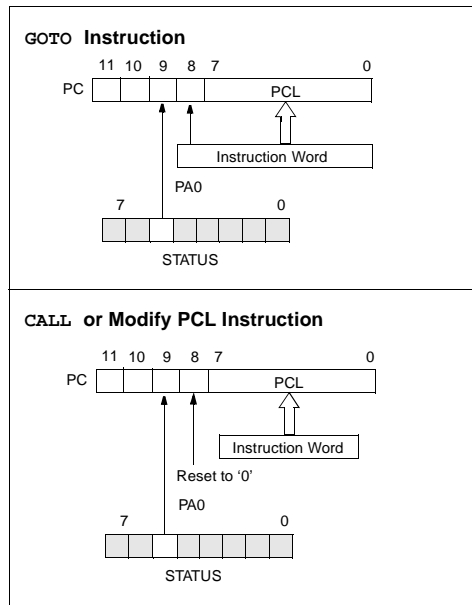
For a `GOTO` instruction, bits 8:0 of the PC are provided by the `GOTO` instruction word. The PC Latch (PCL) is mapped to `PC<7:0>`. Bit 5 of the `STATUS` register provides page information to bit 9 of the PC (Figure 4-8).

For a `CALL` instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, `PC<8>` does not come from the instruction word, but is always cleared (Figure 4-8).

Instructions where the PCL is the destination, or Modify PCL instructions, include `MOVWF PC`, `ADDWF PC`, and `BSF PC, 5`.

Note: Because `PC<8>` is cleared in the `CALL` instruction, or any Modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-8: LOADING OF PC BRANCH INSTRUCTIONS - PIC12C5XX



4.6.1 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page i.e., the oscillator calibration instruction. After executing `MOVLW XX`, the PC will roll over to location 00h, and begin executing user code.

The `STATUS` register page preselect bits are cleared upon a RESET, which means that page 0 is pre-selected.

Therefore, upon a RESET, a `GOTO` instruction will automatically cause the program to jump to page 0 until the value of the page bits is altered.

4.7 Stack

PIC12C5XX devices have a 12-bit wide L.I.F.O. hardware push/pop stack.

A `CALL` instruction will *push* the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential `CALL`'s are executed, only the most recent two return addresses are stored.

A `RETLW` instruction will *pop* the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential `RETLW`'s are executed, the stack will be filled with the address previously stored in level 2. Note that the W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

Upon any reset, the contents of the stack remain unchanged, however the program counter (PCL) will also be reset to 0.

Note 1: There are no `STATUS` bits to indicate stack overflows or stack underflow conditions.

Note 2: There are no instructions mnemonics called `PUSH` or `POP`. These are actions that occur from the execution of the `CALL` and `RETLW` instructions.

5.0 I/O PORT

As with any other register, the I/O register can be written and read under program control. However, read instructions (e.g., `MOVF GPIO, W`) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers are all set. See Section 7.0 for SCL and SDA description for PIC12CE5XX.

5.1 GPIO

GPIO is an 8-bit I/O register. Only the low order 6 bits are used (GP5:GP0). Bits 7 and 6 are unimplemented and read as '0's. Please note that GP3 is an input only pin. The configuration word can set several I/O's to alternate functions. When acting as alternate functions the pins will read as '0' during port read. Pins GP0, GP1, and GP3 can be configured with weak pull-ups and also with wake-up on change. The wake-up on change and weak pull-up functions are not pin selectable. If pin 4 is configured as MCLR, weak pull-up is always on and wake-up on change for this pin is not enabled.

5.2 TRIS Register

The output driver control register is loaded with the contents of the W register by executing the `TRIS f` instruction. A '1' from a TRIS register bit puts the corresponding output driver in a hi-impedance mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer. The exceptions are GP3 which is input only and GP2 which may be controlled by the option register, see Figure 4-5.

Note: A read of the ports reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high, but the external system is holding it low, a read of the port will indicate that the pin is low.

The TRIS registers are "write-only" and are set (output drivers disabled) upon RESET.

5.3 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 5-1. All port pins, except GP3 which is input only, may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., `MOVF GPIO, W`). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit in TRIS must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin (except GP3) can be programmed individually as input or output.

FIGURE 5-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



7.0 EEPROM PERIPHERAL OPERATION

This section applies to PIC12CE518 and PIC12CE519 only.

The PIC12CE518 and PIC12CE519 each have 16 bytes of EEPROM data memory. The EEPROM memory has an endurance of 1,000,000 erase/write cycles and a data retention of greater than 40 years. The EEPROM data memory supports a bi-directional 2-wire bus and data transmission protocol. These two-wires are serial data (SDA) and serial clock (SCL), that are mapped to bit6 and bit7, respectively, of the GPIO register (SFR 06h). Unlike the GP0-GP5 that are connected to the I/O pins, SDA and SCL are only connected to the internal EEPROM peripheral. For most applications, all that is required is calls to the following functions:

```

; Byte_Write: Byte write routine
;   Inputs: EEPROM Address   EEADDR
;           EEPROM Data     EEDATA
;   Outputs: Return 01 in W if OK, else
;           return 00 in W
;
; Read_Current: Read EEPROM at address
; currently held by EE device.
;   Inputs: NONE
;   Outputs: EEPROM Data   EEDATA
;           Return 01 in W if OK, else
;           return 00 in W
;
; Read_Random: Read EEPROM byte at supplied
; address
;   Inputs: EEPROM Address   EEADDR
;   Outputs: EEPROM Data   EEDATA
;           Return 01 in W if OK,
;           else return 00 in W

```

The code for these functions is available on our website www.microchip.com. The code will be accessed by either including the source code FL51XINC.ASM or by linking FLASH5IX.ASM.

It is very important to check the return codes when using these calls, and retry the operation if unsuccessful. Unsuccessful return codes occur when the EE data memory is busy with the previous write, which can take up to 4 mS.

7.0.1 SERIAL DATA

SDA is a bi-directional pin used to transfer addresses and data into and data out of the device.

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

The EEPROM interface is a 2-wire bus protocol consisting of data (SDA) and a clock (SCL). Although these lines are mapped into the GPIO register, they are not accessible as external pins; only to the internal EEPROM peripheral. SDA and SCL operation is also slightly different than GPO-GP5 as listed below.

Namely, to avoid code overhead in modifying the TRIS register, both SDA and SCL are always outputs. To read data from the EEPROM peripheral requires outputting a '1' on SDA placing it in high-Z state, where only the internal 100K pull-up is active on the SDA line.

SDA:

- Built-in 100K (typical) pull-up to VDD
- Open-drain (pull-down only)
- Always an output
- Outputs a '1' on reset

SCL:

- Full CMOS output
- Always an output
- Outputs a '1' on reset

The following example requires:

- Code Space: 77 words
- RAM Space: 5 bytes (4 are overlayable)
- Stack Levels:1 (The call to the function itself. The functions do not call any lower level functions.)
- Timing:
 - WRITE_BYTE takes 328 cycles
 - READ_CURRENT takes 212 cycles
 - READ_RANDOM takes 416 cycles.
- IO Pins: 0 (No external IO pins are used)

This code must reside in the lower half of a page. The code achieves it's small size without additional calls through the use of a sequencing table. The table is a list of procedures that must be called in order. The table uses an ADDWF PCL,F instruction, effectively a computed goto, to sequence to the next procedure. However the ADDWF PCL,F instruction yields an 8 bit address, forcing the code to reside in the first 256 addresses of a page.

PIC12C5XX

BSF Bit Set f

Syntax: [*label*] BSF f,b

Operands: $0 \leq f \leq 31$
 $0 \leq b \leq 7$

Operation: $1 \rightarrow (f < b >)$

Status Affected: None

Encoding:

0101	bbbf	ffff
------	------	------

Description: Bit 'b' in register 'f' is set.

Words: 1

Cycles: 1

Example: BSF FLAG_REG, 7

Before Instruction
 FLAG_REG = 0x0A

After Instruction
 FLAG_REG = 0x8A

BTFSC Bit Test f, Skip if Clear

Syntax: [*label*] BTFSC f,b

Operands: $0 \leq f \leq 31$
 $0 \leq b \leq 7$

Operation: skip if (f < b >) = 0

Status Affected: None

Encoding:

0110	bbbf	ffff
------	------	------

Description: If bit 'b' in register 'f' is 0 then the next instruction is skipped.
 If bit 'b' is 0 then the next instruction fetched during the current instruction execution is discarded, and an NOP is executed instead, making this a 2 cycle instruction.

Words: 1

Cycles: 1(2)

Example:

HERE	BTFSC	FLAG, 1
FALSE	GOTO	PROCESS_CODE
TRUE	•	
	•	
	•	

Before Instruction
 PC = address (HERE)

After Instruction
 if FLAG<1> = 0,
 PC = address (TRUE);
 if FLAG<1> = 1,
 PC = address (FALSE)

BTFSS Bit Test f, Skip if Set

Syntax: [*label*] BTFSS f,b

Operands: $0 \leq f \leq 31$
 $0 \leq b < 7$

Operation: skip if (f < b >) = 1

Status Affected: None

Encoding:

0111	bbbf	ffff
------	------	------

Description: If bit 'b' in register 'f' is '1' then the next instruction is skipped.
 If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and an NOP is executed instead, making this a 2 cycle instruction.

Words: 1

Cycles: 1(2)

Example:

HERE	BTFSS	FLAG, 1
FALSE	GOTO	PROCESS_CODE
TRUE	•	
	•	
	•	

Before Instruction
 PC = address (HERE)

After Instruction
 If FLAG<1> = 0,
 PC = address (FALSE);
 if FLAG<1> = 1,
 PC = address (TRUE)

INCF **Increment f**

Syntax: [*label*] INCF *f,d*

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f) + 1 \rightarrow (\text{dest})$

Status Affected: Z

Encoding:

0010	10df	ffff
------	------	------

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example: INCF CNT, 1

Before Instruction
 CNT = 0xFF
 Z = 0

After Instruction
 CNT = 0x00
 Z = 1

INCFSZ **Increment f, Skip if 0**

Syntax: [*label*] INCFSZ *f,d*

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f) + 1 \rightarrow (\text{dest})$, skip if result = 0

Status Affected: None

Encoding:

0011	11df	ffff
------	------	------

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
 If the result is 0, then the next instruction, which is already fetched, is discarded and an NOP is executed instead making it a two cycle instruction.

Words: 1

Cycles: 1(2)

Example: HERE INCFSZ CNT, 1
 GOTO LOOP
 CONTINUE
 .
 .
 .

Before Instruction
 PC = address (HERE)

After Instruction
 CNT = CNT + 1;
 if CNT = 0,
 PC = address (CONTINUE);
 if CNT \neq 0,
 PC = address (HERE + 1)

IORLW **Inclusive OR literal with W**

Syntax: [*label*] IORLW *k*

Operands: $0 \leq k \leq 255$

Operation: $(W) .OR. (k) \rightarrow (W)$

Status Affected: Z

Encoding:

1101	kkkk	kkkk
------	------	------

Description: The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example: IORLW 0x35

Before Instruction
 W = 0x9A

After Instruction
 W = 0xBF
 Z = 0

IORWF **Inclusive OR W with f**

Syntax: [*label*] IORWF *f,d*

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(W) .OR. (f) \rightarrow (\text{dest})$

Status Affected: Z

Encoding:

0001	00df	ffff
------	------	------

Description: Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example: IORWF RESULT, 0

Before Instruction
 RESULT = 0x13
 W = 0x91

After Instruction
 RESULT = 0x13
 W = 0x93
 Z = 0

10.16 KEELOQ® Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.

TABLE 10-1: DEVELOPMENT TOOLS FROM MICROCHIP

	PIC12C5XX	PIC14000	PIC16C5X	PIC16CXXX	PIC16C6X	PIC16C7XX	PIC16C8X	PIC16C9XX	PIC17C4X	PIC17C7XX	24CXX 25CXX 93CXX	HCS200 HCS300 HCS301
Emulator Products	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
MPLAB™-ICE												
Emulator Products												
ICEPIC™ Low-Cost In-Circuit Emulator												
Software Tools	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
MPLAB™ Integrated Development Environment												
MPLAB™ C17* Compiler												
fuzzyTECH®-MP Explorer/Edition Fuzzy Logic Dev. Tool	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Software Tools												
Total Endurance™ Software Model											✓	
Programmers	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PICSTART® Plus Low-Cost Universal Dev. Kit												
PRO MATE® II Universal Programmer	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
KEELOQ® Programmer												✓
SEEVAL® Designers Kit											✓	
Demo Boards	✓		✓	✓	✓	✓	✓	✓	✓	✓		
SIMICE												
PICDEM-14A		✓										
PICDEM-1			✓	✓			✓					
PICDEM-2					✓							
PICDEM-3								✓				
KEELOQ® Evaluation Kit												✓
KEELOQ Transponder Kit												✓

11.3 Timing Parameter Symbology and Load Conditions - PIC12C508/C509

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T	
F Frequency	T Time

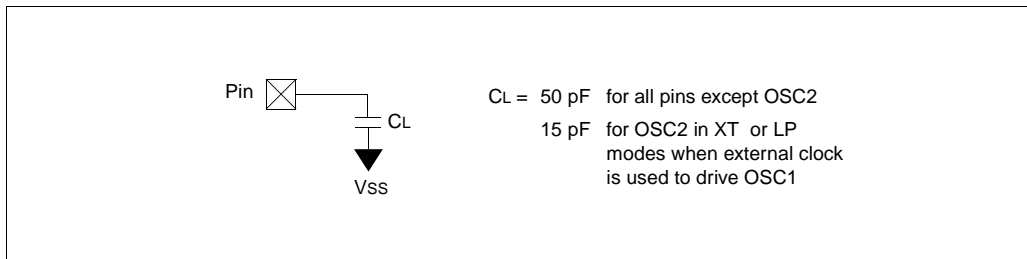
Lowercase subscripts (pp) and their meanings:

pp	
2 to	mc $\overline{\text{MCLR}}$
ck CLKOUT	osc oscillator
cy cycle time	os OSC1
drt device reset timer	t0 T0CKI
io I/O port	wdt watchdog timer

Uppercase letters and their meanings:

S	
F Fall	P Period
H High	R Rise
I Invalid (Hi-impedance)	V Valid
L Low	Z Hi-impedance

FIGURE 11-1: LOAD CONDITIONS - PIC12C508/C509



13.0 ELECTRICAL CHARACTERISTICS - PIC12C508A/PIC12C509A/ PIC12LC508A/PIC12LC509A/PIC12CR509A/PIC12CE518/PIC12CE519/ PIC12LCE518/PIC12LCE519/PIC12LCR509A

Absolute Maximum Ratings†

Ambient Temperature under bias	-40°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on V _{DD} with respect to V _{SS}	0 to +7.0 V
Voltage on $\overline{\text{MCLR}}$ with respect to V _{SS}	0 to +14 V
Voltage on all other pins with respect to V _{SS}	-0.3 V to (V _{DD} + 0.3 V)
Total Power Dissipation ⁽¹⁾	700 mW
Max. Current out of V _{SS} pin	200 mA
Max. Current into V _{DD} pin	150 mA
Input Clamp Current, I _{IK} (V _I < 0 or V _I > V _{DD}).....	±20 mA
Output Clamp Current, I _{OK} (V _O < 0 or V _O > V _{DD}).....	±20 mA
Max. Output Current sunk by any I/O pin.....	25 mA
Max. Output Current sourced by any I/O pin.....	25 mA
Max. Output Current sourced by I/O port (GPIO)	100 mA
Max. Output Current sunk by I/O port (GPIO)	100 mA

Note 1: Power Dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

13.2 DC CHARACTERISTICS: **PIC12LC508A/509A (Commercial, Industrial)**
PIC12LCE518/519 (Commercial, Industrial)
PIC12LCR509A (Commercial, Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)					
Parm No.	Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
D001	Supply Voltage	VDD	2.5		5.5	V	FOSC = DC to 4 MHz (Commercial/Industrial)
D002	RAM Data Retention Voltage⁽²⁾	VDR		1.5*		V	Device in SLEEP mode
D003	VDD Start Voltage to ensure Power-on Reset	VPOR		VSS		V	See section on Power-on Reset for details
D004	VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See section on Power-on Reset for details
D010	Supply Current⁽³⁾	IDD	—	0.4	0.8	mA	XT and EXTRC options (Note 4) FOSC = 4 MHz, VDD = 2.5V INTRC Option FOSC = 4 MHz, VDD = 2.5V LP OPTION, Commercial Temperature FOSC = 32 kHz, VDD = 2.5V, WDT disabled LP OPTION, Industrial Temperature FOSC = 32 kHz, VDD = 2.5V, WDT disabled
D010C			—	0.4	0.8	mA	
D010A			—	15	23	μA	
			—	15	31	μA	
D020	Power-Down Current⁽⁵⁾	IPD	—	0.2	3	μA	VDD = 2.5V, Commercial VDD = 2.5V, Industrial
D021			—	0.2	4	μA	
D021B							
		ΔI _{WDT}	—	2.0	4	mA	VDD = 2.5V, Commercial VDD = 2.5V, Industrial
				2.0	5	mA	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:
 OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kOhm.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

13.5 Timing Parameter Symbology and Load Conditions - PIC12C508A, PIC12C509A, PIC12CR509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

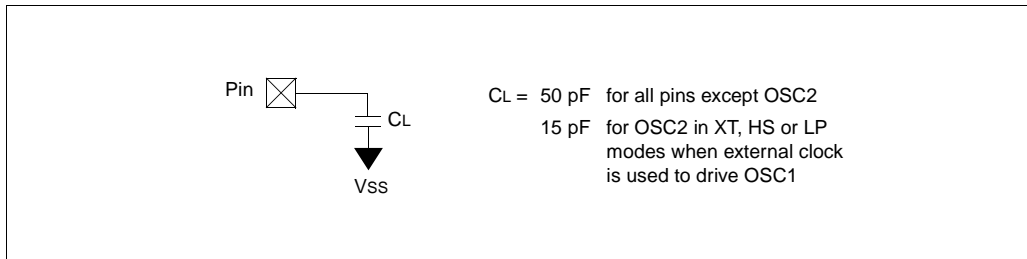
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	TOCKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 13-1: LOAD CONDITIONS - PIC12C508A/C509A, PIC12CE518/519, PIC12LC508A/509A, PIC12LCE518/519, PIC12LCR509A



PIC12C5XX

TABLE 13-6: DRT (DEVICE RESET TIMER PERIOD) - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519

Oscillator Configuration	POR Reset	Subsequent Resets
IntRC & ExtRC	18 ms (typical) ⁽¹⁾	300 μ s (typical) ⁽¹⁾
XT & LP	18 ms (typical) ⁽¹⁾	18 ms (typical) ⁽¹⁾

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 13-5: TIMER0 CLOCK TIMINGS - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519

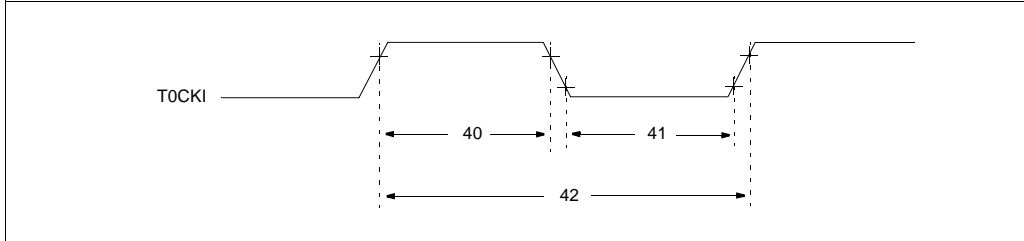


TABLE 13-7: TIMER0 CLOCK REQUIREMENTS - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519

AC Characteristics		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended)					
		Operating Voltage V _{DD} range is described in Section 13.1.					
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
40	Ti0H	TOCKI High Pulse Width - No Prescaler	0.5 T _{CY} + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Ti0L	TOCKI Low Pulse Width - No Prescaler	0.5 T _{CY} + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Ti0P	TOCKI Period	20 or $\frac{T_{CY} + 40}{N}$	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4, ..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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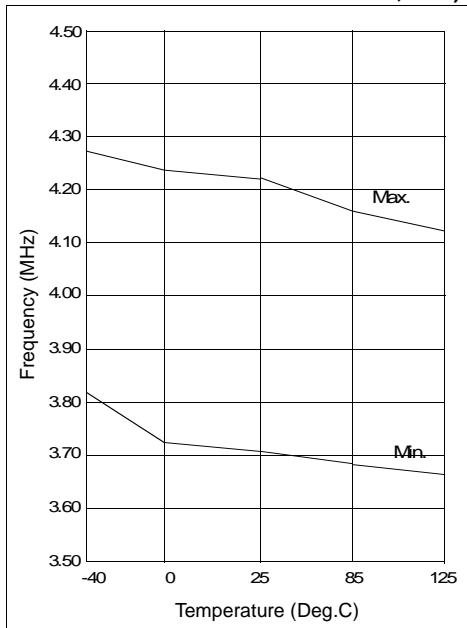
NOTES:

14.0 DC AND AC CHARACTERISTICS - PIC12C508A/PIC12C509A/ PIC12LC508A/PIC12LC509A, PIC12CE518/PIC12CE519/PIC12CR509A/ PIC12LCE518/PIC12LCE519/ PIC12LCR509A

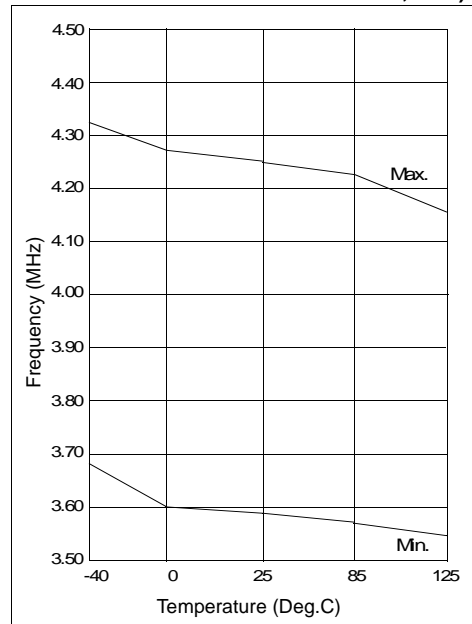
The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified V_{DD} range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean - 3σ) respectively, where σ is standard deviation.

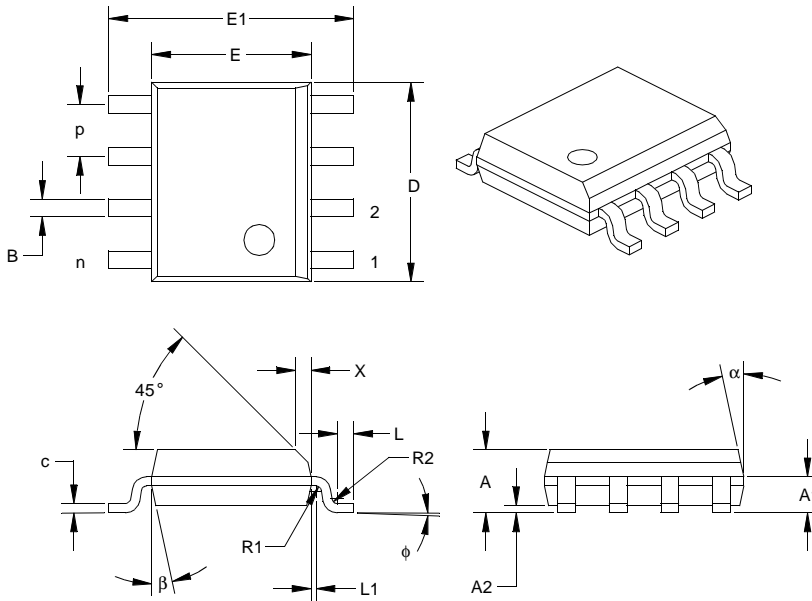
**FIGURE 14-1: CALIBRATED INTERNAL RC
FREQUENCY RANGE VS.
TEMPERATURE (V_{DD} = 5.0V)
(INTERNAL RC IS
CALIBRATED TO 25°C, 5.0V)**



**FIGURE 14-2: CALIBRATED INTERNAL RC
FREQUENCY RANGE VS.
TEMPERATURE (V_{DD} = 2.5V)
(INTERNAL RC IS
CALIBRATED TO 25°C, 5.0V)**



Package Type: K04-057 8-Lead Plastic Small Outline (SN) – Narrow, 150 mil



Units		INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Dimension Limits							
Pitch	p		0.050			1.27	
Number of Pins	n		8			8	
Overall Pack. Height	A	0.054	0.061	0.069	1.37	1.56	1.75
Shoulder Height	A1	0.027	0.035	0.044	0.69	0.90	1.11
Standoff	A2	0.004	0.007	0.010	0.10	0.18	0.25
Molded Package Length	D [‡]	0.189	0.193	0.196	4.80	4.89	4.98
Molded Package Width	E [‡]	0.150	0.154	0.157	3.81	3.90	3.99
Outside Dimension	E1	0.229	0.237	0.244	5.82	6.01	6.20
Chamfer Distance	X	0.010	0.015	0.020	0.25	0.38	0.51
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	φ	0	4	8	0	4	8
Radius Centerline	L1	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.009	0.010	0.19	0.22	0.25
Lower Lead Width	B [†]	0.014	0.017	0.020	0.36	0.43	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter.

† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

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