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# Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

## Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	OTP
EEPROM Size	16 x 8
RAM Size	41 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12ce519-04e-p

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

		PIC12C508(A)	PIC12C509(A)	PIC12CR509A	PIC12CE518	PIC12CE519	PIC12C671	PIC12C672	PIC12CE673	PIC12CE674
Clock	Maximum Frequency of Operation (MHz)	4	4	4	4	4	10	10	10	10
Momony	EPROM Program Memory	512 x 12	1024 x 12	1024 x 12 (ROM)	512 x 12	1024 x 12	1024 x 14	2048 x 14	1024 x 14	2048 x 14
Memory	RAM Data Memory (bytes)	25	41	41	25	41	128	128	128	128
	EEPROM Data Memory (bytes)	_	_	_	16	16	_	—	16	16
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0
	A/D Con- verter (8-bit) Channels	_	_	_	_	_	4	4	4	4
	Wake-up from SLEEP on pin change	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Interrupt Sources	—	—	-			4	4	4	4
Features	I/O Pins	5	5	5	5	5	5	5	5	5
	Input Pins	1	1	1	1	1	1	1	1	1
	Internal Pull-ups	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	In-Circuit Serial Programming	Yes	Yes	_	Yes	Yes	Yes	Yes	Yes	Yes
	Number of Instructions	33	33	33	33	33	35	35	35	35
	Packages	8-pin DIP, JW, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, JW	8-pin DIP, JW

# TABLE 1-1: PIC12CXXX & PIC12CEXXX FAMILY OF DEVICES

All PIC12CXXX & PIC12CEXXX devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

All PIC12CXXX & PIC12CEXXX devices use serial programming with data pin GP0 and clock pin GP1.





Name	DIP Pin #	SOIC Pin #	I/O/P Type	Buffer Type	Description
GP0	7	7	I/O	TTL/ST	Bi-directional I/O port/ serial programming data. Can be software programmed for internal weak pull-up and wake-up from SLEEP on pin change. This buffer is a Schmitt Trigger input when used in serial programming mode.
GP1	6	6	I/O	TTL/ST	Bi-directional I/O port/ serial programming clock. Can be software programmed for internal weak pull-up and wake-up from SLEEP on pin change. This buffer is a Schmitt Trigger input when used in serial programming mode.
GP2/T0CKI	5	5	I/O	ST	Bi-directional I/O port. Can be configured as T0CKI.
GP3/MCLR/Vpp	4	4	1	TTL/ST	Input port/master clear (reset) input/programming volt- age input. When configured as MCLR, this pin is an active low reset to the device. Voltage on MCLR/VPP must not exceed VDD during normal device operation or the device will enter programming mode. Can be software programmed for internal weak pull-up and wake-up from SLEEP on pin change. Weak pull-up always on if configured as MCLR. ST when in MCLR mode.
GP4/OSC2	3	3	I/O	TTL	Bi-directional I/O port/oscillator crystal output. Con- nections to crystal or resonator in crystal oscillator mode (XT and LP modes only, GPIO in other modes).
GP5/OSC1/CLKIN	2	2	I/O	TTL/ST	Bidirectional IO port/oscillator crystal input/external clock source input (GPIO in Internal RC mode only, OSC1 in all other oscillator modes). TTL input when GPIO, ST input in external RC oscillator mode.
VDD	1	1	Р	_	Positive supply for logic and I/O pins
Vss	8	8	Р	_	Ground reference for logic and I/O pins

TABLE 3-1:	PIC12C5XX	PINOUT	DESCRIPTION

Legend: I = input, O = output, I/O = input/output, P = power, — = not used, TTL = TTL input, ST = Schmitt Trigger input

# 4.0 MEMORY ORGANIZATION

PIC12C5XX memory is organized into program memory and data memory. For devices with more than 512 bytes of program memory, a paging scheme is used. Program memory pages are accessed using one STA-TUS register bit. For the PIC12C509, PIC12C509A, PICCR509A and PIC12CE519 with a data memory register file of more than 32 registers, a banking scheme is used. Data memory banks are accessed using the File Select Register (FSR).

#### 4.1 Program Memory Organization

The PIC12C5XX devices have a 12-bit Program Counter (PC) capable of addressing a 2K x 12 program memory space.

Only the first 512 x 12 (0000h-01FFh) for the PIC12C508. PIC12C508A and PIC12CE518 and 1K x 12 (0000h-03FFh) for the PIC12C509, PIC12C509A. PIC12CR509A, and PIC12CE519 are physically implemented. Refer to Figure 4-1. Accessing a location above these boundaries will cause a wraparound within the first 512 x 12 space (PIC12C508, PIC12C508A and PIC12CE518) or 1K x 12 space (PIC12C509, PIC12C509A, PIC12CR509A and PIC12CE519). The effective reset vector is at 000h, (see Figure 4-1). Location 01FFh (PIC12C508, PIC12C508A and PIC12CE518) or location 03FFh (PIC12C509, PIC12C509A, PIC12CR509A and PIC12CE519) contains the internal clock oscillator calibration value. This value should never be overwritten.

#### FIGURE 4-1: PROGRAM MEMORY MAP AND STACK



#### 4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1).

The special registers can be classified into two sets. The special function registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

### TABLE 4-1: SPECIAL FUNCTION REGISTER (SFR) SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets <sup>(2)</sup>
N/A	TRIS	-	-							11 1111	11 1111
N/A	OPTION	Contains c prescaler,	ontrol bits wake-up or	to configur n change,	e Timer0, and weak j	Timer0/WD1 pull-ups	Г			1111 1111	1111 1111
00h	INDF	Uses conte	ents of FSF	R to addres	ss data me	mory (not a	physical rec	gister)		xxxx xxxx	uuuu uuuu
01h	TMR0	8-bit real-ti	me clock/c	ounter						xxxx xxxx	uuuu uuuu
02h <sup>(1)</sup>	PCL	Low order	8 bits of PO	0						1111 1111	1111 1111
03h	STATUS	GPWUF	—	PA0	TO	PD	Z	DC	С	0001 1xxx	q00q quuu <b>(3)</b>
04h	FSR (PIC12C508/ PIC12C508A/ PIC12C518)	Indirect da	ta memory	address p	pointer					111x xxxx	111u uuuu
04h	FSR (PIC12C509/ PIC12C509A/ PIC12CR509A/ PIC12CE519)	Indirect da	ta memory	address p	oointer					110x xxxx	lluu uuuu
05h	OSCCAL (PIC12C508/ PIC12C509)	CAL3	CAL2	CAL1	CAL0	_	_	_	_	0111	uuuu
05h	OSCCAL (PIC12C508A/ PIC12C509A/ PIC12CE518/ PIC12CE519/ PIC12CR509A)	CAL5	CAL4	CAL3	CAL2	CAL1	CALO	_	_	1000 00	uuuu uu
06h	GPIO (PIC12C508/ PIC12C509/ PIC12C508A/ PIC12C509A/ PIC12CR509A)	_	_	GP5	GP4	GP3	GP2	GP1	GP0	xx xxxx	uu uuuu
06h	GPIO (PIC12CE518/ PIC12CE519)	SCL	SDA	GP5	GP4	GP3	GP2	GP1	GP0	11xx xxxx	11uu uuuu

Legend: Shaded boxes = unimplemented or unused, - = unimplemented, read as '0' (if applicable)

x = unknown, u = unchanged, q = see the tables in Section 8.7 for possible values.

Note 1: The upper byte of the Program Counter is not directly accessible. See Section 4.6 for an explanation of how to access these bits.

2: Other (non power-up) resets include external reset through MCLR, watchdog timer and wake-up on pin change reset.

3: If reset was due to wake-up on pin change then bit 7 = 1. All other resets will cause bit 7 = 0.

TABLE 5-1:	SUMMARY OF PORT REGISTERS
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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	TRIS	—	Ι							11 1111	11 1111
N/A	OPTION	GPWU	GPPU	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
03H	STATUS	GPWUF		PAO	TO	PD	Z	DC	С	0001 1xxx	q00q quuu <sup>(1)</sup>
06h	GPIO (PIC12C508/ PIC12C509/ PIC12C508A/ PIC12C509A/ PIC12CR509A)	_		GP5	GP4	GP3	GP2	GP1	GP0	xx xxxx	uu uuuu
06h	GPIO (PIC12CE518/ PIC12CE519)	SCL	SDA	GP5	GP4	GP3	GP2	GP1	GP0	11xx xxxx	11uu uuuu

Legend: Shaded cells not used by Port Registers, read as '0', — = unimplemented, read as '0', x = unknown, u = unchanged, g = see tables in Section 8.7 for possible values.

Note 1: If reset was due to wake-up on change, then bit 7 = 1. All other resets will cause bit 7 = 0.

#### 5.4 I/O Programming Considerations

#### 5.4.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of GPIO will cause all eight bits of GPIO to be read into the CPU, bit5 to be set and the GPIO value to be written to the output latches. If another bit of GPIO is used as a bidirectional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g.,  ${\tt BCF}$  ,  ${\tt BSF}$ , etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wiredand"). The resulting high output currents may damage the chip.

#### EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

; 1 ; ;	Initial GPIO<5 GPIO<2	L GPIO S 5:3> Inp 2:0> Out	Settings puts puts		
;					
;			GPI	) latch	GPIO pins
;					
	BCF	GPIO, 5	5 ;01	-ppp	11 pppp
	BCF	GPIO, 4	i ;10	-ppp	11 pppp
	MOVLW	007h	;		
	TRIS	GPIO	;10	-ppp	11 pppp

;Note that the user may have expected the pin ;values to be --00 pppp. The 2nd BCF caused ;GP5 to be latched as the pin value (High).

# 5.4.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

#### 6.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

#### 6.1.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-4). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device. When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for TOCKI to have a period of at least 4ToSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on TOCKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

#### 6.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 6-4 shows the delay from the external clock edge to the timer incrementing.

#### 6.1.3 OPTION REGISTER EFFECT ON GP2 TRIS

If the option register is set to read TIMER0 from the pin, the port is forced to an input regardless of the TRIS register setting.



#### FIGURE 6-4: TIMER0 TIMING WITH EXTERNAL CLOCK

## 7.0 EEPROM PERIPHERAL OPERATION

# This section applies to PIC12CE518 and PIC12CE519 only.

The PIC12CE518 and PIC12CE519 each have 16 bytes of EEPROM data memory. The EEPROM memory has an endurance of 1,000,000 erase/write cycles and a data retention of greater than 40 years. The EEPROM data memory supports a bi-directional 2-wire bus and data transmission protocol. These two-wires are serial data (SDA) and serial clock (SCL), that are mapped to bit6 and bit7, respectively, of the GPIO register (SFR 06h). Unlike the GP0-GP5 that are connected to the internal EEPROM peripheral. For most applications, all that is required is calls to the following functions:

; Byte\_Write: Byte write routine Inputs: EEPROM Address EEADDR : ; EEPROM Data EEDATA Outputs: Return 01 in W if OK, else ; return 00 in W ; ; Read\_Current: Read EEPROM at address currently held by EE device. Inputs: NONE ; Outputs: EEPROM Data EEDATA ; Return 01 in W if OK, else ; return 00 in W ; ; Read\_Random: Read EEPROM byte at supplied address Inputs: EEPROM Address : FFADDR ; Outputs: EEPROM Data EEDATA Return 01 in W if OK, ; else return 00 in W

The code for these functions is available on our website www.microchip.com. The code will be accessed by either including the source code FL51XINC.ASM or by linking FLASH5IX.ASM.

It is very important to check the return codes when using these calls, and retry the operation if unsuccessful. Unsuccessful return codes occur when the EE data memory is busy with the previous write, which can take up to 4 mS.

#### 7.0.1 SERIAL DATA

SDA is a bi-directional pin used to transfer addresses and data into and data out of the device.

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

The EEPROM interface is a 2-wire bus protocol consisting of data (SDA) and a clock (SCL). Although these lines are mapped into the GPIO register, they are not accessible as external pins; only to the internal EEPROM peripheral. SDA and SCL operation is also slightly different than GPO-GP5 as listed below. Namely, to avoid code overhead in modifying the TRIS register, both SDA and SCL are always outputs. To read data from the EEPROM peripheral requires outputting a '1' on SDA placing it in high-Z state, where only the internal 100K pull-up is active on the SDA line.

SDA:

Built-in 100K (typical) pull-up to VDD Open-drain (pull-down only) Always an output Outputs a '1' on reset

SCL: Full CMOS output Always an output Outputs a '1' on reset

The following example requires:

- · Code Space: 77 words
- RAM Space: 5 bytes (4 are overlayable)
- Stack Levels:1 (The call to the function itself. The functions do not call any lower level functions.)
- Timing:
  - WRITE\_BYTE takes 328 cycles
  - READ\_CURRENT takes 212 cycles
  - READ\_RANDOM takes 416 cycles.
- IO Pins: 0 (No external IO pins are used)

This code must reside in the lower half of a page. The code achieves it's small size without additional calls through the use of a sequencing table. The table is a list of procedures that must be called in order. The table uses an ADDWF PCL,F instruction, effectively a computed goto, to sequence to the next procedure. However the ADDWF PCL,F instruction yields an 8 bit address, forcing the code to reside in the first 256 addresses of a page.

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Figure 7-2: Block diagram of GPIO7 (SCL line)



## FIGURE 7-3: DATA TRANSFER SEQUENCE ON THE SERIAL BUS





### 7.2 Device Addressing

After generating a START condition, the bus master transmits a control byte consisting of a slave address and a Read/Write bit that indicates what type of operation is to be performed. The slave address consists of a 4-bit device code (1010) followed by three don't care bits.

The last bit of the control byte determines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. (Figure 7-5). The bus is monitored for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

#### FIGURE 7-5: CONTROL BYTE FORMAT



#### 8.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance, or one with series resonance.

Figure 8-4 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 k $\Omega$  resistor provides the negative feedback for stability. The 10 k $\Omega$  potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

#### FIGURE 8-4: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT



Figure 8-5 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330  $\Omega$  resistors provide the negative feedback to bias the inverters in their linear region.

#### FIGURE 8-5: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



#### 8.2.4 EXTERNAL RC OSCILLATOR

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used.

Figure 8-6 shows how the R/C combination is connected to the PIC12C5XX. For Rext values below 2.2 k $\Omega$ , the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g., 1 M $\Omega$ ) the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping Rext between 3 k $\Omega$  and 100 k $\Omega$ .

Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

The Electrical Specifications sections show RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

Also, see the Electrical Specifications sections for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

# FIGURE 8-6: EXTERNAL RC OSCILLATOR MODE



#### FIGURE 8-8: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



FIGURE 8-9: TIME-OUT SEQUENCE ON POWER-UP (MCLR PULLED LOW)







#### 8.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, a time-out period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see DC specs).

Under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

#### 8.6.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The SLEEP instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT wake-up reset.



#### FIGURE 8-12: WATCHDOG TIMER BLOCK DIAGRAM

TABLE 8-6: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	OPTION	GPWU	GPPU	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: Shaded boxes = Not used by Watchdog Timer, - = unimplemented, read as '0', u = unchanged

# PIC12C5XX

SWAPF	Swap Nibbles in f						
Syntax:	[label] SWAPF f,d						
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in \left[0,1\right] \end{array}$						
Operation:	$(f{<}3:0{>}) \rightarrow (dest{<}7:4{>}); \\ (f{<}7:4{>}) \rightarrow (dest{<}3:0{>})$						
Status Affected:	None						
Encoding:	0011 10df fff	f					
Description:	The upper and lower nibbl 'f' are exchanged. If 'd' is placed in W register. If 'd' is placed in register 'f'.	les of register 0 the result is is 1 the result					
Words:	1						
Cycles:	1						
Example	SWAPF REG1, 0						
Before Instru REG1	ction = 0xA5						
After Instruct REG1 W	ion = 0xA5 = 0X5A						

TRIS	Load TRIS Register							
Syntax:	[label] TRIS f							
Operands:	f = 6							
Operation:	$(W) \to TRIS \text{ register f}$							
Status Affected:	None							
Encoding:	0000 0000 0fff							
Description:	TRIS register 'f' (f = 6) is loaded with the contents of the W register							
Words:	1							
Cycles:	1							
Example	TRIS GPIO							
Before Instru W	ction = 0XA5							
After Instruct TRIS	ion = 0XA5							
<b>Note:</b> f = 6 for	or PIC12C5XX only.							

XORLW	e OR lite	ral with V	N	
Syntax:	[ <i>label</i> ]	XORLW	k	
Operands:	$0 \le k \le 2$	55		
Operation:	(W) .XOF	$R. k \to (W)$	/)	
Status Affected:	Z			
Encoding:	1111	kkkk	kkkk	
Description:	The conte XOR'ed w result is pl	nts of the vith the eigl laced in the	W register ht bit literal e W registe	are 'k'. The er.
Words:	1			
Cycles:	1			
Example:	XORLW	0xAF		
Before Instru	iction			
W =	0xB5			
After Instruct	ion			
W =	0x1A			

XORWF Exclusive OR W with f					
Syntax:	[ label ]	XORWF	f,d		
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in \left[0,1\right] \end{array}$				
Operation:	(W) .XOR. (f) $\rightarrow$ (dest)				
Status Affected: Z					
Encoding:	0001	10df	ffff		
Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' 1 the result is stored back in register'					
Words:	1				
Cycles:	1				
Example XORWF REG, 1					
Before Instru REG W	ction = 0x/ = 0xf	AF 35			
After Instruct REG W	ion = 0x <sup>-</sup> = 0xl	1A 35			







FIGURE 12-8: IOL vs. VOL, VDD = 5.5 V



#### 13.5 <u>Timing Parameter Symbology and Load Conditions - PIC12C508A, PIC12C509A,</u> PIC12CR509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519

The timing parameter symbols have been created following one of the following formats:

1. TPPSZPPS	1.	Тр	pS2	ppS
-------------	----	----	-----	-----

2. TppS

z. rpps			
т			
F	Frequency	Т	Time
Lowerc	ase subscripts (pp) and their meanings:		
рр			
2	to	mc	MCLR
ck	CLKOUT	osc	oscillator
су	cycle time	os	OSC1
drt	device reset timer	t0	TOCKI
io	I/O port	wdt	watchdog timer
Upperc	ase letters and their meanings:		
S			
F	Fall	Р	Period
Н	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

# FIGURE 13-1: LOAD CONDITIONS - PIC12C508A/C509A, PIC12CE518/519, PIC12LC508A/509A, PIC12LCE518/519, PIC12LCR509A



# PIC12C5XX

#### 13.6 Timing Diagrams and Specifications

#### FIGURE 13-2: EXTERNAL CLOCK TIMING - PIC12C508A, PIC12C509A, PIC12CR509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519



#### TABLE 13-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519

AC Characteristics		$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ (commercial)}, \\ & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ (industrial)}, \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ (extended)} \\ \mbox{Operating Voltage VDD range is described in Section 13.1} \end{array}$						
Parameter No.	Sym	Characteristic	Min	Тур <sup>(1)</sup>	Мах	Units	Conditions	
	Fosc	External CLKIN Frequency <sup>(2)</sup>						
			DC	—	4	MHz	XT osc mode	
			DC	—	200	kHz	LP osc mode	
		Oscillator Frequency <sup>(2)</sup>	DC	—	4	MHz	EXTRC osc mode	
			0.1	—	4	MHz	XT osc mode	
			DC	—	200	kHz	LP osc mode	
1	Tosc	External CLKIN Period <sup>(2)</sup>						
			250	—	_	ns	XT osc mode	
			5	—		ms	LP osc mode	
		Oscillator Period <sup>(2)</sup>	250	—	—	ns	EXTRC osc mode	
			250	—	10,000	ns	XT osc mode	
			5	—	Ι	ms	LP osc mode	
2	Тсу	Instruction Cycle Time <sup>(3)</sup>	—	4/Fosc	—	—		
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—		ns	XT oscillator	
			2*	—	—	ms	LP oscillator	
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator	
			—	—	50*	ns	LP oscillator	

\* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

#### TABLE 13-3: CALIBRATED INTERNAL RC FREQUENCIES - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519

AC Characteristics Standard Operating Conditions (unless otherwise specified)   Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ (commercial), $-40^{\circ}C \le TA \le +85^{\circ}C$ (industrial), $-40^{\circ}C \le TA \le +125^{\circ}C$ (extended)   Operating Voltage VDD range is described in Section 10.1							
Parameter No.	Sym	Characteristic	Min*	Тур <sup>(1)</sup>	Max*	Units	Conditions
		Internal Calibrated RC Frequency	3.65	4.00	4.28	MHz	VDD = 5.0V
		Internal Calibrated RC Frequency	3.55	—	4.31	MHz	VDD = 2.5V

\* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

# 14.0 DC AND AC CHARACTERISTICS - PIC12C508A/PIC12C509A/ PIC12LC508A/PIC12LC509A, PIC12CE518/PIC12CE519/PIC12CR509A/ PIC12LCE518/PIC12LCE519/ PIC12LCR509A

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean +  $3\sigma$ ) and (mean -  $3\sigma$ ) respectively, where  $\sigma$  is standard deviation.







FIGURE 14-6: SHORT DRT PERIOD VS. VDD



FIGURE 14-7: IOH vs. VOH, VDD = 2.5 V



FIGURE 14-8: IOH vs. VOH, VDD = 3.5 V

