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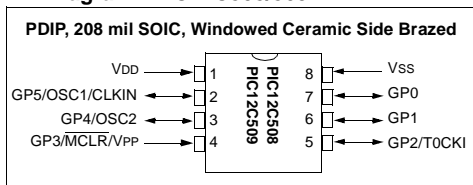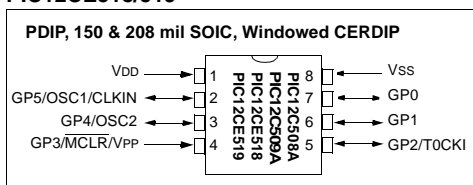
Applications of "**Embedded - Microcontrollers**"

Details

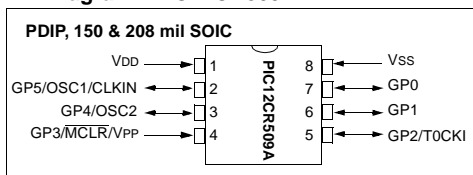|	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12lc508a-04-p

PIC12C5XX

Pin Diagram - PIC12C508/509

PDIP, 208 mil SOIC, Windowed Ceramic Side Brazed

VDD →	1	8	← VSS
GP5/OSC1/CLKIN ↔	2	7	↔ GP0
GP4/OSC2 ↔	3	6	↔ GP1
GP3/MCLR/VPP →	4	5	↔ GP2/T0CKI

(Device: PIC12C508 / PIC12C509)

Pin Diagram - PIC12C508A/509A, PIC12CE518/519

PDIP, 150 & 208 mil SOIC, Windowed CERDIP

VDD →	1	8	← VSS
GP5/OSC1/CLKIN ↔	2	7	↔ GP0
GP4/OSC2 ↔	3	6	↔ GP1
GP3/MCLR/VPP →	4	5	↔ GP2/T0CKI

(Device: PIC12C508A / PIC12C509A / PIC12CE518 / PIC12CE519)

Pin Diagram - PIC12CR509A

PDIP, 150 & 208 mil SOIC

VDD →	1	8	← VSS
GP5/OSC1/CLKIN ↔	2	7	↔ GP0
GP4/OSC2 ↔	3	6	↔ GP1
GP3/MCLR/VPP →	4	5	↔ GP2/T0CKI

(Device: PIC12CR509A)

Device Differences

Device	Voltage Range	Oscillator	Oscillator Calibration[2] (Bits)	Process Technology (Microns)
PIC12C508A	3.0-5.5	See Note 1	6	0.7
PIC12LC508A	2.5-5.5	See Note 1	6	0.7
PIC12C508	2.5-5.5	See Note 1	4	0.9
PIC12C509A	3.0-5.5	See Note 1	6	0.7
PIC12LC509A	2.5-5.5	See Note 1	6	0.7
PIC12C509	2.5-5.5	See Note 1	4	0.9
PIC12CR509A	2.5-5.5	See Note 1	6	0.7
PIC12CE518	3.0-5.5	-	6	0.7
PIC12LCE518	2.5-5.5	-	6	0.7
PIC12CE519	3.0-5.5	-	6	0.7
PIC12LCE519	2.5-5.5	-	6	0.7

Note 1: If you change from the PIC12C50X to the PIC12C50XA or to the PIC12CR50XA, please verify oscillator characteristics in your application.

Note 2: See Section 7.2.5 for OSCCAL implementation differences.

PIC12C5XX

1.0   GENERAL DESCRIPTION

The PIC12C5XX from Microchip Technology is a family of low-cost, high performance, 8-bit, fully static, EEPROM/EPROM/ROM-based CMOS microcontrollers. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle (1 μs) except for program branches which take two cycles. The PIC12C5XX delivers performance an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC12C5XX products are equipped with special features that reduce system cost and power requirements. The Power-On Reset (POR) and Device Reset Timer (DRT) eliminate the need for external reset circuitry. There are four oscillator configurations to choose from, including INTRC internal oscillator mode and the power-saving LP (Low Power) oscillator mode. Power saving SLEEP mode, Watchdog Timer and code protection features also improve system cost, power and reliability.

The PIC12C5XX are available in the cost-effective One-Time-Programmable (OTP) versions which are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers while benefiting from the OTP's flexibility.

The PIC12C5XX products are supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a 'C' compiler, fuzzy logic support tools, a low-cost development programmer, and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

1.1   Applications

The PIC12C5XX series fits perfectly in applications ranging from personal care appliances and security systems to low-power remote transmitters/receivers. The EPROM technology makes customizing application programs (transmitter codes, appliance settings, receiver frequencies, etc.) extremely fast and convenient, while the EEPROM data memory technology allows for the changing of calibration factors and security codes. The small footprint packages, for through hole or surface mounting, make this microcontroller series perfect for applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the PIC12C5XX series very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic and PLD's in larger systems, coprocessor applications).

4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1).

The special registers can be classified into two sets. The special function registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

TABLE 4-1: SPECIAL FUNCTION REGISTER (SFR) SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets[2]
N/A	TRIS	—	—							--11 1111	--11 1111
N/A	OPTION	Contains control bits to configure Timer0, Timer0/WDT prescaler, wake-up on change, and weak pull-ups								1111 1111	1111 1111
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
01h	TMR0	8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
02h[1]	PCL	Low order 8 bits of PC								1111 1111	1111 1111
03h	STATUS	GPWUF	—	PA0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	q00q quuu[3]
04h	FSR (PIC12C508/ PIC12C508A/ PIC12C518)	Indirect data memory address pointer								111x xxxx	111u uuuu
04h	FSR (PIC12C509/ PIC12C509A/ PIC12CR509A/ PIC12CE519)	Indirect data memory address pointer								110x xxxx	11uu uuuu
05h	OSCCAL (PIC12C508/ PIC12C509)	CAL3	CAL2	CAL1	CAL0	—	—	—	—	0111 ----	uuuu ----
05h	OSCCAL (PIC12C508A/ PIC12C509A/ PIC12CE518/ PIC12CE519/ PIC12CR509A)	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	—	1000 00--	uuuu uu--
06h	GPIO (PIC12C508/ PIC12C509/ PIC12C508A/ PIC12C509A/ PIC12CR509A)	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	--uu uuuu
06h	GPIO (PIC12CE518/ PIC12CE519)	SCL	SDA	GP5	GP4	GP3	GP2	GP1	GP0	11xx xxxx	11uu uuuu

Legend: Shaded boxes = unimplemented or unused, − = unimplemented, read as '0' (if applicable)
x = unknown, u = unchanged, q = see the tables in Section 8.7 for possible values.

Note 1: The upper byte of the Program Counter is not directly accessible. See Section 4.6 for an explanation of how to access these bits.

2: Other (non power-up) resets include external reset through $\overline{\text{MCLR}}$, watchdog timer and wake-up on pin change reset.

3: If reset was due to wake-up on pin change then bit 7 = 1. All other resets will cause bit 7 = 0.

PIC12C5XX

5.0   I/O PORT

As with any other register, the I/O register can be written and read under program control. However, read instructions (e.g., MOVF GPIO,W) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers are all set. See Section 7.0 for SCL and SDA description for PIC12CE5XX.

5.1   GPIO

GPIO is an 8-bit I/O register. Only the low order 6 bits are used (GP5:GP0). Bits 7 and 6 are unimplemented and read as '0's. Please note that GP3 is an input only pin. The configuration word can set several I/O's to alternate functions. When acting as alternate functions the pins will read as '0' during port read. Pins GP0, GP1, and GP3 can be configured with weak pull-ups and also with wake-up on change. The wake-up on change and weak pull-up functions are not pin selectable. If pin 4 is configured as MCLR, weak pull-up is always on and wake-up on change for this pin is not enabled.

5.2   TRIS Register

The output driver control register is loaded with the contents of the W register by executing the TRIS f instruction. A '1' from a TRIS register bit puts the corresponding output driver in a hi-impedance mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer. The exceptions are GP3 which is input only and GP2 which may be controlled by the option register, see Figure 4-5.

> **Note:** A read of the ports reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high, but the external system is holding it low, a read of the port will indicate that the pin is low.

The TRIS registers are "write-only" and are set (output drivers disabled) upon RESET.

5.3   I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 5-1. All port pins, except GP3 which is input only, may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., MOVF GPIO,W). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit in TRIS must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin (except GP3) can be programmed individually as input or output.
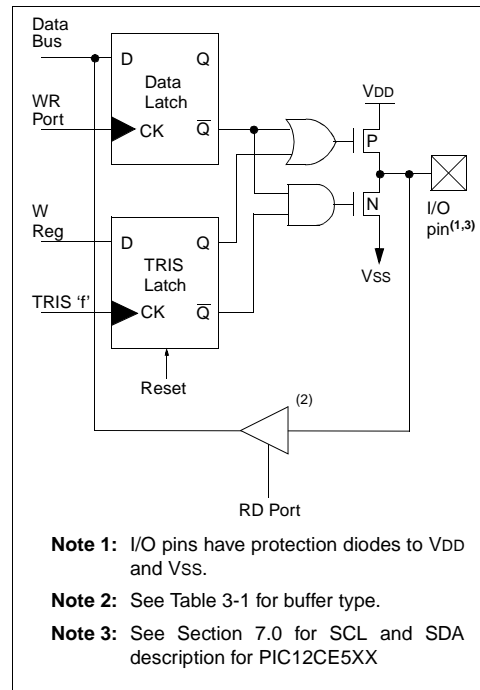
FIGURE 5-1:   EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN

Note 1: I/O pins have protection diodes to VDD and VSS.

Note 2: See Table 3-1 for buffer type.

Note 3: See Section 7.0 for SCL and SDA description for PIC12CE5XX

PIC12C5XX

TABLE 5-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	TRIS	—	—							--11 1111	--11 1111
N/A	OPTION	$\overline{GPWU}$	$\overline{GPPU}$	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
03H	STATUS	GPWUF	—	PAO	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	q00q quuu[(1)]
06h	GPIO (PIC12C508/ PIC12C509/ PIC12C508A/ PIC12C509A/ PIC12CR509A)	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	--uu uuuu
06h	GPIO (PIC12CE518/ PIC12CE519)	SCL	SDA	GP5	GP4	GP3	GP2	GP1	GP0	11xx xxxx	11uu uuuu

Legend: Shaded cells not used by Port Registers, read as '0', — = unimplemented, read as '0', x = unknown, u = unchanged,
q = see tables in Section 8.7 for possible values.

Note 1: If reset was due to wake-up on change, then bit 7 = 1. All other resets will cause bit 7 = 0.

5.4   I/O Programming Considerations

5.4.1   BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of GPIO will cause all eight bits of GPIO to be read into the CPU, bit5 to be set and the GPIO value to be written to the output latches. If another bit of GPIO is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

EXAMPLE 5-1:   READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial GPIO Settings
; GPIO<5:3> Inputs
; GPIO<2:0> Outputs
;
;                   GPIO latch  GPIO pins
;                   ----------  ----------
  BCF    GPIO, 5  ;--01 -ppp   --11 pppp
  BCF    GPIO, 4  ;--10 -ppp   --11 pppp
  MOVLW 007h      ;
  TRIS   GPIO     ;--10 -ppp   --11 pppp
;
;Note that the user may have expected the pin
;values to be --00 pppp. The 2nd BCF caused
;GP5 to be latched as the pin value (High).
```

5.4.2   SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

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6.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
  - Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
  - Edge select for external clock

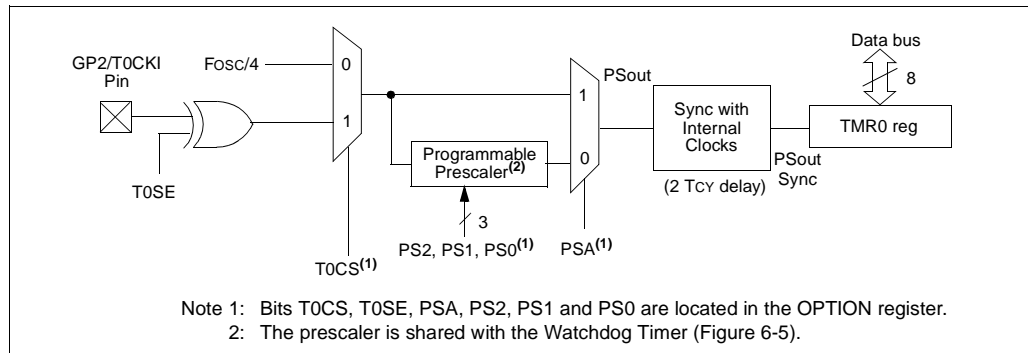Figure 6-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two instruction cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The T0SE bit (OPTION<4>) determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.1.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. Section 6.2 details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 6-1.

FIGURE 6-1: TIMER0 BLOCK DIAGRAM

Note 1: Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in the OPTION register.
2: The prescaler is shared with the Watchdog Timer (Figure 6-5).

6.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (T$_{OSC}$) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

6.1.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-4). Therefore, it is necessary for T0CKI to be high for at least 2T$_{OSC}$ (and a small RC delay of 20 ns) and low for at least 2T$_{OSC}$ (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4T$_{OSC}$ (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.
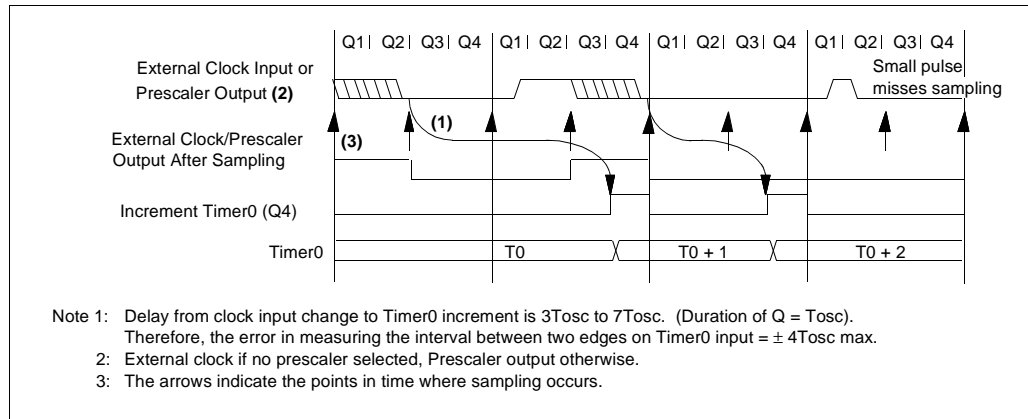
6.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 6-4 shows the delay from the external clock edge to the timer incrementing.

6.1.3 OPTION REGISTER EFFECT ON GP2 TRIS

If the option register is set to read TIMER0 from the pin, the port is forced to an input regardless of the TRIS register setting.

FIGURE 6-4: TIMER0 TIMING WITH EXTERNAL CLOCK

Note 1: Delay from clock input change to Timer0 increment is 3Tosc to 7Tosc. (Duration of Q = Tosc). Therefore, the error in measuring the interval between two edges on Timer0 input = ± 4Tosc max.
2: External clock if no prescaler selected, Prescaler output otherwise.
3: The arrows indicate the points in time where sampling occurs.

7.0 EEPROM PERIPHERAL OPERATION

This section applies to PIC12CE518 and PIC12CE519 only.

The PIC12CE518 and PIC12CE519 each have 16 bytes of EEPROM data memory. The EEPROM memory has an endurance of 1,000,000 erase/write cycles and a data retention of greater than 40 years. The EEPROM data memory supports a bi-directional 2-wire bus and data transmission protocol. These two-wires are serial data (SDA) and serial clock (SCL), that are mapped to bit6 and bit7, respectively, of the GPIO register (SFR 06h). Unlike the GP0-GP5 that are connected to the I/O pins, SDA and SCL are only connected to the internal EEPROM peripheral. For most applications, all that is required is calls to the following functions:

```
; Byte_Write: Byte write routine
;     Inputs: EEPROM Address     EEADDR
;             EEPROM Data        EEDATA
;     Outputs:   Return 01 in W if OK, else
;                return 00 in W
;
; Read_Current: Read EEPROM at address
currently held by EE device.
;     Inputs: NONE
;     Outputs:   EEPROM Data    EEDATA
;                Return 01 in W if OK, else
;                return 00 in W
;
; Read_Random: Read EEPROM byte at supplied
address
;     Inputs: EEPROM Address     EEADDR
;     Outputs:   EEPROM Data    EEDATA
;                Return 01 in W if OK,
;                else return 00 in W
```

The code for these functions is available on our website www.microchip.com. The code will be accessed by either including the source code FL51XINC.ASM or by linking FLASH5IX.ASM.

It is very important to check the return codes when using these calls, and retry the operation if unsuccessful. Unsuccessful return codes occur when the EE data memory is busy with the previous write, which can take up to 4 mS.

7.0.1 SERIAL DATA

SDA is a bi-directional pin used to transfer addresses and data into and data out of the device.

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

The EEPROM interface is a 2-wire bus protocol consisting of data (SDA) and a clock (SCL). Although these lines are mapped into the GPIO register, they are not accessible as external pins; only to the internal EEPROM peripheral. SDA and SCL operation is also slightly different than GPO-GP5 as listed below.

Namely, to avoid code overhead in modifying the TRIS register, both SDA and SCL are always outputs. To read data from the EEPROM peripheral requires outputting a '1' on SDA placing it in high-Z state, where only the internal 100K pull-up is active on the SDA line.

SDA:
  Built-in 100K (typical) pull-up to VDD
  Open-drain (pull-down only)
  Always an output
  Outputs a '1' on reset

SCL:
  Full CMOS output
  Always an output
  Outputs a '1' on reset

The following example requires:

- Code Space: 77 words
- RAM Space: 5 bytes (4 are overlayable)
- Stack Levels:1 (The call to the function itself. The functions do not call any lower level functions.)
- Timing:
  - WRITE_BYTE takes 328 cycles
  - READ_CURRENT takes 212 cycles
  - READ_RANDOM takes 416 cycles.
- IO Pins: 0 (No external IO pins are used)

This code must reside in the lower half of a page. The code achieves it's small size without additional calls through the use of a sequencing table. The table is a list of procedures that must be called in order. The table uses an ADDWF PCL,F instruction, effectively a computed goto, to sequence to the next procedure. However the ADDWF PCL,F instruction yields an 8 bit address, forcing the code to reside in the first 256 addresses of a page.

PIC12C5XX

BSF	Bit Set f
Syntax:	[*label*] BSF f,b
Operands:	$0 \le f \le 31$ $0 \le b \le 7$
Operation:	$1 \rightarrow$ (f\<b\>)
Status Affected:	None

Encoding:

0101	bbbf	ffff

Description:	Bit 'b' in register 'f' is set.
Words:	1
Cycles:	1
Example:	BSF FLAG_REG, 7

Before Instruction
    FLAG_REG = 0x0A
After Instruction
    FLAG_REG = 0x8A

BTFSC	Bit Test f, Skip if Clear
Syntax:	[*label*] BTFSC f,b
Operands:	$0 \le f \le 31$ $0 \le b \le 7$
Operation:	skip if (f\<b\>) = 0
Status Affected:	None

Encoding:

0110	bbbf	ffff

Description:	If bit 'b' in register 'f' is 0 then the next instruction is skipped. If bit 'b' is 0 then the next instruction fetched during the current instruction execution is discarded, and an NOP is executed instead, making this a 2 cycle instruction.
Words:	1
Cycles:	1(2)

Example:	HERE BTFSC FLAG,1
	FALSE GOTO PROCESS_CODE
	TRUE •
	   •
	   •

Before Instruction
    PC   =   address (HERE)
After Instruction
    if FLAG\<1\> =   0,
    PC   =   address (TRUE);
    if FLAG\<1\> =   1,
    PC   =   address(FALSE)

BTFSS	Bit Test f, Skip if Set
Syntax:	[*label*] BTFSS f,b
Operands:	$0 \le f \le 31$ $0 \le b < 7$
Operation:	skip if (f\<b\>) = 1
Status Affected:	None

Encoding:

0111	bbbf	ffff

Description:	If bit 'b' in register 'f' is '1' then the next instruction is skipped. If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and an NOP is executed instead, making this a 2 cycle instruction.
Words:	1
Cycles:	1(2)

Example:	HERE BTFSS FLAG,1
	FALSE GOTO PROCESS_CODE
	TRUE •
	   •
	   •

Before Instruction
    PC   =   address (HERE)
After Instruction
    If FLAG\<1\> =   0,
    PC   =   address (FALSE);
    if FLAG\<1\> =   1,
    PC   =   address (TRUE)

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CALL	**Subroutine Call**
Syntax:	[*label*] CALL k
Operands:	0 ≤ k ≤ 255
Operation:	(PC) + 1→ Top of Stack; k → PC<7:0>; (STATUS<6:5>) → PC<10:9>; 0 → PC<8>
Status Affected:	None

Encoding:

1001	kkkk	kkkk

Description:	Subroutine call. First, return address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two cycle instruction.
Words:	1
Cycles:	2
Example:	HERE CALL THERE

Before Instruction
PC =   address (HERE)

After Instruction
PC =   address (THERE)
TOS =   address (HERE + 1)

CLRF	**Clear f**
Syntax:	[*label*] CLRF f
Operands:	0 ≤ f ≤ 31
Operation:	00h → (f); 1 → Z
Status Affected:	Z

Encoding:

0000	011f	ffff

Description:	The contents of register 'f' are cleared and the Z bit is set.
Words:	1
Cycles:	1
Example:	CLRF FLAG_REG

Before Instruction
FLAG_REG =   0x5A

After Instruction
FLAG_REG =   0x00
Z   =   1

CLRW	**Clear W**
Syntax:	[*label*] CLRW
Operands:	None
Operation:	00h → (W); 1 → Z
Status Affected:	Z

Encoding:

0000	0100	0000

Description:	The W register is cleared. Zero bit (Z) is set.
Words:	1
Cycles:	1
Example:	CLRW

Before Instruction
W =   0x5A

After Instruction
W =   0x00
Z =   1

CLRWDT	**Clear Watchdog Timer**
Syntax:	[*label*] CLRWDT
Operands:	None
Operation:	00h → WDT; 0 → WDT prescaler (if assigned); 1 → $\overline{TO}$; 1 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$

Encoding:

0000	0000	0100

Description:	The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits $\overline{TO}$ and $\overline{PD}$ are set.
Words:	1
Cycles:	1
Example:	CLRWDT

Before Instruction
WDT counter =   ?

After Instruction
WDT counter =   0x00
WDT prescale =   0
$\overline{TO}$ =   1
$\overline{PD}$ =   1

NOTES:

11.1 DC CHARACTERISTICS: PIC12C508/509 (Commercial, Industrial, Extended)

	DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature $0°C \leq T_A \leq +70°C$ (commercial) $-40°C \leq T_A \leq +85°C$ (industrial) $-40°C \leq T_A \leq +125°C$ (extended)					
Parm No.	Characteristic	Sym	Min	Typ[1]	Max	Units	Conditions
D001	**Supply Voltage**	V_{DD}	2.5		5.5	V	F_{OSC} = DC to 4 MHz (Commercial/ Industrial)
			3.0		5.5	V	F_{OSC} = DC to 4 MHz (Extended)
D002	**RAM Data Retention Voltage**[2]	V_{DR}		1.5*		V	Device in SLEEP mode
D003	**V_{DD} Start Voltage to ensure Power-on Reset**	V_{POR}		V_{SS}		V	See section on Power-on Reset for details
D004	**V_{DD} Rise Rate to ensure Power-on Reset**	S_{VDD}	0.05 *			V/ms	See section on Power-on Reset for details
D010	**Supply Current**[3]	I_{DD}	—	.78	2.4	mA	XT and EXTRC options [4] F_{OSC} = 4 MHz, V_{DD} = 5.5V
D010C			—	1.1	2.4	mA	INTRC Option F_{OSC} = 4 MHz, V_{DD} = 5.5V
D010A			—	10	27	µA	LP OPTION, Commercial Temperature F_{OSC} = 32 kHz, V_{DD} = 3.0V, WDT disabled
			—	14	35	µA	LP OPTION, Industrial Temperature F_{OSC} = 32 kHz, V_{DD} = 3.0V, WDT disabled
			—	14	35	µA	LP OPTION, Extended Temperature F_{OSC} = 32 kHz, V_{DD} = 3.0V, WDT disabled
D020 D021 D021B	**Power-Down Current** [5]	I_{PD}	— — —	0.25 0.25 2	4 5 18	µA µA µA	V_{DD} = 3.0V, Commercial WDT disabled V_{DD} = 3.0V, Industrial WDT disabled V_{DD} = 3.0V, Extended WDT disabled
D022		ΔI_{WDT}	— — —	3.75 3.75 3.75	8 9 14	µA µA µA	V_{DD} = 3.0V, Commercial V_{DD} = 3.0V, Industrial V_{DD} = 3.0V, Extended

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

    a) The test conditions for all I_{DD} measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to
V_{SS}, T0CKI = V_{DD}, $\overline{MCLR}$ = V_{DD}; WDT enabled/disabled as specified.

    b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: I_R = V_{DD}/2Rext (mA) with Rext in kOhm.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD} or V_{SS}.
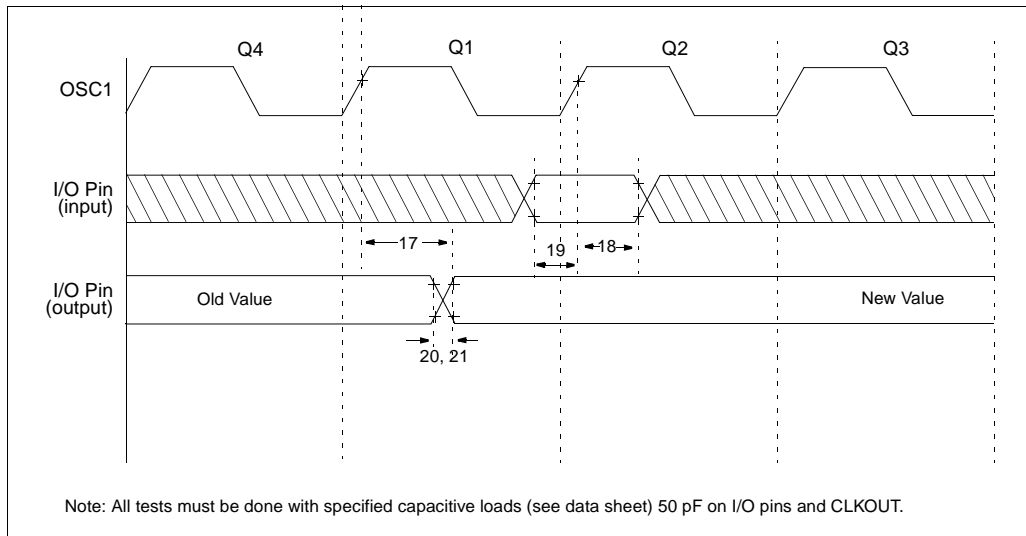
TABLE 11-3:   CALIBRATED INTERNAL RC FREQUENCIES - PIC12C508/C509

AC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature $0°C ≤ T_A ≤ +70°C$ (commercial), $-40°C ≤ T_A ≤ +85°C$ (industrial), $-40°C ≤ T_A ≤ +125°C$ (extended) Operating Voltage V_{DD} range is described in Section 10.1					
Parameter No.	Sym	Characteristic	Min*	Typ[1]	Max*	Units	Conditions
		Internal Calibrated RC Frequency	3.58	4.00	4.32	MHz	$V_{DD} = 5.0V$
		Internal Calibrated RC Frequency	3.50	—	4.26	MHz	$V_{DD} = 2.5V$

*   These parameters are characterized but not tested.
Note 1:   Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 11-3:   I/O TIMING - PIC12C508/C509

Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

13.1 DC CHARACTERISTICS: PIC12C508A/509A (Commercial, Industrial, Extended)
PIC12CE518/519 (Commercial, Industrial, Extended)
PIC12CR509A (Commercial, Industrial, Extended)

DC Characteristics Power Supply Pins				Standard Operating Conditions (unless otherwise specified)				
				Operating Temperature	$0°C \leq T_A \leq +70°C$ (commercial)			
					$-40°C \leq T_A \leq +85°C$ (industrial)			
					$-40°C \leq T_A \leq +125°C$ (extended)			
Parm No.	Characteristic	Sym	Min	Typ[1]	Max	Units	Conditions	
D001	Supply Voltage	V_{DD}	3.0		5.5	V	F_{OSC} = DC to 4 MHz (Commercial/ Industrial, Extended)	
D002	RAM Data Retention Voltage[2]	V_{DR}		1.5*		V	Device in SLEEP mode	
D003	V_{DD} Start Voltage to ensure Power-on Reset	V_{POR}		V_{SS}		V	See section on Power-on Reset for details	
D004	V_{DD} Rise Rate to ensure Power-on Reset	S_{VDD}	0.05*			V/ms	See section on Power-on Reset for details	
D010	Supply Current[3]	I_{DD}	—	0.8	1.4	mA	XT and EXTRC options (Note 4) F_{OSC} = 4 MHz, V_{DD} = 5.5V	
D010C			—	0.8	1.4	mA	INTRC Option F_{OSC} = 4 MHz, V_{DD} = 5.5V	
D010A			—	19	27	µA	LP OPTION, Commercial Temperature F_{OSC} = 32 kHz, V_{DD} = 3.0V, WDT disabled	
			—	19	35	µA	LP OPTION, Industrial Temperature F_{OSC} = 32 kHz, V_{DD} = 3.0V, WDT disabled	
			—	30	55	µA	LP OPTION, Extended Temperature F_{OSC} = 32 kHz, V_{DD} = 3.0V, WDT disabled	
D020 D021 D021B	Power-Down Current [5]	I_{PD}	— — —	0.25 0.25 2	4 5 12	µA µA µA	V_{DD} = 3.0V, Commercial WDT disabled V_{DD} = 3.0V, Industrial WDT disabled V_{DD} = 3.0V, Extended WDT disabled	
D022	Power-Down Current	ΔI_{WDT}	— — —	2.2 2.2 4	5 6 11	µA µA µA	V_{DD} = 3.0V, Commercial V_{DD} = 3.0V, Industrial V_{DD} = 3.0V, Extended	
	Supply Current [3] During read/write to EEPROM peripheral	ΔI_{EE}	—	0.1	0.2	mA	F_{OSC} = 4 MHz, Vdd = 5.5V, SCL = 400kHz	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

　a) The test conditions for all I_{DD} measurements in active operation mode are:
　　OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V_{SS}, T0CKI = V_{DD}, $\overline{MCLR}$ = V_{DD}; WDT enabled/disabled as specified.
　b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: I_R = V_{DD}/2Rext (mA) with Rext in kOhm.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD} or V_{SS}.

13.4   DC CHARACTERISTICS: PIC12LC508A/509A (Commercial, Industrial)
PIC12LC518/519 (Commercial, Industrial)
PIC12LCR509A (Commercial, Industrial)

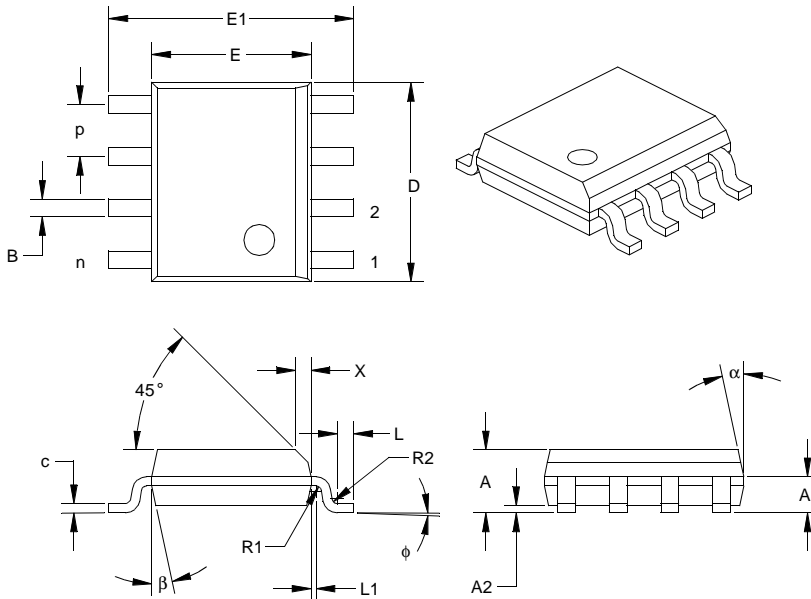| DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) −40°C ≤ TA ≤ +85°C (industrial) Operating voltage VDD range as described in DC spec Section 13.1 and Section 13.2.					
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions	
	Input Low Voltage							
	I/O ports	VIL						
D030	with TTL buffer		Vss	-	0.8V	V	For 4.5V ≤ VDD ≤ 5.5V	
			Vss	-	0.15VDD	V	otherwise	
D031	with Schmitt Trigger buffer		Vss	-	0.2VDD	V		
D032	$\overline{MCLR}$, GP2/T0CKI (in EXTRC mode)		Vss	-	0.2VDD	V		
D033	OSC1 (in EXTRC mode)		Vss	-	0.2VDD	V	Note 1	
D033	OSC1 (in XT and LP)		Vss	-	0.3VDD	V	Note 1	
	Input High Voltage							
	I/O ports	VIH		-				
D040	with TTL buffer		0.25VDD + 0.8V	-	VDD	V	4.5V ≤ VDD ≤ 5.5V	
D040A			2.0V	-	VDD	V	otherwise	
D041	with Schmitt Trigger buffer		0.8VDD	-	VDD	V	For entire VDD range	
D042	$\overline{MCLR}$, GP2/T0CKI		0.8VDD	-	VDD	V		
D042A	OSC1 (XT and LP)		0.7VDD	-	VDD	V	Note 1	
D043	OSC1 (in EXTRC mode)		0.9VDD	-	VDD	V		
D070	GPIO weak pull-up current (Note 4)	IPUR	30	250	400	µA	VDD = 5V, VPIN = VSS	
	$\overline{MCLR}$ pull-up current	-	-	-	30	µA	VDD = 5V, VPIN = VSS	
	Input Leakage Current (Notes 2, 3)							
D060	I/O ports	IIL	-	-	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance	
D061	T0CKI		-	-	±5	µA	Vss ≤ VPIN ≤ VDD	
D063	OSC1		-	-	±5	µA	Vss ≤ VPIN ≤ VDD, XT and LP osc configuration	
	Output Low Voltage							
D080	I/O ports	VOL	-	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V, −40°C to +85°C	
D080A			-	-	0.6	V	IOL = 7.0 mA, VDD = 4.5V, −40°C to +125°C	
	Output High Voltage							
D090	I/O ports (Note 3)	VOH	VDD - 0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, −40°C to +85°C	
D090A			VDD - 0.7	-	-	V	IOH = -2.5 mA, VDD = 4.5V, −40°C to +125°C	
	Capacitive Loading Specs on Output Pins							
D100	OSC2 pin	COSC2	-	-	15	pF	In XT and LP modes when external clock is used to drive OSC1.	
D101	All I/O pins	CIO	-	-	50	pF		

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C5XX be driven with external clock in RC mode.
2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
3: Negative current is defined as coming out of the pin.
4: This spec. applies when GP3/$\overline{MCLR}$ is configured as $\overline{MCLR}$. The leakage current of the $\overline{MCLR}$ circuit is higher than the standard I/O logic.

NOTES:

Package Type: K04-057 8-Lead Plastic Small Outline (SN) – Narrow, 150 mil

Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.050			1.27	
Number of Pins	n		8			8	
Overall Pack. Height	A	0.054	0.061	0.069	1.37	1.56	1.75
Shoulder Height	A1	0.027	0.035	0.044	0.69	0.90	1.11
Standoff	A2	0.004	0.007	0.010	0.10	0.18	0.25
Molded Package Length	D‡	0.189	0.193	0.196	4.80	4.89	4.98
Molded Package Width	E‡	0.150	0.154	0.157	3.81	3.90	3.99
Outside Dimension	E1	0.229	0.237	0.244	5.82	6.01	6.20
Chamfer Distance	X	0.010	0.015	0.020	0.25	0.38	0.51
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	φ	0	4	8	0	4	8
Radius Centerline	L1	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.009	0.010	0.19	0.22	0.25
Lower Lead Width	B†	0.014	0.017	0.020	0.36	0.43	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter.

† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

NOTES: