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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.209", 5.30mm Width)
Supplier Device Package	8-SOIJ
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12lc508a-04-sm

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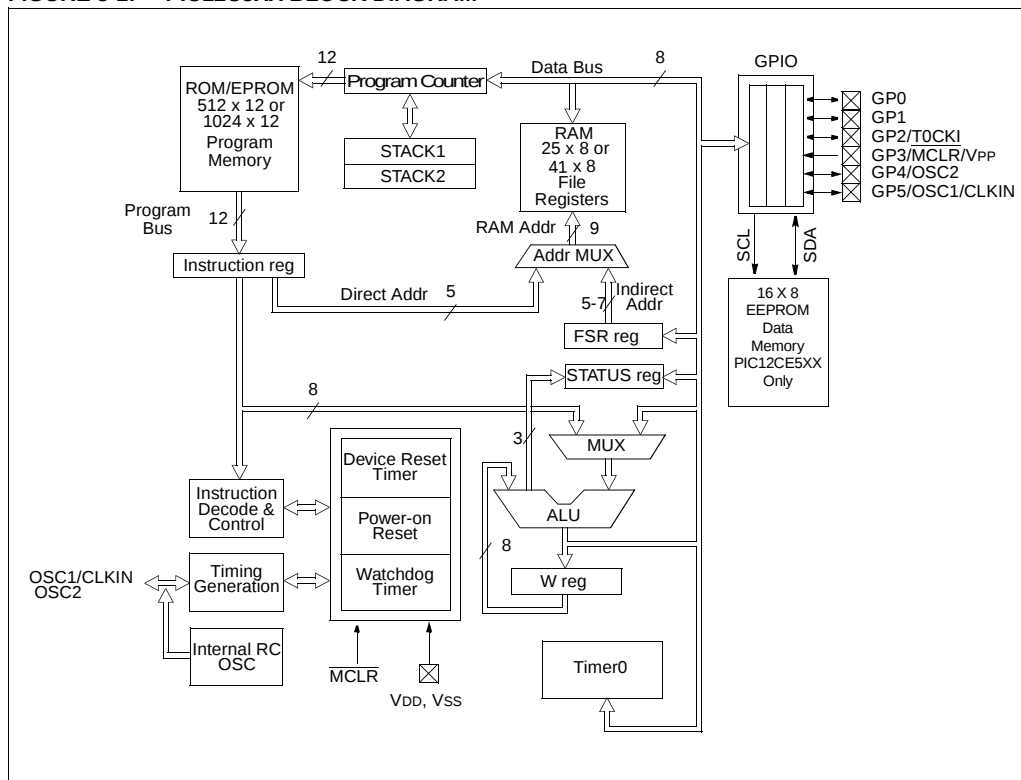
We appreciate your assistance in making this a better document.

PIC12C5XX

NOTES:

PIC12C5XX

FIGURE 3-1: PIC12C5XX BLOCK DIAGRAM



4.4 OPTION Register

The OPTION register is a 8-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the OPTION instruction, the contents of the W register will be transferred to the OPTION register. A RESET sets the OPTION<7:0> bits.

Note: If TRIS bit is set to '0', the wake-up on change and pull-up functions are disabled for that pin; i.e., note that TRIS overrides OPTION control of $\overline{\text{GPPU}}$ and $\overline{\text{GPWU}}$.

Note: If the T0CS bit is set to '1', GP2 is forced to be an input even if TRIS GP2 = '0'.

FIGURE 4-5: OPTION REGISTER

W-1	W-1	W-1	W-1	W-1	W-1	W-1	W-1
$\overline{\text{GPWU}}$	$\overline{\text{GPPU}}$	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7	6	5	4	3	2	1	bit0

W = Writable bit
U = Unimplemented bit
- n = Value at POR reset
Reference Table 4-1 for other resets.

bit 7: **$\overline{\text{GPWU}}$** : Enable wake-up on pin change (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 6: **$\overline{\text{GPPU}}$** : Enable weak pull-ups (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 5: **T0CS**: Timer0 clock source select bit
1 = Transition on T0CKI pin
0 = Transition on internal instruction cycle clock, Fosc/4

bit 4: **T0SE**: Timer0 source edge select bit
1 = Increment on high to low transition on the T0CKI pin
0 = Increment on low to high transition on the T0CKI pin

bit 3: **PSA**: Prescaler assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0: **PS2:PS0**: Prescaler rate select bits

Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

PIC12C5XX

4.8 Indirect Data Addressing: INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 4-1: INDIRECT ADDRESSING

- Register file 07 contains the value 10h
- Register file 08 contains the value 0Ah
- Load the value 07 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 08)
- A read of the INDR register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```

movlw 0x10 ;initialize pointer
movwf FSR ; to RAM
NEXT   clrf INDF ;clear INDF register
       incf FSR,F ;inc pointer
       btfsc FSR,4 ;all done?
       goto NEXT ;NO, clear next

CONTINUE
:      ;YES, continue
  
```

The FSR is a 5-bit wide register. It is used in conjunction with the INDF register to indirectly address the data memory area.

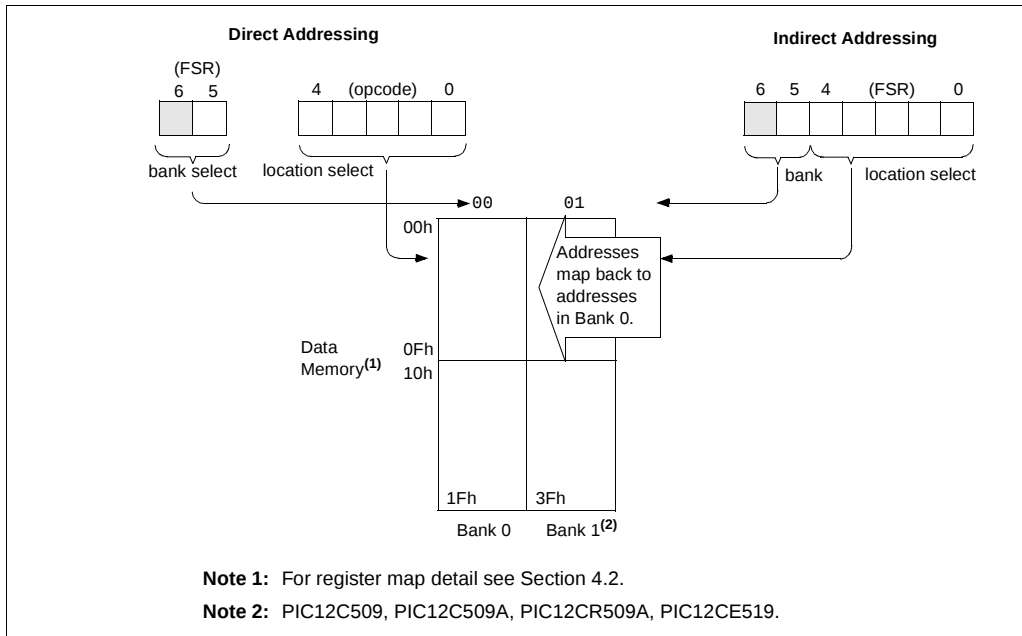
The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

PIC12C508/PIC12C508A/PIC12CE518: Does not use banking. FSR<7:5> are unimplemented and read as '1's.

PIC12C509/PIC12C509A/PIC12CR509A/

PIC12CE519: Uses FSR<5>. Selects between bank 0 and bank 1. FSR<7:6> is unimplemented, read as '1'.

FIGURE 4-9: DIRECT/INDIRECT ADDRESSING



PIC12C5XX

NOTES:

PIC12C5XX

8.7 Time-Out Sequence, Power Down, and Wake-up from SLEEP Status Bits (TO/PD/GPWUF)

The $\overline{\text{TO}}$, $\overline{\text{PD}}$, and GPWUF bits in the STATUS register can be tested to determine if a RESET condition has been caused by a power-up condition, a $\overline{\text{MCLR}}$ or Watchdog Timer (WDT) reset.

TABLE 8-7: $\overline{\text{TO}}/\overline{\text{PD}}/\text{GPWUF}$ STATUS AFTER RESET

GPWUF	$\overline{\text{TO}}$	$\overline{\text{PD}}$	RESET caused by
0	0	0	WDT wake-up from SLEEP
0	0	u	WDT time-out (not from SLEEP)
0	1	0	$\overline{\text{MCLR}}$ wake-up from SLEEP
0	1	1	Power-up
0	u	u	$\overline{\text{MCLR}}$ not during SLEEP
1	1	0	Wake-up from SLEEP on pin change

Legend: u = unchanged

Note 1: The $\overline{\text{TO}}$, $\overline{\text{PD}}$, and GPWUF bits maintain their status (u) until a reset occurs. A low-pulse on the $\overline{\text{MCLR}}$ input does not change the $\overline{\text{TO}}$, $\overline{\text{PD}}$, and GPWUF status bits.

8.8 Reset on Brown-Out

A brown-out is a condition where device power (V_{DD}) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

To reset PIC12C5XX devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 8-13 , Figure 8-14 and Figure 8-15

FIGURE 8-13: BROWN-OUT PROTECTION CIRCUIT 1

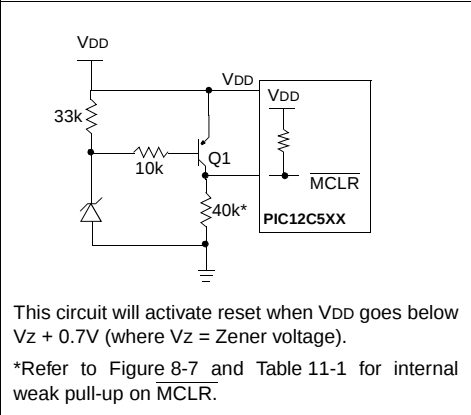


FIGURE 8-14: BROWN-OUT PROTECTION CIRCUIT 2

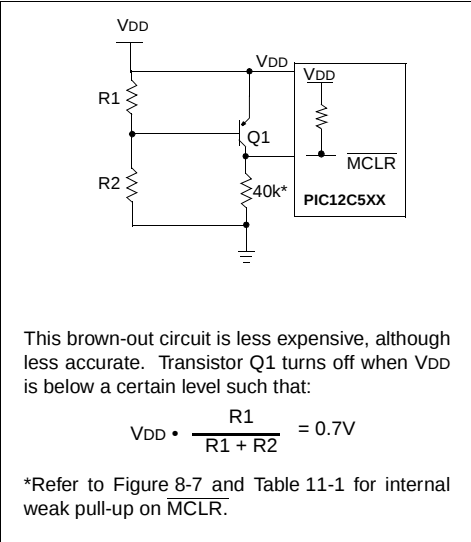
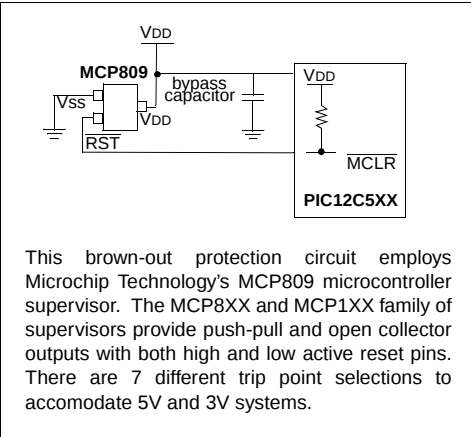


FIGURE 8-15: BROWN-OUT PROTECTION CIRCUIT 3



8.9 Power-Down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

8.9.1 SLEEP

The Power-Down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{TO}$ bit (STATUS<4>) is set, the $\overline{PD}$ bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low, or hi-impedance).

It should be noted that a RESET generated by a WDT time-out does not drive the $\overline{MCLR}$ pin low.

For lowest current consumption while powered down, the $\overline{TOCKI}$ input should be at V_{DD} or V_{SS} and the GP3/ $\overline{MCLR}/V_{PP}$ pin must be at a logic high level (V_{IHMC}) if $\overline{MCLR}$ is enabled.

8.9.2 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

1. An external reset input on GP3/ $\overline{MCLR}/V_{PP}$ pin, when configured as $\overline{MCLR}$.
2. A Watchdog Timer time-out reset (if WDT was enabled).
3. A change on input pin GP0, GP1, or GP3/ $\overline{MCLR}/V_{PP}$ when wake-up on change is enabled.

These events cause a device reset. The $\overline{TO}$, $\overline{PD}$, and GPWUF bits can be used to determine the cause of device reset. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up). The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked. The GPWUF bit indicates a change in state while in SLEEP at pins GP0, GP1, or GP3 (since the last time there was a file or bit operation on GP port).

Caution: Right before entering SLEEP, read the input pins. When in SLEEP, wake up occurs when the values at the pins change from the state they were in at the last reading. If a wake-up on change occurs and the pins are not read before reentering SLEEP, a wake up will occur immediately even if no pins change while in SLEEP mode.

The WDT is cleared when the device wakes from sleep, regardless of the wake-up source.

8.10 Program Verification/Code Protection

If the code protection bit has not been programmed, the on-chip program memory can be read out for verification purposes.

The first 64 locations can be read by the PIC12C5XX regardless of the code protection bit setting.

The last memory location cannot be read if code protection is enabled on the PIC12C508/509.

The last memory location can be read regardless of the code protection bit setting on the PIC12C508A/509A/CR509A/CE518/CE519.

8.11 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '0's.

9.0 INSTRUCTION SET SUMMARY

Each PIC12C5XX instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type, and one or more operands which further specify the operation of the instruction. The PIC12C5XX instruction set summary in Table 9-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 9-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 9-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0 (store result in W) d = 1 (store result in file register 'f') Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
WDT	Watchdog Timer Counter
T $\overline{O}$	Time-Out bit
P $\overline{D}$	Power-Down bit
dest	Destination, either the W register or the specified register file location
[]	Options
()	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
<i>italics</i>	User defined term (font is courier)

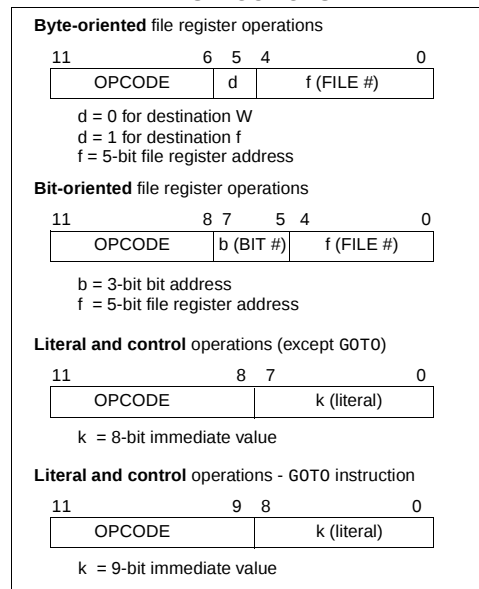
All instructions are executed within a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μ s. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μ s.

Figure 9-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

FIGURE 9-1: GENERAL FORMAT FOR INSTRUCTIONS



SWAPF Swap Nibbles in f

Syntax: `[label] SWAPF f,d`

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f<3:0>) \rightarrow (dest<7:4>);$
 $(f<7:4>) \rightarrow (dest<3:0>)$

Status Affected: None

Encoding:

0011	10df	ffff
------	------	------

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.

Words: 1

Cycles: 1

Example `SWAPF REG1, 0`

Before Instruction
`REG1 = 0xA5`

After Instruction
`REG1 = 0xA5`
`W = 0x5A`

TRIS Load TRIS Register

Syntax: `[label] TRIS f`

Operands: $f = 6$

Operation: $(W) \rightarrow \text{TRIS register } f$

Status Affected: None

Encoding:

0000	0000	0fff
------	------	------

Description: TRIS register 'f' ($f = 6$) is loaded with the contents of the W register

Words: 1

Cycles: 1

Example `TRIS GPIO`

Before Instruction
`W = 0xA5`

After Instruction
`TRIS = 0xA5`

Note: $f = 6$ for PIC12C5XX only.

XORLW Exclusive OR literal with W

Syntax: `[label] XORLW k`

Operands: $0 \leq k \leq 255$

Operation: $(W) .XOR. k \rightarrow (W)$

Status Affected: Z

Encoding:

1111	kkkk	kkkk
------	------	------

Description: The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example: `XORLW 0xAF`

Before Instruction
`W = 0xB5`

After Instruction
`W = 0x1A`

XORWF Exclusive OR W with f

Syntax: `[label] XORWF f,d`

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(W) .XOR. (f) \rightarrow (dest)$

Status Affected: Z

Encoding:

0001	10df	ffff
------	------	------

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example `XORWF REG, 1`

Before Instruction
`REG = 0xAF`
`W = 0xB5`

After Instruction
`REG = 0x1A`
`W = 0xB5`

NOTES:

TABLE 11-4: TIMING REQUIREMENTS - PIC12C508/C509

AC Characteristics		Standard Operating Conditions (unless otherwise specified)				
		Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)				
		Operating Voltage V_{DD} range is described in Section 11.1				
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units
17	TosH2ioV	OSC1 $\uparrow$ (Q1 cycle) to Port out valid ⁽³⁾	—	—	100*	ns
18	TosH2ioI	OSC1 $\uparrow$ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1 $\uparrow$ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time ^(2, 3)	—	10	25**	ns
21	TioF	Port output fall time ^(2, 3)	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in EXTRC mode.

3: See Figure 11-1 for loading conditions.

FIGURE 11-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC12C508/C509

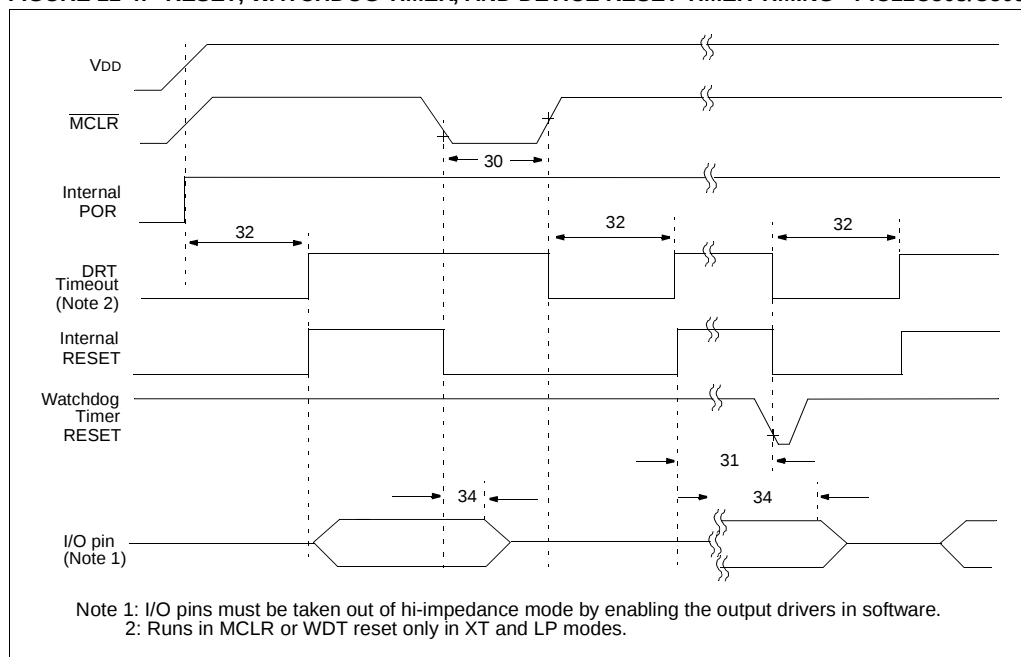


TABLE 11-5: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC12C508/C509

AC Characteristics Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) Operating Voltage V_{DD} range is described in Section 11.1							
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
30	TmCL	MCLR Pulse Width (low)	2000*	—	—	ns	$V_{DD} = 5\text{ V}$
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9*	18*	30*	ms	$V_{DD} = 5\text{ V}$ (Commercial)
32	TDRT	Device Reset Timer Period ⁽²⁾	9*	18*	30*	ms	$V_{DD} = 5\text{ V}$ (Commercial)
34	Tioz	I/O Hi-impedance from MCLR Low	—	—	2000*	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 2: See Table 11-6.

TABLE 11-6: DRT (DEVICE RESET TIMER PERIOD - PIC12C508/C509)

Oscillator Configuration	POR Reset	Subsequent Resets
IntRC & ExtRC	18 ms (typical)	300 μs (typical)
XT & LP	18 ms (typical)	18 ms (typical)

NOTES:

13.1 DC CHARACTERISTICS: PIC12C508A/509A (Commercial, Industrial, Extended) PIC12CE518/519 (Commercial, Industrial, Extended) PIC12CR509A (Commercial, Industrial, Extended)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) −40°C ≤ TA ≤ +85°C (industrial) −40°C ≤ TA ≤ +125°C (extended)					
Parm No.	Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
D001	Supply Voltage	VDD	3.0		5.5	V	Fosc = DC to 4 MHz (Commercial/Industrial, Extended)
D002	RAM Data Retention Voltage ⁽²⁾	VDR		1.5*		V	Device in SLEEP mode
D003	VDD Start Voltage to ensure Power-on Reset	VPOR		VSS		V	See section on Power-on Reset for details
D004	VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See section on Power-on Reset for details
D010	Supply Current ⁽³⁾	IDD	—	0.8	1.4	mA	XT and EXTRC options (Note 4) Fosc = 4 MHz, VDD = 5.5V
D010C			—	0.8	1.4	mA	INTRC Option Fosc = 4 MHz, VDD = 5.5V
D010A			—	19	27	μA	LP OPTION, Commercial Temperature Fosc = 32 kHz, VDD = 3.0V, WDT disabled
			—	19	35	μA	LP OPTION, Industrial Temperature Fosc = 32 kHz, VDD = 3.0V, WDT disabled
			—	30	55	μA	LP OPTION, Extended Temperature Fosc = 32 kHz, VDD = 3.0V, WDT disabled
D020 D021 D021B	Power-Down Current ⁽⁵⁾	IPD	— — —	0.25 0.25 2	4 5 12	μA μA μA	VDD = 3.0V, Commercial WDT disabled VDD = 3.0V, Industrial WDT disabled VDD = 3.0V, Extended WDT disabled
D022	Power-Down Current	ΔIWDT	— — —	2.2 2.2 4	5 6 11	μA μA μA	VDD = 3.0V, Commercial VDD = 3.0V, Industrial VDD = 3.0V, Extended
	Supply Current ⁽³⁾ During read/write to EEPROM peripheral	ΔIEE	—	0.1	0.2	mA	FOSC = 4 MHz, Vdd = 5.5V, SCL = 400kHz

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kOhm.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

PIC12C5XX

FIGURE 13-3: I/O TIMING - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519

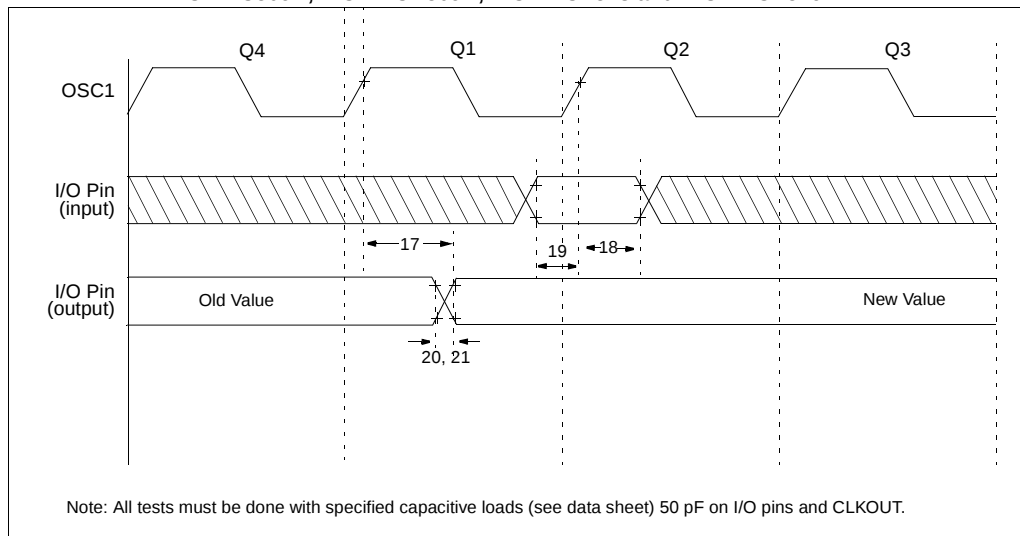


TABLE 13-4: TIMING REQUIREMENTS - PIC12C508A, PIC12C509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519

AC Characteristics		Standard Operating Conditions (unless otherwise specified)				
		Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)				
		Operating Voltage V_{DD} range is described in Section 13.1				
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid ⁽³⁾	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time ^(2, 3)	—	10	25**	ns
21	TioF	Port output fall time ^(2, 3)	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in EXTRC mode.

3: See Figure 13-1 for loading conditions.

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TABLE 14-1: DYNAMIC I_{DD} (TYPICAL) - WDT ENABLED, 25°C

Oscillator	Frequency	V _{DD} = 3.0V	V _{DD} = 5.5V
External RC	4 MHz	240 µA*	800 µA*
Internal RC	4 MHz	320 µA	800 µA
XT	4 MHz	300 µA	800 µA
LP	32 KHz	19 µA	50 µA

*Does not include current through external R&C.

FIGURE 14-3: TYPICAL I_{DD} VS. V_{DD}
(WDT DIS, 25°C, FREQUENCY
= 4MHz)

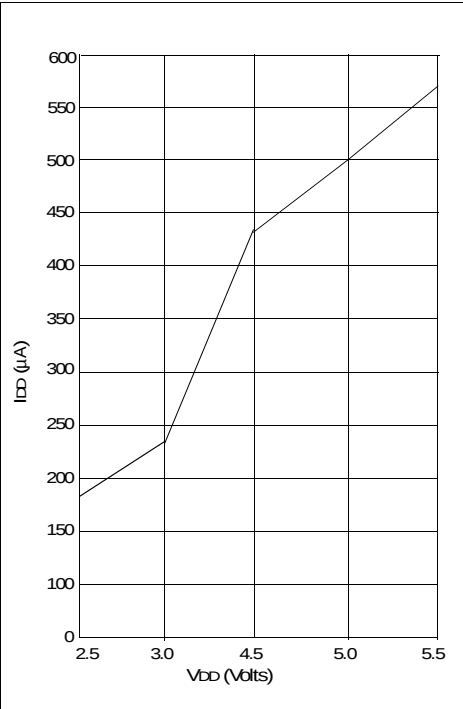


FIGURE 14-4: TYPICAL I_{DD} VS. FREQUENCY
(WDT DIS, 25°C, V_{DD} = 5.5V)

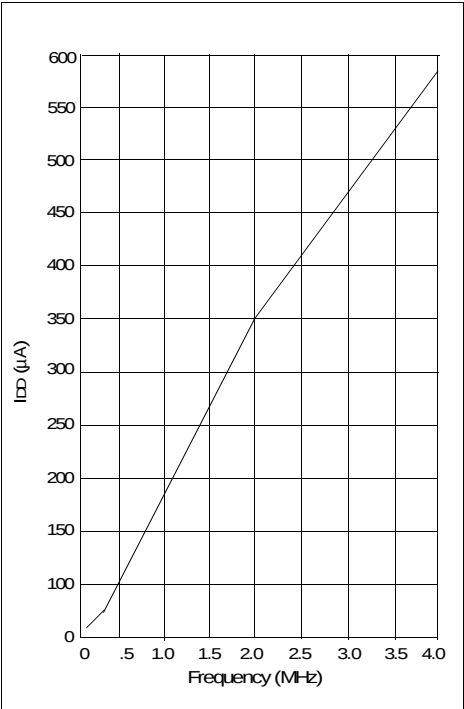


FIGURE 14-9: IOL vs. VOL, VDD = 2.5 V

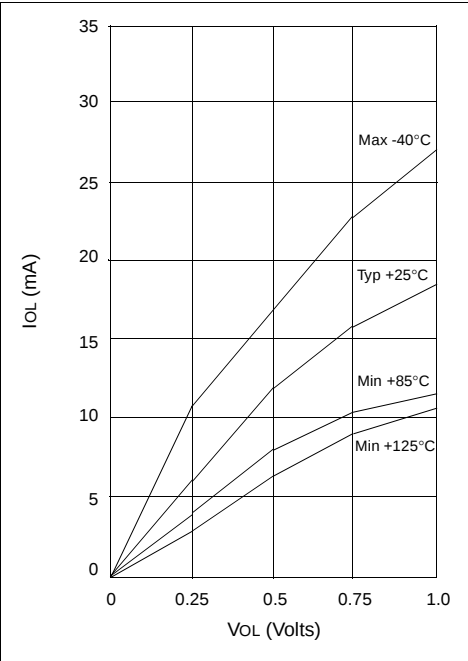


FIGURE 14-11: IOH vs. VOH, VDD = 5.5 V

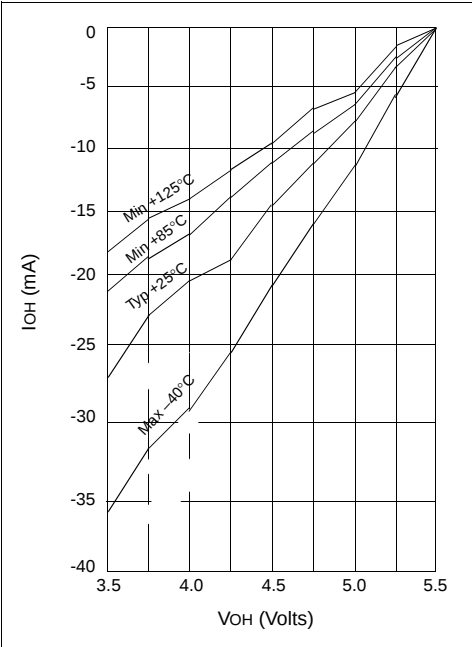


FIGURE 14-10: IOL vs. VOL, VDD = 3.5 V

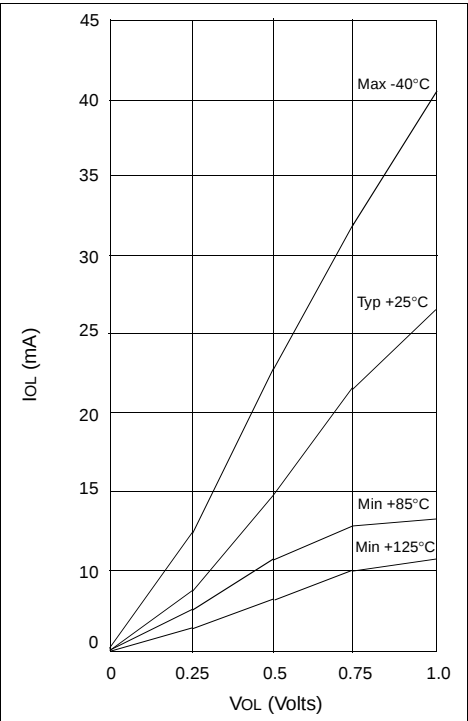


FIGURE 14-12: IOL vs. VOL, VDD = 5.5 V

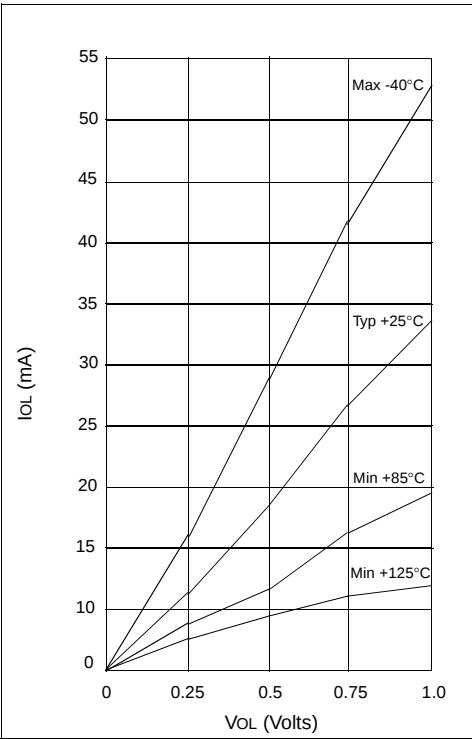
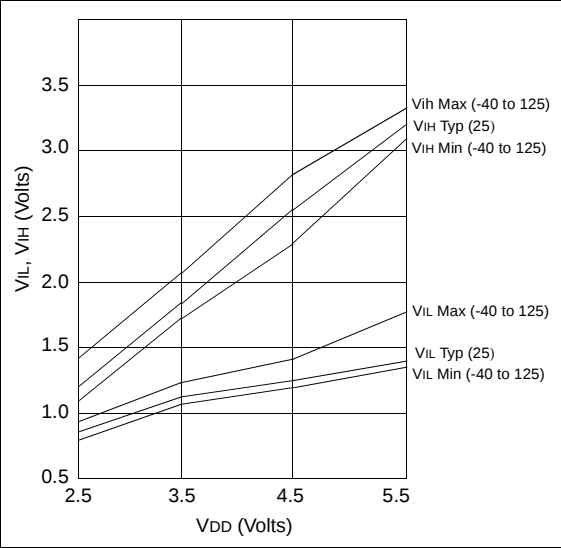


FIGURE 14-15: VIL, VIH OF NMCLR, AND T0CKI VS. VDD



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