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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	41 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.209", 5.30mm Width)
Supplier Device Package	8-SOIJ
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12lc509at-04i-sm

TABLE 1-1: PIC12CXXX & PIC12CEXXX FAMILY OF DEVICES

		PIC12C508(A)	PIC12C509(A)	PIC12CR509A	PIC12CE518	PIC12CE519	PIC12C671	PIC12C672	PIC12CE673	PIC12CE674
Clock	Maximum Frequency of Operation (MHz)	4	4	4	4	4	10	10	10	10
Memory	EPROM Program Memory	512 x 12	1024 x 12	1024 x 12 (ROM)	512 x 12	1024 x 12	1024 x 14	2048 x 14	1024 x 14	2048 x 14
	RAM Data Memory (bytes)	25	41	41	25	41	128	128	128	128
Peripherals	EEPROM Data Memory (bytes)	—	—	—	16	16	—	—	16	16
	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0
	A/D Converter (8-bit) Channels	—	—	—	—	—	4	4	4	4
Features	Wake-up from SLEEP on pin change	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Interrupt Sources	—	—	—	—	—	4	4	4	4
	I/O Pins	5	5	5	5	5	5	5	5	5
	Input Pins	1	1	1	1	1	1	1	1	1
	Internal Pull-ups	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	In-Circuit Serial Programming	Yes	Yes	—	Yes	Yes	Yes	Yes	Yes	Yes
	Number of Instructions	33	33	33	33	33	35	35	35	35
	Packages	8-pin DIP, JW, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, JW	8-pin DIP, JW

All PIC12CXXX & PIC12CEXXX devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

All PIC12CXXX & PIC12CEXXX devices use serial programming with data pin GP0 and clock pin GP1.

4.2 Data Memory Organization

Data memory is composed of registers, or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: special function registers and general purpose registers.

The special function registers include the TMR0 register, the Program Counter (PC), the Status Register, the I/O registers (ports), and the File Select Register (FSR). In addition, special purpose registers are used to control the I/O port configuration and prescaler options.

The general purpose registers are used for data and control information under command of the instructions.

For the PIC12C508, PIC12C508A and PIC12CE518, the register file is composed of 7 special function registers and 25 general purpose registers (Figure 4-2).

For the PIC12C509, PIC12C509A, PIC12CR509A, and PIC12CE519 the register file is composed of 7 special function registers, 25 general purpose registers, and 16 general purpose registers that may be addressed using a banking scheme (Figure 4-3).

4.2.1 GENERAL PURPOSE REGISTER FILE

The general purpose register file is accessed either directly or indirectly through the file select register FSR (Section 4.8).

FIGURE 4-2: PIC12C508, PIC12C508A AND PIC12CE518 REGISTER FILE MAP

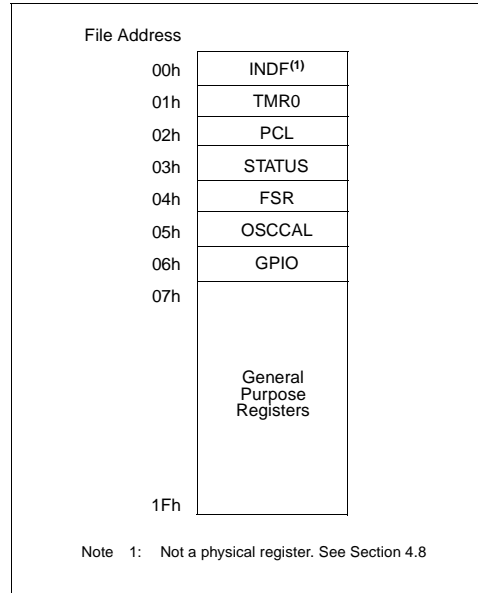
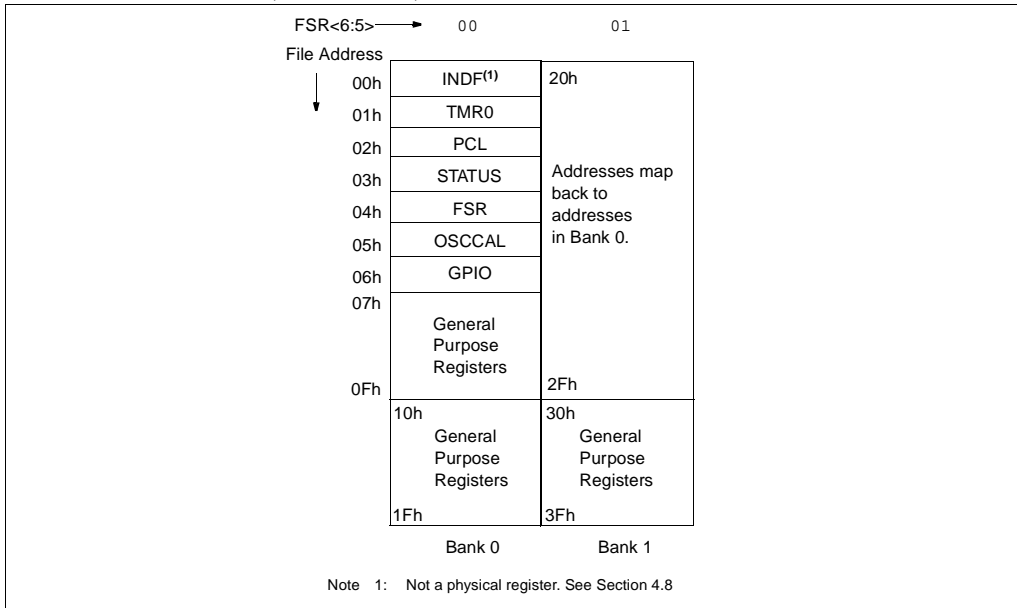


FIGURE 4-3: PIC12C509, PIC12C509A, PIC12CR509A AND PIC12CE519 REGISTER FILE MAP



4.6 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

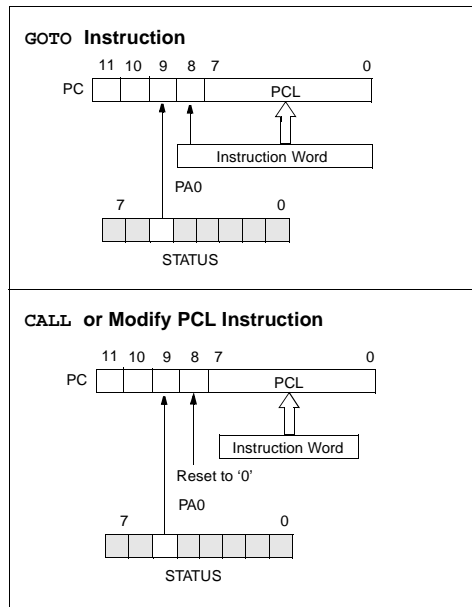
For a GOTO instruction, bits 8:0 of the PC are provided by the GOTO instruction word. The PC Latch (PCL) is mapped to PC<7:0>. Bit 5 of the STATUS register provides page information to bit 9 of the PC (Figure 4-8).

For a CALL instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-8).

Instructions where the PCL is the destination, or Modify PCL instructions, include MOVWF PC, ADDWF PC, and BSF PC, 5.

Note: Because PC<8> is cleared in the CALL instruction, or any Modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-8: LOADING OF PC BRANCH INSTRUCTIONS - PIC12C5XX



4.6.1 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page i.e., the oscillator calibration instruction. After executing MOVLW XX, the PC will roll over to location 00h, and begin executing user code.

The STATUS register page preselect bits are cleared upon a RESET, which means that page 0 is pre-selected.

Therefore, upon a RESET, a GOTO instruction will automatically cause the program to jump to page 0 until the value of the page bits is altered.

4.7 Stack

PIC12C5XX devices have a 12-bit wide L.I.F.O. hardware push/pop stack.

A CALL instruction will *push* the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential CALLs are executed, only the most recent two return addresses are stored.

A RETLW instruction will *pop* the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential RETLW's are executed, the stack will be filled with the address previously stored in level 2. Note that the W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

Upon any reset, the contents of the stack remain unchanged, however the program counter (PCL) will also be reset to 0.

Note 1: There are no STATUS bits to indicate stack overflows or stack underflow conditions.

Note 2: There are no instructions mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL and RETLW instructions.

7.3 WRITE OPERATIONS

7.3.1 BYTE WRITE

Following the start signal from the master, the device code (4 bits), the don't care bits (3 bits), and the R/W bit (which is a logic low) are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer. Only the lower four address bits are used by the device, and the upper four bits are don't cares. The address byte is acknowledgeable and the master device will then transmit the data word to be written into the addressed memory location. The memory acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time will not generate acknowledge signals (Figure 7-7). After a byte write command, the internal address counter will not be incremented and will point to the same address location that was just written. If a stop bit is transmitted to the device at any point in the write command sequence before the entire sequence is complete, then the command will abort and no data will be written. If more than 8 data bits are transmitted before the stop bit is sent, then the device will clear the previously loaded byte and begin loading the data buffer again. If more than one data byte is transmitted to the device and a stop bit is sent before a full eight data bits have been transmitted, then the write command will abort and no data will be written. The EEPROM memory employs a VCC threshold detector circuit which disables the internal erase/write logic if the VCC is below minimum VDD.

Byte write operations must be preceded and immediately followed by a bus not busy bus cycle where both SDA and SCL are held high.

7.4 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/W = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the start bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-6 for flow diagram.

FIGURE 7-6: ACKNOWLEDGE POLLING FLOW

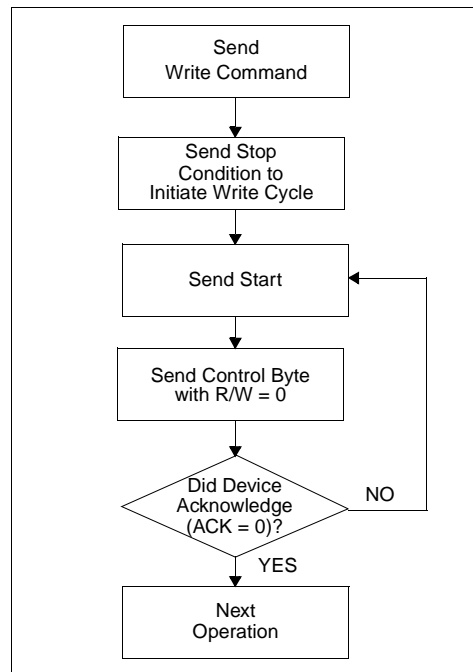
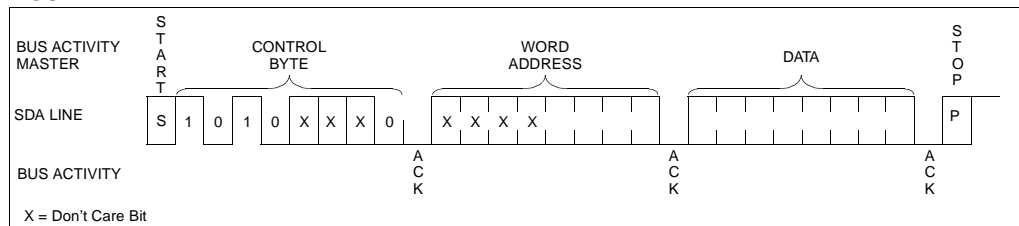


FIGURE 7-7: BYTE WRITE



8.2 Oscillator Configurations

8.2.1 OSCILLATOR TYPES

The PIC12C5XX can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

- LP: Low Power Crystal
- XT: Crystal/Resonator
- INTRC: Internal 4 MHz Oscillator
- EXTRC: External Resistor/Capacitor

8.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT or LP modes, a crystal or ceramic resonator is connected to the GP5/OSC1/CLKIN and GP4/OSC2 pins to establish oscillation (Figure 8-2). The PIC12C5XX oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT or LP modes, the device can have an external clock source drive the GP5/OSC1/CLKIN pin (Figure 8-3).

FIGURE 8-2: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (XT OR LP OSC CONFIGURATION)

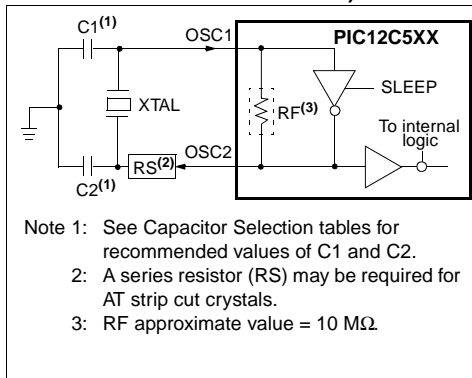


FIGURE 8-3: EXTERNAL CLOCK INPUT OPERATION (XT OR LP OSC CONFIGURATION)

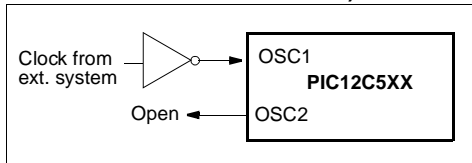


TABLE 8-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS - PIC12C5XX

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
XT	4.0 MHz	30 pF	30 pF

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 8-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - PIC12C5XX

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
LP	32 kHz ⁽¹⁾	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF

Note 1: For VDD > 4.5V, C1 = C2 ≈ 30 pF is recommended.

These values are for design guidance only. Rs may be required to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

TABLE 8-3: RESET CONDITIONS FOR REGISTERS

Register	Address	Power-on Reset	MCLR Reset WDT time-out Wake-up on Pin Change
W (PIC12C508/509)	—	q q q q x x x x ⁽¹⁾	q q q q u u u u ⁽¹⁾
W (PIC12C508A/509A/ PIC12CE518/519/ PIC12CE509A)	—	q q q q q q x x ⁽¹⁾	q q q q q q u u ⁽¹⁾
INDF	00h	x x x x x x x x	u u u u u u u u
TMR0	01h	x x x x x x x x	u u u u u u u u
PC	02h	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
STATUS	03h	0 0 0 1 1 x x x	q 0 0 q q u u u ^(2,3)
FSR (PIC12C508/ PIC12C508A/ PIC12CE518)	04h	1 1 1 x x x x x	1 1 1 u u u u u
FSR (PIC12C509/ PIC12C509A/ PIC12CE519/ PIC12CR509A)	04h	1 1 0 x x x x x	1 1 u u u u u u
OSCCAL (PIC12C508/509)	05h	0 1 1 1 - - - -	u u u u - - - -
OSCCAL (PIC12C508A/509A/ PIC12CE518/512/ PIC12CR509A)	05h	1 0 0 0 0 0 - -	u u u u u u - -
GPIO (PIC12C508/PIC12C509/ PIC12C508A/ PIC12C509A/ PIC12CR509A)	06h	- - x x x x x x	- - u u u u u u
GPIO (PIC12CE518/ PIC12CE519)	06h	1 1 x x x x x x	1 1 u u u u u u
OPTION	—	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
TRIS	—	- - 1 1 1 1 1 1	- - 1 1 1 1 1 1

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition.

Note 1: Bits <7:2> of W register contain oscillator calibration values due to MOV LW XX instruction at top of memory.

Note 2: See Table 8-7 for reset value for specific conditions

Note 3: If reset was due to wake-up on pin change, then bit 7 = 1. All other resets will cause bit 7 = 0.

TABLE 8-4: RESET CONDITION FOR SPECIAL REGISTERS

	STATUS Addr: 03h	PCL Addr: 02h
Power on reset	0 0 0 1 1 x x x	1 1 1 1 1 1 1 1
MCLR reset during normal operation	0 0 0 u u u u u	1 1 1 1 1 1 1 1
MCLR reset during SLEEP	0 0 0 1 0 u u u	1 1 1 1 1 1 1 1
WDT reset during SLEEP	0 0 0 0 0 u u u	1 1 1 1 1 1 1 1
WDT reset normal operation	0 0 0 0 u u u u	1 1 1 1 1 1 1 1
Wake-up from SLEEP on pin change	1 0 0 1 0 u u u	1 1 1 1 1 1 1 1

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0'.

MOVF Move f

Syntax: [*label*] MOVF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f) \rightarrow (dest)$

Status Affected: Z

Encoding:

0010	00df	ffff
------	------	------

Description: The contents of register 'f' is moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' is 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example: MOVF FSR, 0

After Instruction
W = value in FSR register

MOVLW Move Literal to W

Syntax: [*label*] MOVLW k

Operands: $0 \leq k \leq 255$

Operation: $k \rightarrow (W)$

Status Affected: None

Encoding:

1100	kkkk	kkkk
------	------	------

Description: The eight bit literal 'k' is loaded into the W register. The don't cares will assemble as 0s.

Words: 1

Cycles: 1

Example: MOVLW 0x5A

After Instruction
W = 0x5A

MOVWF Move W to f

Syntax: [*label*] MOVWF f

Operands: $0 \leq f \leq 31$

Operation: $(W) \rightarrow (f)$

Status Affected: None

Encoding:

0000	001f	ffff
------	------	------

Description: Move data from the W register to register 'f'.

Words: 1

Cycles: 1

Example: MOVWF TEMP_REG

Before Instruction
TEMP_REG = 0xFF
W = 0x4F

After Instruction
TEMP_REG = 0x4F
W = 0x4F

NOP No Operation

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Encoding:

0000	0000	0000
------	------	------

Description: No operation.

Words: 1

Cycles: 1

Example: NOP

10.0 DEVELOPMENT SUPPORT

10.1 Development Tools

The PICmicro[®] microcontrollers are supported with a full range of hardware and software development tools:

- MPLAB[™]-ICE Real-Time In-Circuit Emulator
- ICEPIC[™] Low-Cost PIC16C5X and PIC16CXXX In-Circuit Emulator
- PRO MATE[®] II Universal Programmer
- PICSTART[®] Plus Entry-Level Prototype Programmer
- SIMICE
- PICDEM-1 Low-Cost Demonstration Board
- PICDEM-2 Low-Cost Demonstration Board
- PICDEM-3 Low-Cost Demonstration Board
- MPASM Assembler
- MPLAB[™] SIM Software Simulator
- MPLAB-C17 (C Compiler)
- Fuzzy Logic Development System (fuzzyTECH[®]-MP)
- KEELQ[®] Evaluation Kits and Programmer

10.2 MPLAB-ICE: High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB-ICE Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro[®] microcontrollers (MCUs). MPLAB-ICE is supplied with the MPLAB Integrated Development Environment (IDE), which allows editing, "make" and download, and source debugging from a single environment.

Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB-ICE allows expansion to support all new Microchip microcontrollers.

The MPLAB-ICE Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC compatible 386 (and higher) machine platform and Microsoft Windows[®] 3.x or Windows 95 environment were chosen to best make these features available to you, the end user.

MPLAB-ICE is available in two versions. MPLAB-ICE 1000 is a basic, low-cost emulator system with simple trace capabilities. It shares processor modules with the MPLAB-ICE 2000. This is a full-featured emulator system with enhanced trace, trigger, and data monitoring features. Both systems will operate across the entire operating speed range of the PICmicro[®] MCU.

10.3 ICEPIC: Low-Cost PICmicro[®] In-Circuit Emulator

ICEPIC is a low-cost in-circuit emulator solution for the Microchip PIC12CXXX, PIC16C5X and PIC16CXXX families of 8-bit OTP microcontrollers.

ICEPIC is designed to operate on PC-compatible machines ranging from 386 through Pentium[™] based machines under Windows 3.x, Windows 95, or Windows NT environment. ICEPIC features real time, non-intrusive emulation.

10.4 PRO MATE II: Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode. PRO MATE II is CE compliant.

The PRO MATE II has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode the PRO MATE II can read, verify or program PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices. It can also set configuration and code-protect bits in this mode.

10.5 PICSTART Plus Entry Level Development System

The PICSTART programmer is an easy-to-use, low-cost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. PICSTART Plus is not recommended for production programming.

PICSTART Plus supports all PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices with up to 40 pins. Larger pin count devices such as the PIC16C923, PIC16C924 and PIC17C756 may be supported with an adapter socket. PICSTART Plus is CE compliant.

10.10 MPLAB Integrated Development Environment Software

The MPLAB IDE Software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a windows based application which contains:

- A full featured editor
- Three operating modes
 - editor
 - emulator
 - simulator
- A project manager
- Customizable tool bar and key mapping
- A status bar with project information
- Extensive on-line help

MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PICmicro[®] tools (automatically updates all project information)
- Debug using:
 - source files
 - absolute listing file

The ability to use MPLAB with Microchip's simulator allows a consistent platform and the ability to easily switch from the low cost simulator to the full featured emulator with minimal retraining due to development tools.

10.11 Assembler (MPASM)

The MPASM Universal Macro Assembler is a PC-hosted symbolic assembler. It supports all microcontroller series including the PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX, and PIC17CXX families.

MPASM offers full featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from MPLAB-ICE, Microchip's Universal Emulator System.

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro assembly capability.
- Produces all the files (Object, Listing, Symbol, and special) required for symbolic debug with Microchip's emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a rich directive language to support programming of the PICmicro[®]. Directives are helpful in making the development of your assemble source code shorter and more maintainable.

10.12 Software Simulator (MPLAB-SIM)

The MPLAB-SIM Software Simulator allows code development in a PC host environment. It allows the user to simulate the PICmicro[®] series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in; single step, execute until break, or in a trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C17 and MPASM. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

10.13 MPLAB-C17 Compiler

The MPLAB-C17 Code Development System is a complete ANSI 'C' compiler and integrated development environment for Microchip's PIC17CXXX family of microcontrollers. The compiler provides powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compiler provides symbol information that is compatible with the MPLAB IDE memory display.

10.14 Fuzzy Logic Development System (fuzzyTECH-MP)

fuzzyTECH-MP fuzzy logic development tool is available in two versions - a low cost introductory version, MP Explorer, for designers to gain a comprehensive working knowledge of fuzzy logic system design; and a full-featured version, *fuzzyTECH-MP*, Edition for implementing more complex systems.

Both versions include Microchip's *fuzzyLAB*[™] demonstration board for hands-on experience with fuzzy logic systems implementation.

10.15 SEEVAL[®] Evaluation and Programming System

The SEEVAL SEEPRO Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPRO product including Smart Serials[™] and secure serials. The Total Endurance[™] Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

11.2 DC CHARACTERISTICS: PIC12C508/509 (Commercial, Industrial, Extended)

Standard Operating Conditions (unless otherwise specified) Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) Operating voltage V_{DD} range as described in DC spec Section 11.1 and Section 11.2.							
DC CHARACTERISTICS							
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D030	Input Low Voltage I/O ports with TTL buffer	V_{IL}	V_{SS}	-	0.8V	V	$4.5 < V_{DD} \leq 5.5\text{V}$ otherwise Note1
D031	with Schmitt Trigger buffer		V_{SS}	-	0.15V _{DD}	V	
D032	$\overline{\text{MCLR}}$, GP2/T0CKI (in EXTRC mode)		V_{SS}	-	0.15V _{DD}	V	
D033	OSC1 (EXTRC) ⁽¹⁾		V_{SS}	-	0.15V _{DD}	V	
D033	OSC1 (in XT and LP)		V_{SS}	-	0.3V _{DD}	V	
D040	Input High Voltage I/O ports with TTL buffer	V_{IH} V_{SS}	2.0V	-	V _{DD}	V	$4.5 \leq V_{DD} \leq 5.5\text{V}$ otherwise For entire V _{DD} range Note1
D040A			0.25V _{DD} + 0.8V	-	V _{DD}	V	
D041	with Schmitt Trigger buffer		0.85V _{DD}	-	V _{DD}	V	
D042	$\overline{\text{MCLR}}$ /GP2/T0CKI		0.85V _{DD}	-	V _{DD}	V	
D042A	OSC1 (XT and LP)		0.7V _{DD}	-	V _{DD}	V	
D043	OSC1 (in EXTRC mode)		0.85V _{DD}	-	V _{DD}	V	
D070	GPIO weak pull-up current	IPUR	50	250	400	μA	V _{DD} = 5V, V _{PIN} = V _{SS}
D060	Input Leakage Current ^(2, 3) I/O ports	I _{IL}	-1	0.5	±1	μA	For V _{DD} ≤ 5.5V V _{SS} ≤ V _{PIN} ≤ V _{DD} , Pin at hi-impedance
D061	$\overline{\text{MCLR}}$, GP2/T0CKI		20	130	250	μA	V _{PIN} = V _{SS} + 0.25V ⁽²⁾
D063	OSC1		-3	0.5	+3	μA	V _{PIN} = V _{DD} V _{SS} ≤ V _{PIN} ≤ V _{DD} , XT and LP options
D080	Output Low Voltage I/O ports/CLKOUT	V _{OL}	-	-	0.6	V	I _{OL} = 8.7 mA, V _{DD} = 4.5V
D090	Output High Voltage I/O ports/CLKOUT ⁽³⁾	V _{OH}	V _{DD} - 0.7	-	-	V	I _{OH} = -5.4 mA, V _{DD} = 4.5V
D100	Capacitive Loading Specs on Output Pins OSC2 pin	C _{OSC2}	-	-	15	pF	In XT and LP modes when external clock is used to drive OSC1.
D101	All I/O pins	C _{IO}	-	-	50	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C5XX be driven with external clock in RC mode.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

11.4 Timing Diagrams and Specifications

FIGURE 11-2: EXTERNAL CLOCK TIMING - PIC12C508/C509

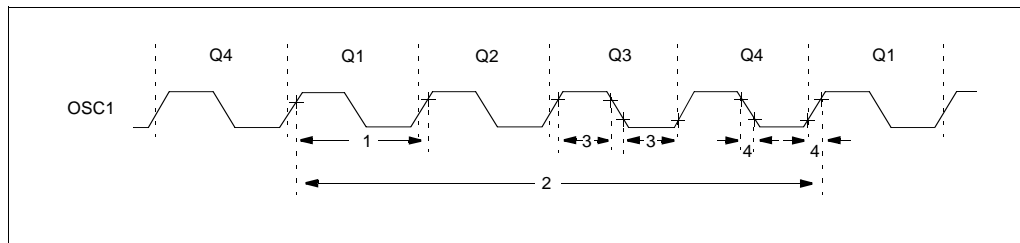


TABLE 11-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC12C508/C509

AC Characteristics		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), 					

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (Tcy) equals four times the input oscillator time base period.

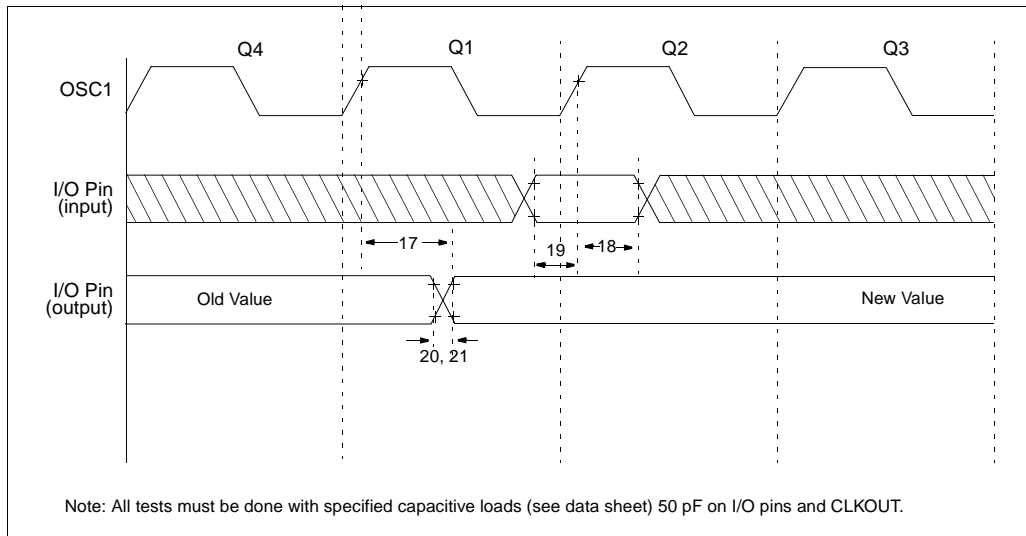
TABLE 11-3: CALIBRATED INTERNAL RC FREQUENCIES - PIC12C508/C509

AC Characteristics		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial), $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial), $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)					
		Operating Voltage V_{DD} range is described in Section 10.1					
Parameter No.	Sym	Characteristic	Min*	Typ ⁽¹⁾	Max*	Units	Conditions
		Internal Calibrated RC Frequency	3.58	4.00	4.32	MHz	$V_{DD} = 5.0\text{V}$
		Internal Calibrated RC Frequency	3.50	—	4.26	MHz	$V_{DD} = 2.5\text{V}$

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 11-3: I/O TIMING - PIC12C508/C509



NOTES:

13.1 DC CHARACTERISTICS: PIC12C508A/509A (Commercial, Industrial, Extended) PIC12CE518/519 (Commercial, Industrial, Extended) PIC12CR509A (Commercial, Industrial, Extended)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended)					
Parm No.	Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
D001	Supply Voltage	VDD	3.0		5.5	V	FOSC = DC to 4 MHz (Commercial/Industrial, Extended)
D002	RAM Data Retention Voltage ⁽²⁾	VDR		1.5*		V	Device in SLEEP mode
D003	VDD Start Voltage to ensure Power-on Reset	VPOR		VSS		V	See section on Power-on Reset for details
D004	VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See section on Power-on Reset for details
D010	Supply Current ⁽³⁾	IDD	—	0.8	1.4	mA	XT and EXTRC options (Note 4) FOSC = 4 MHz, VDD = 5.5V
D010C			—	0.8	1.4	mA	INTRC Option FOSC = 4 MHz, VDD = 5.5V
D010A			—	19	27	μA	LP OPTION, Commercial Temperature FOSC = 32 kHz, VDD = 3.0V, WDT disabled
			—	19	35	μA	LP OPTION, Industrial Temperature FOSC = 32 kHz, VDD = 3.0V, WDT disabled
			—	30	55	μA	LP OPTION, Extended Temperature FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D020	Power-Down Current ⁽⁵⁾	IPD	—	0.25	4	μA	VDD = 3.0V, Commercial WDT disabled
D021			—	0.25	5	μA	VDD = 3.0V, Industrial WDT disabled
D021B			—	2	12	μA	VDD = 3.0V, Extended WDT disabled
D022	Power-Down Current	ΔIWDT	—	2.2	5	μA	VDD = 3.0V, Commercial
			—	2.2	6	μA	VDD = 3.0V, Industrial
			—	4	11	μA	VDD = 3.0V, Extended
	Supply Current ⁽³⁾ During read/write to EEPROM peripheral	ΔIEE	—	0.1	0.2	mA	FOSC = 4 MHz, Vdd = 5.5V, SCL = 400kHz

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
- 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
- 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kOhm.
- 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

PIC12C5XX

TABLE 13-1: PULL-UP RESISTOR RANGES* - PIC12C508A, PIC12C509A, PIC12CR509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519

V _{DD} (Volts)	Temperature (°C)	Min	Typ	Max	Units
GP0/GP1					
2.5	–40	38K	42K	63K	Ω
	25	42K	48K	63K	Ω
	85	42K	49K	63K	Ω
	125	50K	55K	63K	Ω
5.5	–40	15K	17K	20K	Ω
	25	18K	20K	23K	Ω
	85	19K	22K	25K	Ω
	125	22K	24K	28K	Ω
GP3					
2.5	–40	285K	346K	417K	Ω
	25	343K	414K	532K	Ω
	85	368K	457K	532K	Ω
	125	431K	504K	593K	Ω
5.5	–40	247K	292K	360K	Ω
	25	288K	341K	437K	Ω
	85	306K	371K	448K	Ω
	125	351K	407K	500K	Ω

* These parameters are characterized but not tested.

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PIC12C5XX Product Identification System

PART NO.	-XX	X	/XX	XXX			Examples
					Pattern:	Special Requirements	a) PIC12C508A-04/P Commercial Temp., PDIP Package, 4 MHz, normal VDD limits
					Package:	SN = 150 mil SOIC SM = 208 mil SOIC P = 300 mil PDIP JW = 300 mil Windowed Ceramic Side Brazed	b) PIC12C508A-04I/SM Industrial Temp., SOIC package, 4 MHz, normal VDD limits
					Temperature Range:	- = 0°C to +70°C I = -40°C to +85°C E = -40°C to +125°C	c) PIC12C509-04I/P Industrial Temp., PDIP package, 4 MHz, normal VDD limits
					Frequency Range:	04 = 4 MHz	
					Device	PIC12C508 PIC12C509 PIC12C508T (Tape & reel for SOIC only) PIC12C509T (Tape & reel for SOIC only) PIC12C508A PIC12C509A PIC12C508AT (Tape & reel for SOIC only) PIC12C509AT (Tape & reel for SOIC only) PIC12LC508A PIC12LC509A PIC12LC508AT (Tape & reel for SOIC only) PIC12LC509AT (Tape & reel for SOIC only) PIC12CR509A PIC12CR509AT (Tape & reel for SOIC only) PIC12LCR509A PIC12LCR509AT (Tape & reel for SOIC only) PIC12CE518 PIC12CE518T (Tape & reel for SOIC only) PIC12CE519 PIC12CE519T (Tape & reel for SOIC only) PIC12LCE518 PIC12LCE518T (Tape & reel for SOIC only) PIC12LCE519 PIC12LCE519T (Tape & reel for SOIC only)	

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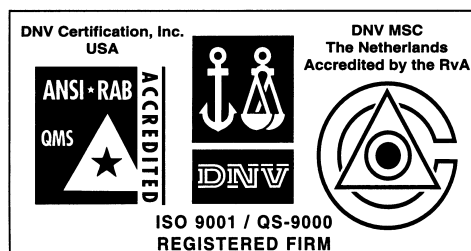
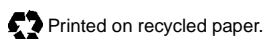
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