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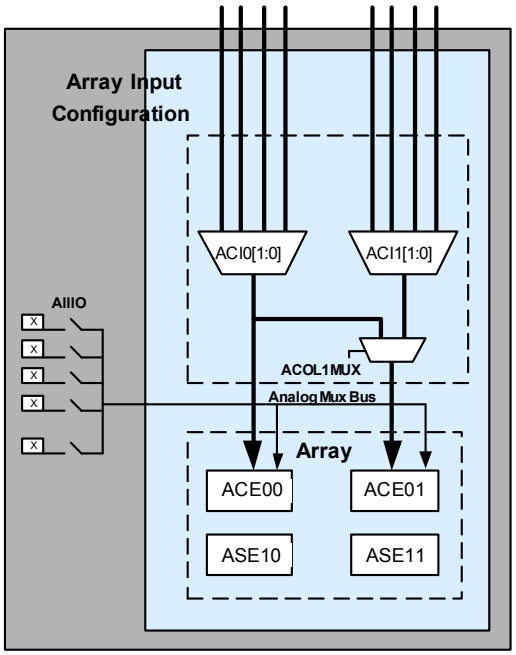
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	12MHz
Connectivity	I²C, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c60323-ltxc

Figure 2. Analog System Block Diagram



The Analog Multiplexer System

The analog mux bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters (ADC). An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Additional System Resources

System resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a switch mode pump, low voltage detection, and power on reset. Brief statements describing the merits of each system resource follow.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks may be generated using digital blocks as clock dividers.
- The I^2C module provides 100 kHz and 400 kHz communication over two wires. slave, master, and multi-master modes are all supported.
- Low voltage detection interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- An internal 1.3-V voltage reference provides an absolute reference for the analog system.
- An integrated switch mode pump generates normal operating voltages from a single 1.2 V battery cell, providing a low-cost boost converter.
- Versatile analog multiplexer system.

enCoRe III LV Device Characteristics

The enCoRe III LV devices have four digital blocks and four analog blocks. Table 1 lists the resources available for specific enCoRe III LV devices.

Table 1. enCoRe III LV Device Characteristics

Part Number	Digital IO	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY7C60323-PVXC	24	1	4	24	0	2	4	512 Bytes	8K

Getting Started

The quickest path to understanding the enCoRe III LV silicon is by reading this data sheet and using the PSoC Designer integrated development environment (IDE). This data sheet is an overview of the enCoRe III LV and presents specific pin, register, and electrical specifications. enCoRe III LV is based on the architecture of the CY8C21x34. For in-depth information, along with detailed programming information, refer to the PSoC Programmable System-on-Chip Technical Reference Manual, which is available at http://www.cypress.com.

For up-to-date ordering, packaging, and electrical specification information, refer to the latest device data sheets on the web at http://www.cypress.com.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select user modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Pin Information

The enCoRe III LV device is available in 28-pin SSOP and 32-pin QFN packages. Every port pin (labeled with a “P”) is capable of Digital IO and connection to the common analog bus. However, Vss, V_{DD}, SMP, and XRES are not capable of Digital IO.

28-pin Part Pinout

Figure 3. CY7C60323-PVXC 28-pin Device

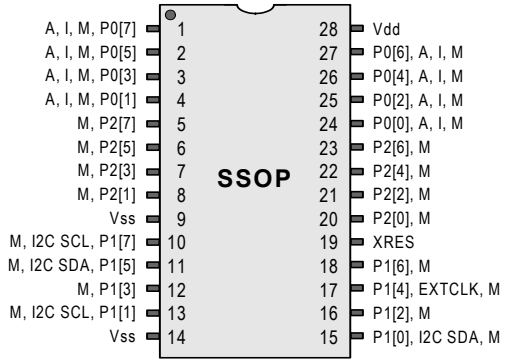


Table 2. Pin Definitions - CY7C60323-PVXC 28-pin Device

Pin No.	Type		Name	Description
	Digital	Analog		
1	IO	I, M	P0[7]	Analog column mux input.
2	IO	I, M	P0[5]	Analog column mux input and column output.
3	IO	I, M	P0[3]	Analog column mux input and column output, integrating input.
4	IO	I, M	P0[1]	Analog column mux input, integrating input.
5	IO	M	P2[7]	
6	IO	M	P2[5]	
7	IO	I, M	P2[3]	Direct switched capacitor block input.
8	IO	I, M	P2[1]	Direct switched capacitor block input.
9	Power		Vss	Ground connection.
10	IO	M	P1[7]	I^2C serial clock (SCL).
11	IO	M	P1[5]	I^2C serial data (SDA).
12	IO	M	P1[3]	
13	IO	M	P1[1]	I^2C SCL, ISSP-SCLK.
14	Power		Vss	Ground connection.
15	IO	M	P1[0]	I^2C SDA, ISSP-SDATA.
16	IO	M	P1[2]	
17	IO	M	P1[4]	Optional external clock input (EXTCLK).
18	IO	M	P1[6]	
19	Input		XRES	Active HIGH external reset with internal pull down.
20	IO	I, M	P2[0]	Direct switched capacitor block input.
21	IO	I, M	P2[2]	Direct switched capacitor block input.
22	IO	M	P2[4]	
23	IO	M	P2[6]	
24	IO	I, M	P0[0]	Analog column mux input
25	IO	I, M	P0[2]	Analog column mux input
26	IO	I, M	P0[4]	Analog column mux input
27	IO	I, M	P0[6]	Analog column mux input
28	Power		V_{DD}	Supply voltage.

LEGEND A = analog, I = input, O = output, and M = analog mux input.

32-pin Part Pinout

Figure 4. CY7C60323-LFXC 32-pin Device

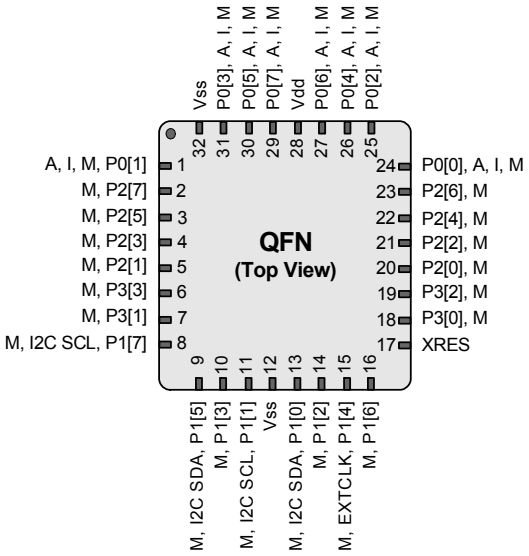
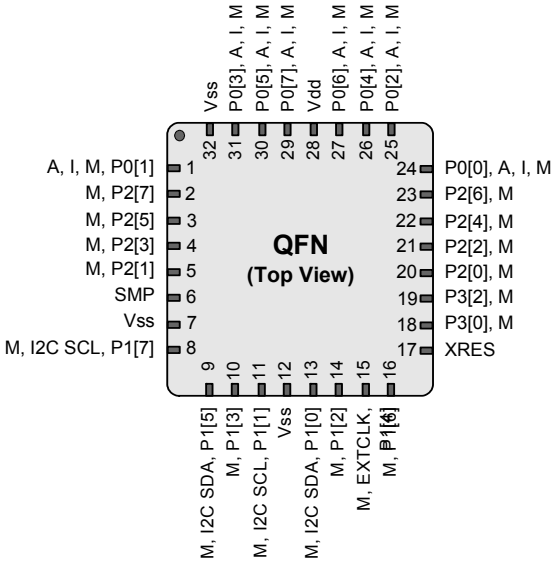


Figure 5. CY7C60333-LFXC 32-pin Device



Register Reference

This section lists the registers of the enCoRe III LV device. For detailed register information, refer the PSoC System-on-Chip Technical Reference Manual.

Register Conventions

The register conventions specific to this section are listed in Table 4.

Table 4. Register Conventions

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The enCoRe III LV device has a total register address space of 512 bytes. The register space is referred to as IO space and is divided into two banks, Bank 0 and Bank 1. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set to 1 the user is in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and must not be accessed.

Table 5. Register Map 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASE10CR0	80	RW		C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASE11CR0	84	RW		C4	
PRT1IE	05	RW		45			85			C5	
PRT1GS	06	RW		46			86			C6	
PRT1DM2	07	RW		47			87			C7	
PRT2DR	08	RW		48			88			C8	
PRT2IE	09	RW		49			89			C9	
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	
PRT3DR	0C	RW		4C			8C			CC	
PRT3IE	0D	RW		4D			8D			CD	
PRT3GS	0E	RW		4E			8E			CE	
PRT3DM2	0F	RW		4F			8F			CF	
	10			50			90		CUR_PP	D0	RW
	11			51			91		STK_PP	D1	RW
	12			52			92			D2	
	13			53			93		IDX_PP	D3	RW
	14			54			94		MVR_PP	D4	RW
	15			55			95		MVW_PP	D5	RW
	16			56			96		I2C_CFG	D6	RW
	17			57			97		I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 5. Register Map 0 Table: User Space *(continued)*

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W	AMUXCFG	61	RW		A1		INT_MSK1	E1	RW
DBB00DR2	22	RW	PWM_CR	62	RW		A2		INT_VC	E2	RC
DBB00CR0	23	#		63			A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4			E4	
DBB01DR1	25	W		65			A5			E5	
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#	ADC0_CR	68	#		A8			E8	
DCB02DR1	29	W	ADC1_CR	69	#		A9			E9	
DCB02DR2	2A	RW		6A			AA			EA	
DCB02CR0	2B	#		6B			AB			EB	
DCB03DR0	2C	#	TMP_DR0	6C	RW		AC			EC	
DCB03DR1	2D	W	TMP_DR1	6D	RW		AD			ED	
DCB03DR2	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCB03CR0	2F	#	TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_D	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 6. Register Map 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASE10CR0	80	RW		C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASE11CR0	84	RW		C4	
PRT1DM1	05	RW		45			85			C5	
PRT1IC0	06	RW		46			86			C6	
PRT1IC1	07	RW		47			87			C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
	10			50			90		GDI_O_IN	D0	RW
	11			51			91		GDI_E_IN	D1	RW
	12			52			92		GDI_O_OU	D2	RW
	13			53			93		GDI_E_OU	D3	RW
	14			54			94			D4	
	15			55			95			D5	
	16			56			96			D6	
	17			57			97			D7	
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A			9A		MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5		ADC0_TR	E5	RW
DBB01OU	26	RW	AMD_CR1	66	RW		A6		ADC1_TR	E6	RW
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B		CLK_CR3	6B	RW		AB		ECO_TR	EB	W

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 6. Register Map 1 Table: Configuration Space *(continued)*

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA		FLS_PR1	FA	RW
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_CR	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the enCoRe III LV device. For up-to-date electrical specifications, check the latest data sheet by visiting the web at http://www.cypress.com.

Specifications are valid for 0 °C ≤ T_A ≤ 70 °C and T_J ≤ 85 °C as specified, except where noted.

Refer to Table 19 on page 22 for the electrical specifications for the internal main oscillator (IMO) using SLIMO mode.

Figure 10. Voltage versus CPU Frequency

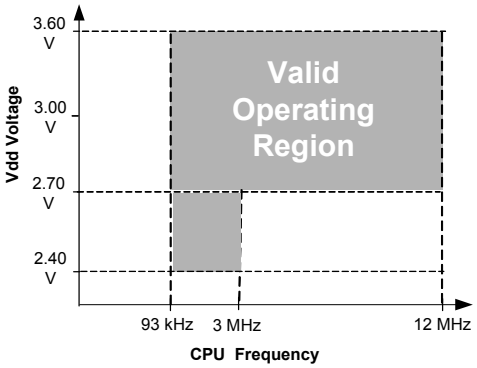
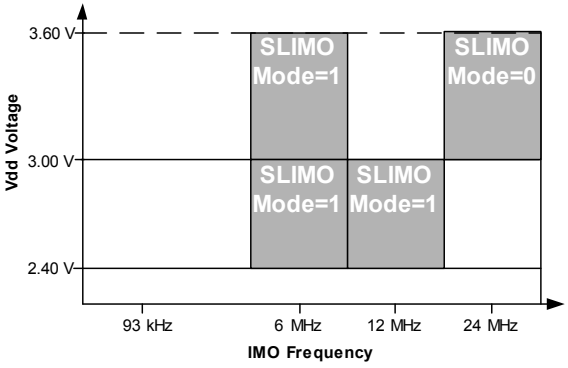
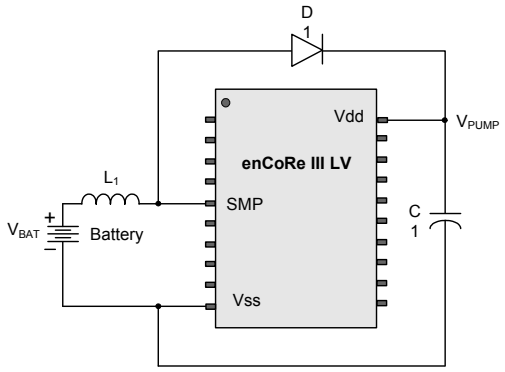


Figure 11. IMO Frequency Trim Options



The allowable CPU operating region for 12 MHz has been extended down to 2.7 V from the original 3.0 V design target. The customer's application is responsible for monitoring voltage and throttling back CPU speed in accordance with Figure 10 when voltage approaches 2.7 V. Refer to Table 16 for LVD specifications. Note that the device does not support a preset trip at 2.7 V. To detect V_{DD} drop at 2.7 V, an external circuit or device such as the WirelessUSB LP - CYRF6936 must be employed; or if the design permits, the nearest LVD trip value at 2.9 V can be used.

Figure 12. Basic Switch Mode Pump Circuit



DC Analog Mux Bus Specifications

Table 15 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ T_A ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70° C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 15. DC Analog Mux Bus Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{SW}	Switch resistance to common analog bus	–	–	400 800	Ω Ω	V_{DD} ≥ 2.7 V 2.4 V ≤ V_{DD} ≤ 2.7 V
R_{VDD}	Resistance of initialization switch to V_{DD}	–	–	800	Ω	

DC POR and LVD Specifications

Table 16 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ T_A ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 16. DC POR and LVD Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{PPOR0} V_{PPOR1}	V_{DD} value for PPOR Trip PORLEV[1:0] = 00b PORLEV[1:0] = 01b	 –	 2.36 2.82	 2.40 2.95	 V V	V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from Watchdog.
	V_{DD} value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b	2.40	2.45	2.51[3]	V	
V_{LVD1}	VM[2:0] = 001b	2.85	2.92	2.99[4]	V	
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD37}	VM[2:0] = 011b	3.06	3.13	3.20	V	
	V_{DD} value for PUMP Trip					
V_{PUMP0}	VM[2:0] = 000b	2.45	2.55	2.62[5]	V	
V_{PUMP1}	VM[2:0] = 001b	2.96	3.02	3.09	V	
V_{PUMP2}	VM[2:0] = 010b	3.03	3.10	3.16	V	
V_{PUMP3}	VM[2:0] = 011b	3.18	3.25	3.32[6]	V	

Notes
3. Always greater than 50 mV above VPPOR (PORLEV = 00) for falling supply.
4. Always greater than 50 mV above VPPOR (PORLEV = 01) for falling supply.
5. Always greater than 50 mV above VLVD0.
6. Always greater than 50 mV above VLVD3.

DC Programming Specifications

Table 17 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ T_A ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 17. DC Programming Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5.0	5.5	V	This specification applies to the functional requirements of external programmer tools.
V_{DDLV}	Low V_{DD} for verify	2.4	2.5	2.6	V	This specification applies to the functional requirements of external programmer tools.
V_{DDHV}	High V_{DD} for verify	3.5	3.6	3.7	V	This specification applies to the functional requirements of external programmer tools.
$V_{DDIWRITE}$	Supply voltage for flash write operation	2.7	–	3.6	V	This specification applies to this device when it is executing internal flash writes.
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.1	–	–	V	
I_{ILP}	Input current when applying Vilp to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input current when applying Vihp to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	Vss + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)	50,000[7]	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash dndurance (total)[8]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	10	–	–	Years	

DC I^2C Specifications

Table 18 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ T_A ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 18. DC I^2C Specifications[9]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	2.4 V ≤ V_{DD} ≤ 3.6 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	2.4 V ≤ V_{DD} ≤ 3.6 V

Notes
7. The 50,000 cycle Flash endurance per block will only be guaranteed if the Flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V and 3.0 V to 3.6 V.
8. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
9. All GPIO meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I^2C GPIO pins also meet the above specs.

AC Digital Block Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ T_A ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 24. 3.3 V AC Digital Block Specifications

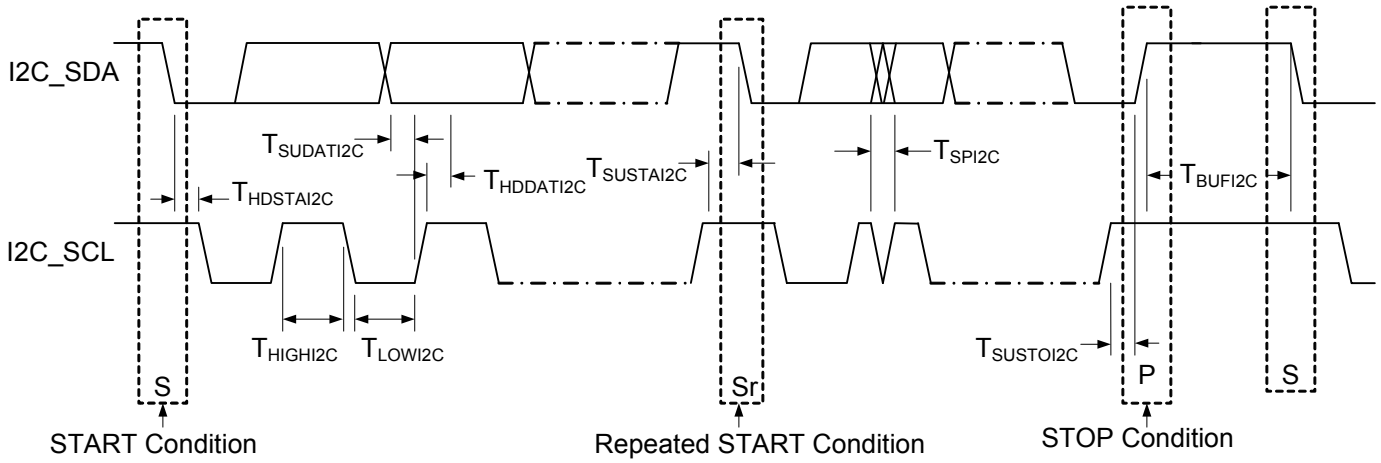
Function	Description	Min	Typ	Max	Unit	Notes
All Functions	Block input clock frequency	–	–	24.6	MHz	3.0 V < V_{DD} < 3.6 V.
Timer/ Counter/ PWM	Enable input pulse width	50[17]	–	–	ns	
	Input clock frequency	–	–	24.6	MHz	
Dead Band	Kill pulse width:					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50	–	–	ns	
	Disable mode	50	–	–	ns	
	Input clock frequency	–	–	24.6	MHz	3.0 V ≤ V_{DD} ≤ 3.6 V.
SPIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock frequency	–	–	4.1	MHz	Note for SPIS Input Clock Frequency: The input clock is the SPI SCLK in SPIS mode.
	Width of SS_ Negated between transmissions	50	–	–	ns	
Transmitter	Input clock frequency	–	–	24.6	MHz	The baud rate is equal to the input clock frequency divided by 8.
Receiver	Input clock frequency	–	–	24.6	MHz	The baud rate is equal to the input clock frequency divided by 8.

Table 25. 2.7 V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All Functions	Block input clock frequency	–	–	12.7	MHz	2.4 V ≤ V_{DD} ≤ 3.0 V.
Timer/ Counter/ PWM	Enable input clock width	100	–	–	ns	
	Input clock frequency	–	–	12.7	MHz	
Dead Band	Kill pulse width:					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	100	–	–	ns	
	Disable mode	100	–	–	ns	
	Input clock frequency	–	–	12.7	MHz	2.4 V ≤ V_{DD} < 3.0 V.
SPIM	Input clock frequency	–	–	6.35	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock frequency	–	–	4.1	MHz	Note for input clock frequency: The input clock is the SPI SCLK in SPIS mode.
	Width of SS_ Negated between transmissions	100	–	–	ns	
Transmitter	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.
Receiver	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.

Note
17. 50 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

Figure 14. Definition of Timing for Fast-/Standard-Mode on the I²C Bus



Packaging Information

This section illustrates the packaging specifications for the CY7C603xx device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled PSoC Emulator Pod Dimensions at http://www.cypress.com.

Packaging Dimensions

Figure 15. 28-pin (210-Mil) SSOP

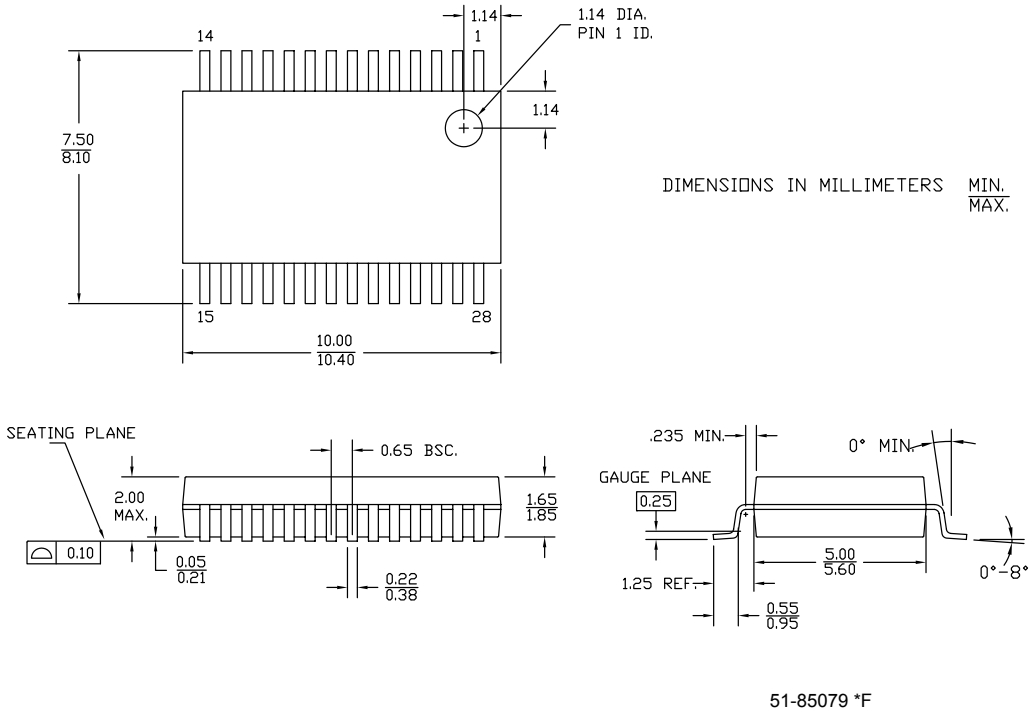
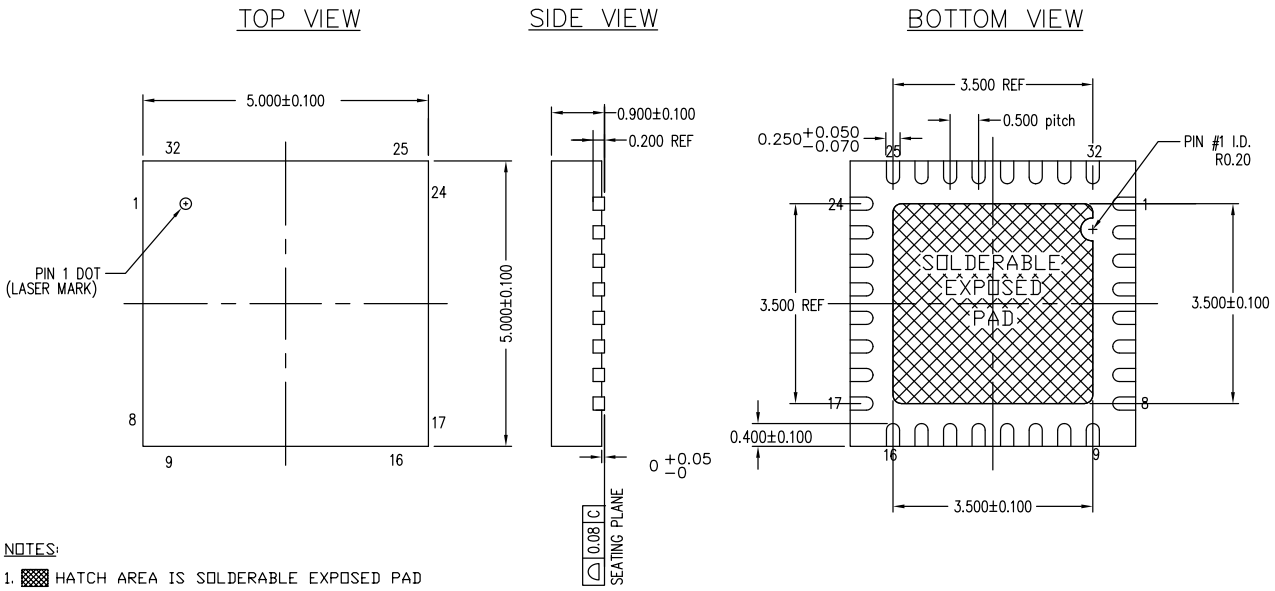


Figure 16. 32-pin QFN (5 × 5 mm) (SAWN)



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-220
3. DIMENSIONS ARE IN MILLIMETERS
4. PACKAGE WEIGHT: SEE CYPRESS PACKAGE MATERIAL DECLARATION DATASHEET (PMDD) POSTED ON THE CYPRESS WEB

001-30999 *D

Acronyms

Acronyms Used

Table 34 lists the acronyms that are used in this document.

Table 34. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	PCB	printed circuit board
API	application programming interface	PGA	programmable gain amplifier
CPU	central processing unit	PLL	phase-locked loop
CT	continuous time	POR	power-on reset
DAC	digital-to-analog converter	PPOR	precision power on reset
DC	direct current	PSoC®	Programmable System-on-Chip
DTMF	dual-tone multi-frequency	PWM	pulse-width modulator
ECO	external crystal oscillator	QFN	quad flat no leads
EEPROM	electrically erasable programmable read-only memory	RTC	real time clock
GPIO	general purpose I/O	SAR	successive approximation
ICE	in-circuit emulator	SC	switched capacitor
IDE	integrated development environment	SLIMO	slow IMO
ILO	internal low speed oscillator	SMP	switch mode pump
IMO	internal main oscillator	SPI™	serial peripheral interface
I/O	input/output	SRAM	static random access memory
ISSP	in-system serial programming	SROM	supervisory read only memory
LCD	liquid crystal display	SSOP	shrink small-outline package
LPC	low power comparator	USB	universal serial bus
LVD	low voltage detect	WDT	watchdog timer
MAC	multiply-accumulate	XRES	external reset

Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 (001-14503)

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages – available at http://www.amkor.com.

Document Conventions

Units of Measure

Table 35 lists the units of measures.

Table 35. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
kB	1024 bytes	µH	microhenry
dB	decibels	µs	microseconds
°C	degree Celsius	ms	milliseconds
µF	microfarads	ns	nanoseconds
fF	femtofarads	ps	picoseconds
pF	picofarads	µV	microvolts
kHz	kilohertz	mV	millivolts
MHz	megahertz	mVpp	millivolts peak-to-peak
rt-Hz	root hertz	nV	nanovolts
kΩ	kilohms	V	volts
Ω	ohm	µW	microwatts
µA	microamperes	W	watts
mA	milliamperes	mm	millimeter
nA	nanoamperes	ppm	parts per million
pA	pikoamperes	%	percent

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are switched capacitor (SC) and continuous time (CT) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
Application Programming Interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.

Glossary *(continued)*

duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
flash	An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I^2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I^2C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls below a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the *slave device*.

Glossary *(continued)*

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level *API* for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Document History Page *(continued)*

Description Title: CY7C603xx, enCoRe™ III Low Voltage Document Number: 38-16018				
*N	3285017	DIVA	07/07/2011	Updated Getting Started, Development Tools, and Designing with PSoC Designer. Updated Thermal Impedances and Solder Reflow Peak Temperature table.
*O	3521530	CSAI	02/10/2012	No technical updates.
*P	4623515	SIRK	01/14/2015	Updated Packaging Information: spec 51-85079 – Changed revision from *E to *F. spec 001-30999 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.

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