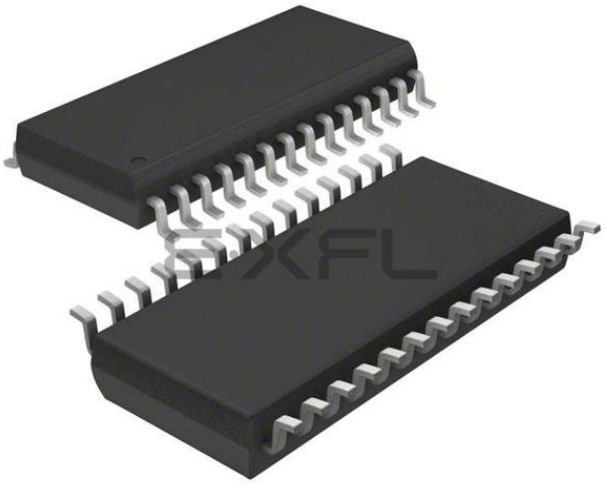


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	12MHz
Connectivity	I²C, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c60323-pvxc

Contents

enCoRe III Low Voltage Functional Overview

The enCoRe III low voltage (enCoRe III LV) CY7C603xx device is based on the flexible PSoC® architecture. This supports a simple set of peripherals that can be configured to match the needs of each application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts.

This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. A fast CPU, flash program memory, SRAM data memory, and configurable IO are included in both 28-pin SSOP and 32-pin QFN packages.

The enCoRe III LV architecture, as shown in Figure 1, consists of four main areas: the enCoRe III LV Core, the system resources, digital system, and analog system. Configurable global bus resources allow combining all the device resources into a complete custom system. Each enCoRe III LV device supports a limited set of digital and analog peripherals. Depending on the package, up to 28 general purpose I/Os (GPIOs) are also included. The GPIOs provide access to the global digital and analog interconnects.

enCoRe III LV Core

The enCoRe III LV core is a powerful engine that supports a rich feature set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO (internal main oscillator) and ILO (internal low-speed oscillator).

The CPU core, called the M8C, is a powerful processor with speeds up to 12 MHz. The M8C is a four MIPS 8-bit Harvard -architecture microprocessor. The core includes a CPU, memory, clocks, and configurable GPIO.

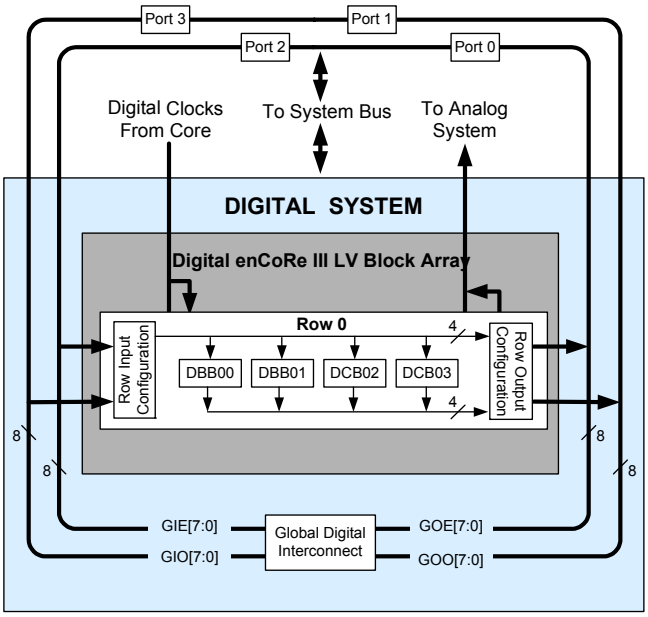
System resources provide additional capability, such as digital clocks to increase flexibility, I^2C functionality for implementing an I^2C master, slave, multi-master, an internal voltage reference that provides an absolute value of 1.3 V to a number of subsystems, a switch mode pump (SMP) that generates normal operating voltages off a single battery cell, and various system resets supported by the M8C.

The Digital System

The digital system consists of 4 digital enCoRe III LV blocks. Each block is an 8-bit resource. Digital peripheral configurations include the following:

- PWM usable as timer or counter
- SPI master and slave
- I^2C slave and multi-master
- CMP
- ADC10
- SARADC

Figure 1. Digital System Block Diagram



The digital blocks may be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

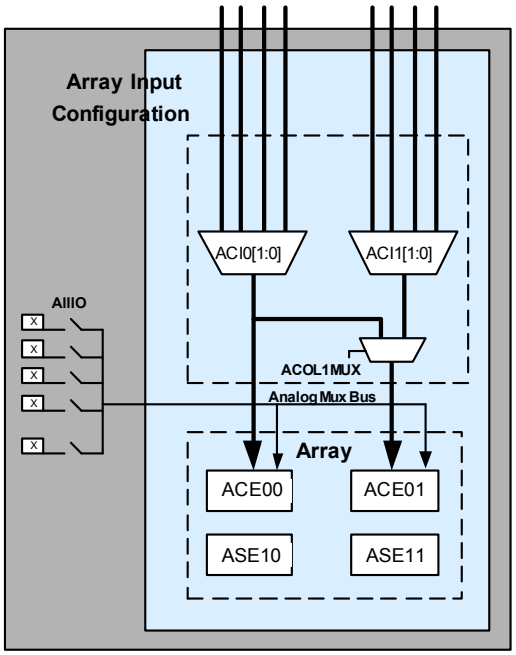
The Analog System

The analog system consists of two configurable blocks. Analog peripherals are very flexible and may be customized to support specific application requirements. Some of the common analog functions for this device (available as user modules) are:

- Analog-to-digital converters (single with 8-bit resolution)
- Pin-to-pin comparators
- Single-ended comparators with absolute (1.3-V) reference
- 1.3-V reference (as a system resource)

Analog blocks are provided in columns of two, which includes one continuous time (CT) (CT - ACE00 or ACE01) and one switched capacitor (SC) (SC - ASE10 or ASE11) blocks.

Figure 2. Analog System Block Diagram



The Analog Multiplexer System

The analog mux bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters (ADC). An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Additional System Resources

System resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a switch mode pump, low voltage detection, and power on reset. Brief statements describing the merits of each system resource follow.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks may be generated using digital blocks as clock dividers.
- The I^2C module provides 100 kHz and 400 kHz communication over two wires. slave, master, and multi-master modes are all supported.
- Low voltage detection interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- An internal 1.3-V voltage reference provides an absolute reference for the analog system.
- An integrated switch mode pump generates normal operating voltages from a single 1.2 V battery cell, providing a low-cost boost converter.
- Versatile analog multiplexer system.

enCoRe III LV Device Characteristics

The enCoRe III LV devices have four digital blocks and four analog blocks. Table 1 lists the resources available for specific enCoRe III LV devices.

Table 1. enCoRe III LV Device Characteristics

Part Number	Digital IO	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY7C60323-PVXC	24	1	4	24	0	2	4	512 Bytes	8K

Getting Started

The quickest path to understanding the enCoRe III LV silicon is by reading this data sheet and using the PSoC Designer integrated development environment (IDE). This data sheet is an overview of the enCoRe III LV and presents specific pin, register, and electrical specifications. enCoRe III LV is based on the architecture of the CY8C21x34. For in-depth information, along with detailed programming information, refer to the PSoC Programmable System-on-Chip Technical Reference Manual, which is available at http://www.cypress.com.

For up-to-date ordering, packaging, and electrical specification information, refer to the latest device data sheets on the web at http://www.cypress.com.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Figure 6. CY7C60323-LTXC 32-pin Device Sawn

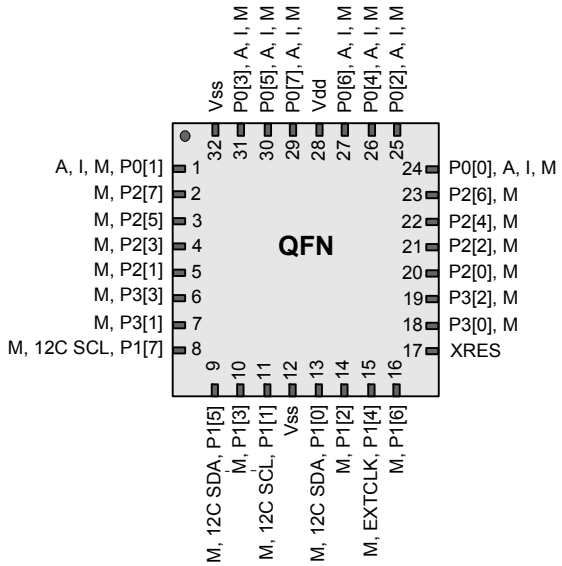


Figure 7. CY7C60333-LTXC 32-pin Device Sawn

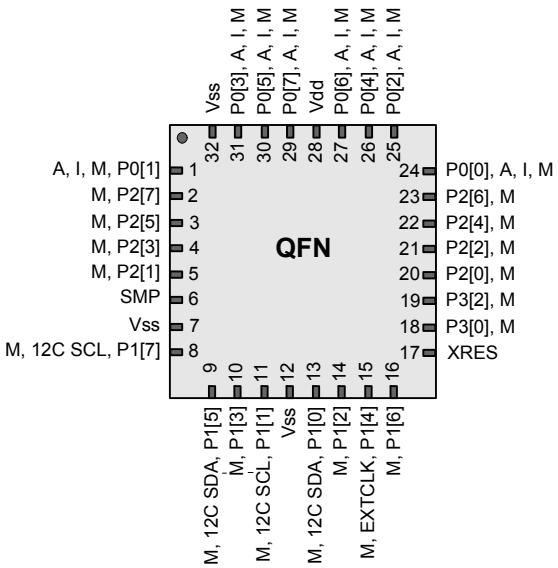


Table 3. 32-pin Part Pinout (QFN[1])

Pin No.	Type		Name	Description
	Digital	Analog		
1	IO	I, M	P0[1]	Analog column mux input, integrating input.
2	IO	M	P2[7]	
3	IO	M	P2[5]	
4	IO	M	P2[3]	
5	IO	M	P2[1]	
6	IO	M	P3[3]	In CY7C60323 part.
6	Power		SMP	Switch mode pump (SMP) connection to required external components in CY7C60333 part.
7	IO	M	P3[1]	In CY7C60323 Part.
7	Power		Vss	Ground connection in CY7C60333 part.
8	IO	M	P1[7]	I^2C serial clock (SCL).
9	IO	M	P1[5]	I^2C serial data (SDA).
10	IO	M	P1[3]	
11	IO	M	P1[1]	I^2C SCL, ISSP-SCLK.
12	Power		Vss	Ground connection.
13	IO	M	P1[0]	I^2C SDA, ISSP-SDATA.
14	IO	M	P1[2]	
15	IO	M	P1[4]	Optional external clock input (EXTCLK).
16	IO	M	P1[6]	
17	Input		XRES	Active HIGH external reset with internal pull-down.
18	IO	M	P3[0]	
19	IO	M	P3[2]	
20	IO	M	P2[0]	
21	IO	M	P2[2]	
22	IO	M	P2[4]	
23	IO	M	P2[6]	
24	IO	I, M	P0[0]	Analog column mux input.
25	IO	I, M	P0[2]	Analog column mux input.
26	IO	I, M	P0[4]	Analog column mux input.
27	IO	I, M	P0[6]	Analog column mux input.
28	Power		V_{DD}	Supply voltage.
29	IO	I, M	P0[7]	Analog column mux input.
30	IO	I, M	P0[5]	Analog column mux input
31	IO	I, M	P0[3]	Analog column mux input, integrating input.
32	Power		Vss	Ground connection.

LEGEND A = analog, I = input, O = output, and M = analog mux input.

Note
1. The QFN package has a center pad that must be connected to ground (Vss).

Table 6. Register Map 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASE10CR0	80	RW		C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASE11CR0	84	RW		C4	
PRT1DM1	05	RW		45			85			C5	
PRT1IC0	06	RW		46			86			C6	
PRT1IC1	07	RW		47			87			C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
	10			50			90		GDI_O_IN	D0	RW
	11			51			91		GDI_E_IN	D1	RW
	12			52			92		GDI_O_OU	D2	RW
	13			53			93		GDI_E_OU	D3	RW
	14			54			94			D4	
	15			55			95			D5	
	16			56			96			D6	
	17			57			97			D7	
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A			9A		MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5		ADC0_TR	E5	RW
DBB01OU	26	RW	AMD_CR1	66	RW		A6		ADC1_TR	E6	RW
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B		CLK_CR3	6B	RW		AB		ECO_TR	EB	W

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 6. Register Map 1 Table: Configuration Space *(continued)*

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA		FLS_PR1	FA	RW
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_CR	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the enCoRe III LV device. For up-to-date electrical specifications, check the latest data sheet by visiting the web at http://www.cypress.com.

Specifications are valid for 0 °C ≤ T_A ≤ 70 °C and T_J ≤ 85 °C as specified, except where noted.

Refer to Table 19 on page 22 for the electrical specifications for the internal main oscillator (IMO) using SLIMO mode.

Figure 10. Voltage versus CPU Frequency

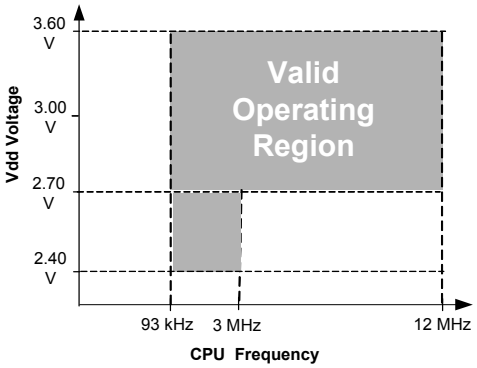
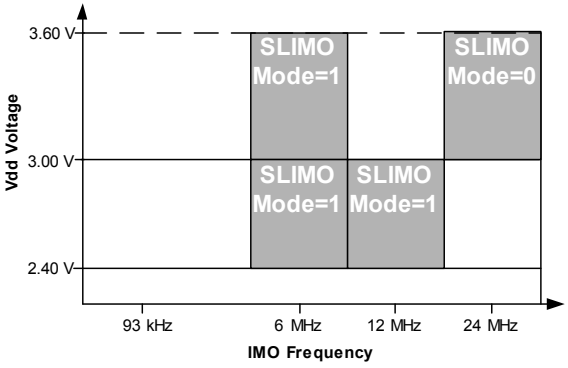


Figure 11. IMO Frequency Trim Options



The allowable CPU operating region for 12 MHz has been extended down to 2.7 V from the original 3.0 V design target. The customer's application is responsible for monitoring voltage and throttling back CPU speed in accordance with Figure 10 when voltage approaches 2.7 V. Refer to Table 16 for LVD specifications. Note that the device does not support a preset trip at 2.7 V. To detect V_{DD} drop at 2.7 V, an external circuit or device such as the WirelessUSB LP - CYRF6936 must be employed; or if the design permits, the nearest LVD trip value at 2.9 V can be used.

Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{STG}	Storage temperature	–40	–	+90	°C	Higher storage temperatures reduce data retention time.
$T_{BAKETEMP}$	Bake temperature		125	See package label	°C	
$T_{BAKETIME}$	Bake time	See package label		72	Hours	
T_A	Ambient temperature with power applied	0	–	+70	°C	
V_{DD}	Supply voltage on V_{DD} relative to Vss	–0.5	–	5	V	
V_{IO}	DC input voltage	Vss – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	Vss – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+25	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human body model ESD.
LU	Latch up current	–	–	200	mA	

Operating Temperature

Table 8. Operating Temperature

Parameter	Description	Min	Typ	Max	Unit	Notes
T_A	Ambient temperature	0	–	+70	°C	
T_J	Junction temperature	0	–	+85	°C	The temperature rise from ambient to junction is package specific. See Table 31 on page 30. The user must limit the power consumption to comply with this requirement.

Table 11. 2.7V DC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	V_{DD} – 0.4	–	–	V	I_{OH} = 2.5 mA (6.25 Typ), V_{DD} = 2.4 to 3.0 V (16 mA maximum, 50 mA Typ combined I_{OH} budget).
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 10 mA, V_{DD} = 2.4 to 3.0 V (90 mA maximum combined I_{OL} budget).
I_{OH}	High level source current	2.5	–	–	mA	
I_{OL}	Low level sink current	10	–	–	mA	
V_{IL}	Input low level	–	–	0.75	V	V_{DD} = 2.4 to 3.0.
V_{IH}	Input high level	2.0	–	–	V	V_{DD} = 2.4 to 3.0.
V_H	Input hysteresis	–	90	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.

DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ T_A ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 12. 3.3-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	μV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 μA
I_{EBOA00}	Input leakage current (Port 0, Pin 0 analog pin)	–	50	–	nA	Gross tested to 1 μA
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0	–	V_{DD} – 1	V	
G_{OLOA}	Open loop gain	–	80	–	dB	
I_{SOA}	Amplifier supply current	–	10	30	μA	

Table 13. 2.7-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	μV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 μA
I_{EBOA00}	Input leakage current (Port 0, Pin 0 analog pin)	–	50	–	nA	Gross tested to 1 μA
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0	–	V_{DD} – 1	V	
G_{OLOA}	Open loop gain	–	80	–	dB	
I_{SOA}	Amplifier supply current	–	10	30	μA	

DC Programming Specifications

Table 17 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ T_A ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 17. DC Programming Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5.0	5.5	V	This specification applies to the functional requirements of external programmer tools.
V_{DDLV}	Low V_{DD} for verify	2.4	2.5	2.6	V	This specification applies to the functional requirements of external programmer tools.
V_{DDHV}	High V_{DD} for verify	3.5	3.6	3.7	V	This specification applies to the functional requirements of external programmer tools.
$V_{DDIWRITE}$	Supply voltage for flash write operation	2.7	–	3.6	V	This specification applies to this device when it is executing internal flash writes.
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.1	–	–	V	
I_{ILP}	Input current when applying Vilp to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input current when applying Vihp to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	Vss + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)	50,000[7]	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash dndurance (total)[8]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	10	–	–	Years	

DC I^2C Specifications

Table 18 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ T_A ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 18. DC I^2C Specifications[9]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	2.4 V ≤ V_{DD} ≤ 3.6 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	2.4 V ≤ V_{DD} ≤ 3.6 V

Notes
7. The 50,000 cycle Flash endurance per block will only be guaranteed if the Flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V and 3.0 V to 3.6 V.
8. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
9. All GPIO meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I^2C GPIO pins also meet the above specs.

Table 20. 2.7 V AC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
F_{IMO12}	Internal main oscillator (IMO) frequency for 12 MHz	11.5	12	12.7[14, 15]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 11 on page 15. SLIMO mode = 1.
F_{IMO6}	IMO frequency for 6 MHz	5.5	6	6.5[14, 15]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 11 on page 15. SLIMO mode = 1.
F_{CPU1}	CPU frequency (2.7 V nominal)	0.093	3	3.15[14, 15]	MHz	12 MHz only for SLIMO mode = 0.
F_{BLK27}	Digital block frequency (2.7 V nominal)	0	12	12.5[14, 15]	MHz	Refer to the AC digital block specifications.
F_{32K1}	Internal low speed oscillator frequency	8	32	96	kHz	
F_{32K_U}	Internal low speed oscillator untrimmed frequency	5	–	100	kHz	
DC_{ILO}	Internal low speed oscillator duty cycle	20	50	80	%	
T_{XRST}	External reset pulse width	10	–	–	µs	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V / ms	
$T_{POWERUP}$	Time from End of POR to CPU executing code	–	16	100	ms	
t_{jit_IMO}	12 MHz IMO cycle-to-cycle jitter (RMS)[16]	–	400	1000	ps	
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)[16]	–	600	1300	ps	N = 32
	12 MHz IMO period jitter (RMS)[16]	–	100	500	ps	

Notes
14. Accuracy derived from Internal Main Oscillator with appropriate trim for V_{DD} range.
15. 2.4 V < V_{DD} < 3.0 V.
16. Refer to Cypress Jitter Specifications Application Note AN5054 “Understanding Datasheet Jitter Specifications for Cypress Timing Products” at www.cypress.com under Application Notes for more information.

AC GPIO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ T_A ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

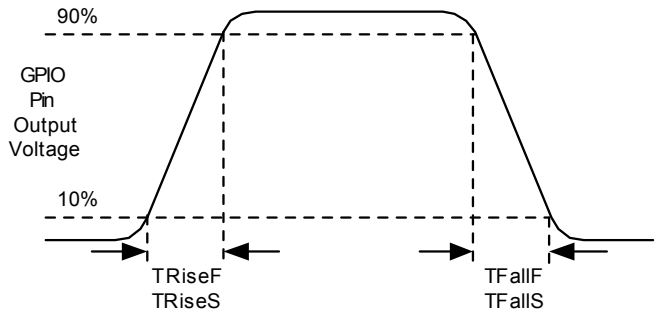
Table 21. 3.3 V AC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
F_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal Strong Mode
TRiseS	Rise time, slow strong mode, cload = 50 pF	7	27	–	ns	V_{DD} = 3 to 3.6 V, 10%–90%
TFallS	Fall time, slow strong mode, cload = 50 pF	7	22	–	ns	V_{DD} = 3 to 3.6 V, 10%–90%

Table 22. 2.7 V AC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
F_{GPIO}	GPIO operating frequency	0	–	3	MHz	Normal Strong Mode
TRiseF	Rise time, normal strong mode, cload = 50 pF	6	–	50	ns	V_{DD} = 2.4 to 3.0 V, 10%–90%
TFallF	Fall time, normal strong mode, cload = 50 pF	6	–	50	ns	V_{DD} = 2.4 to 3.0 V, 10%–90%
TRiseS	Rise time, slow strong mode, cload = 50 pF	18	40	120	ns	V_{DD} = 2.4 to 3.0 V, 10%–90%
TFallS	Fall time, slow strong mode, cload = 50 pF	18	40	120	ns	V_{DD} = 2.4 to 3.0 V, 10%–90%

Figure 13. GPIO Timing Diagram



AC Operational Amplifier Specifications

Table 23 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ T_A ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 23. AC Operational Amplifier Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{COMP}	Comparator mode response time, 50 mV overdrive			100 200	ns ns	V_{DD} ≥ 3.0 V. 2.4 V < Vcc < 3.0 V.

AC Digital Block Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ T_A ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 24. 3.3 V AC Digital Block Specifications

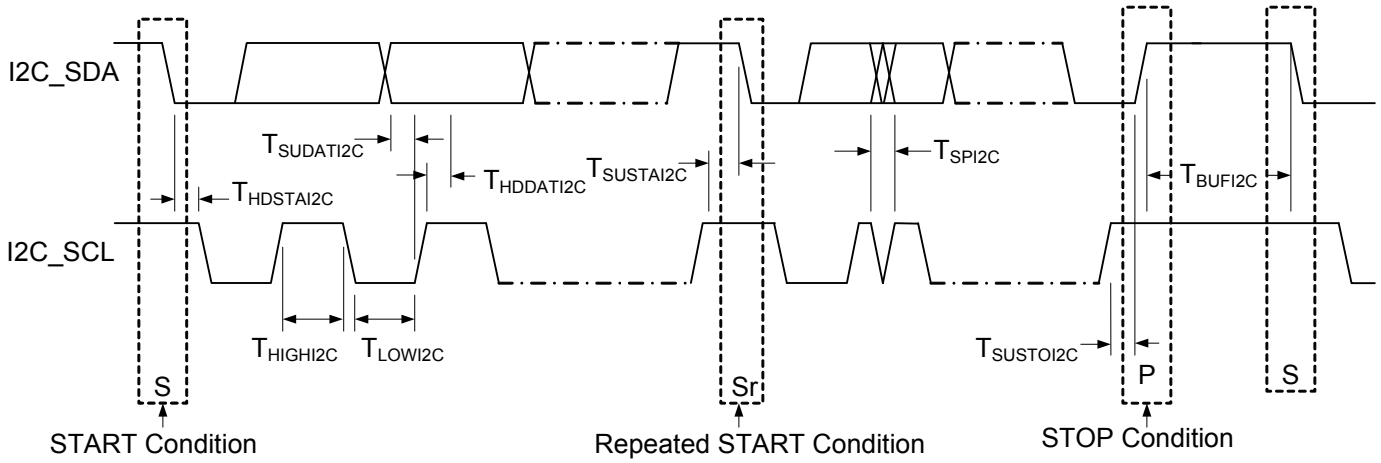
Function	Description	Min	Typ	Max	Unit	Notes
All Functions	Block input clock frequency	–	–	24.6	MHz	3.0 V < V_{DD} < 3.6 V.
Timer/ Counter/ PWM	Enable input pulse width	50[17]	–	–	ns	
	Input clock frequency	–	–	24.6	MHz	
Dead Band	Kill pulse width:					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50	–	–	ns	
	Disable mode	50	–	–	ns	
	Input clock frequency	–	–	24.6	MHz	3.0 V ≤ V_{DD} ≤ 3.6 V.
SPIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock frequency	–	–	4.1	MHz	Note for SPIS Input Clock Frequency: The input clock is the SPI SCLK in SPIS mode.
	Width of SS_ Negated between transmissions	50	–	–	ns	
Transmitter	Input clock frequency	–	–	24.6	MHz	The baud rate is equal to the input clock frequency divided by 8.
Receiver	Input clock frequency	–	–	24.6	MHz	The baud rate is equal to the input clock frequency divided by 8.

Table 25. 2.7 V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All Functions	Block input clock frequency	–	–	12.7	MHz	2.4 V ≤ V_{DD} ≤ 3.0 V.
Timer/ Counter/ PWM	Enable input clock width	100	–	–	ns	
	Input clock frequency	–	–	12.7	MHz	
Dead Band	Kill pulse width:					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	100	–	–	ns	
	Disable mode	100	–	–	ns	
	Input clock frequency	–	–	12.7	MHz	2.4 V ≤ V_{DD} < 3.0 V.
SPIM	Input clock frequency	–	–	6.35	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock frequency	–	–	4.1	MHz	Note for input clock frequency: The input clock is the SPI SCLK in SPIS mode.
	Width of SS_ Negated between transmissions	100	–	–	ns	
Transmitter	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.
Receiver	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.

Note
17. 50 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

Figure 14. Definition of Timing for Fast-/Standard-Mode on the I²C Bus



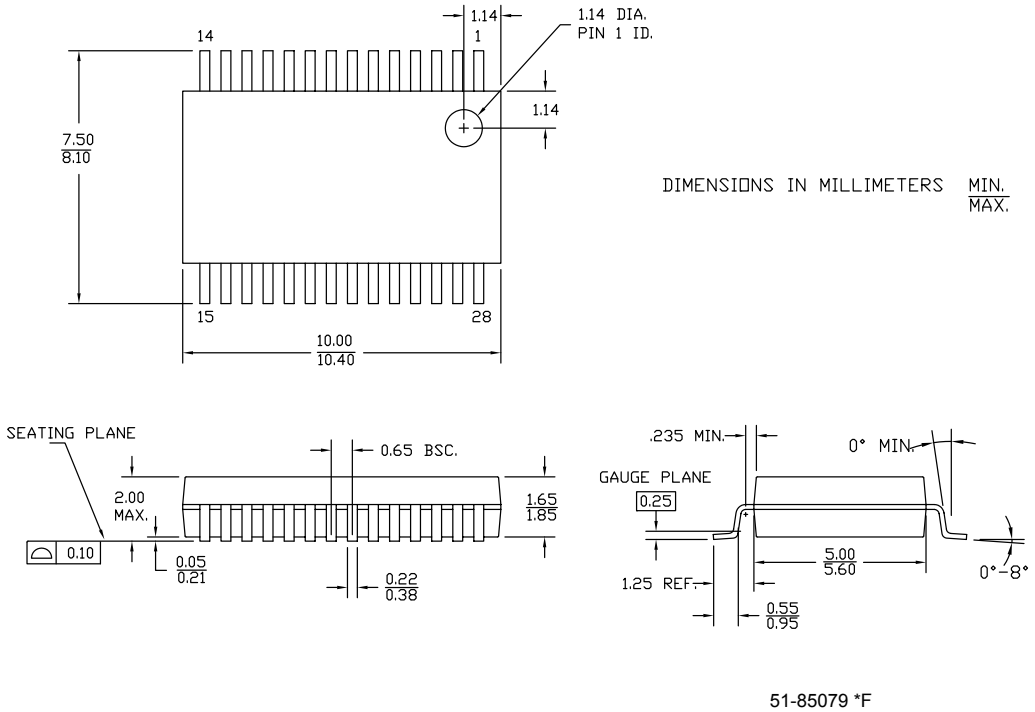
Packaging Information

This section illustrates the packaging specifications for the CY7C603xx device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled PSoC Emulator Pod Dimensions at http://www.cypress.com.

Packaging Dimensions

Figure 15. 28-pin (210-Mil) SSOP



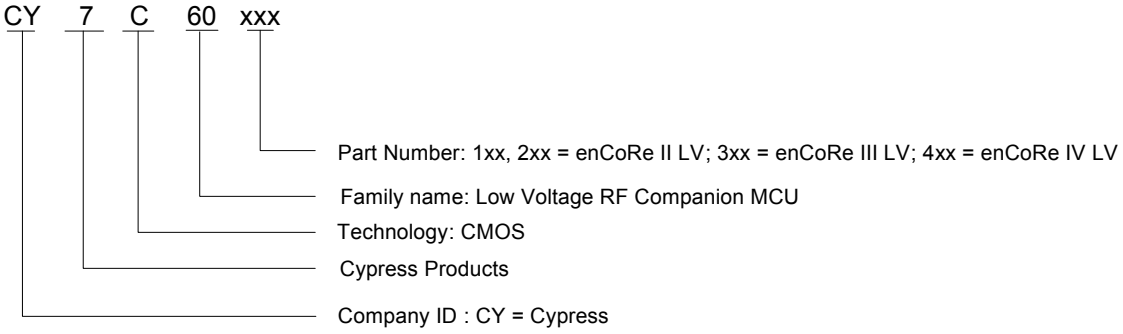
Ordering Information

The following table lists the CY7C603xx device's key package features and ordering codes

Table 33. CY7C603xx Device Key Features and Ordering Information

Package Type	Ordering Part Number	Flash Size	RAM Size	SMP	I/O
28-SSOP	CY7C60323-PVXC	8K	512	No	24
28-SSOP Tape and Reel	CY7C60323-PVXCT	8K	512	No	24
32-QFN SAWN	CY7C60323-LTXC	8K	512	No	28
32-QFN SAWN Tape and Reel	CY7C60323-LTXCT	8K	512	No	28

Ordering Code Definitions



Acronyms

Acronyms Used

Table 34 lists the acronyms that are used in this document.

Table 34. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	PCB	printed circuit board
API	application programming interface	PGA	programmable gain amplifier
CPU	central processing unit	PLL	phase-locked loop
CT	continuous time	POR	power-on reset
DAC	digital-to-analog converter	PPOR	precision power on reset
DC	direct current	PSoC®	Programmable System-on-Chip
DTMF	dual-tone multi-frequency	PWM	pulse-width modulator
ECO	external crystal oscillator	QFN	quad flat no leads
EEPROM	electrically erasable programmable read-only memory	RTC	real time clock
GPIO	general purpose I/O	SAR	successive approximation
ICE	in-circuit emulator	SC	switched capacitor
IDE	integrated development environment	SLIMO	slow IMO
ILO	internal low speed oscillator	SMP	switch mode pump
IMO	internal main oscillator	SPI™	serial peripheral interface
I/O	input/output	SRAM	static random access memory
ISSP	in-system serial programming	SROM	supervisory read only memory
LCD	liquid crystal display	SSOP	shrink small-outline package
LPC	low power comparator	USB	universal serial bus
LVD	low voltage detect	WDT	watchdog timer
MAC	multiply-accumulate	XRES	external reset

Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 (001-14503)

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages – available at http://www.amkor.com.

Glossary *(continued)*

duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
flash	An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I^2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I^2C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls below a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the *slave device*.

Document History Page *(continued)*

Description Title: CY7C603xx, enCoRe™ III Low Voltage Document Number: 38-16018				
*N	3285017	DIVA	07/07/2011	Updated Getting Started, Development Tools, and Designing with PSoC Designer. Updated Thermal Impedances and Solder Reflow Peak Temperature table.
*O	3521530	CSAI	02/10/2012	No technical updates.
*P	4623515	SIRK	01/14/2015	Updated Packaging Information: spec 51-85079 – Changed revision from *E to *F. spec 001-30999 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC® Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/go/support