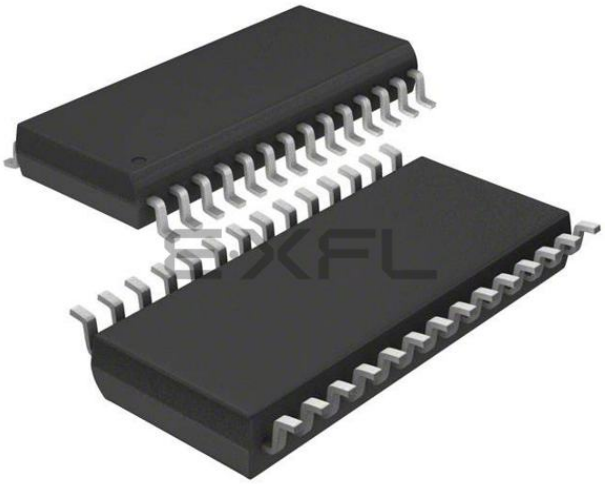

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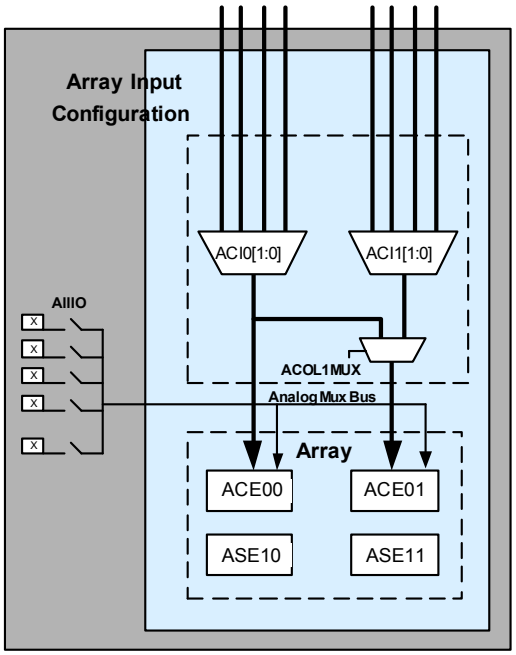
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	12MHz
Connectivity	I²C, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c60323-pvxct

Figure 2. Analog System Block Diagram



The Analog Multiplexer System

The analog mux bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters (ADC). An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Additional System Resources

System resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a switch mode pump, low voltage detection, and power on reset. Brief statements describing the merits of each system resource follow.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks may be generated using digital blocks as clock dividers.
- The I^2C module provides 100 kHz and 400 kHz communication over two wires. slave, master, and multi-master modes are all supported.
- Low voltage detection interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- An internal 1.3-V voltage reference provides an absolute reference for the analog system.
- An integrated switch mode pump generates normal operating voltages from a single 1.2 V battery cell, providing a low-cost boost converter.
- Versatile analog multiplexer system.

enCoRe III LV Device Characteristics

The enCoRe III LV devices have four digital blocks and four analog blocks. Table 1 lists the resources available for specific enCoRe III LV devices.

Table 1. enCoRe III LV Device Characteristics

Part Number	Digital IO	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY7C60323-PVXC	24	1	4	24	0	2	4	512 Bytes	8K

Getting Started

The quickest path to understanding the enCoRe III LV silicon is by reading this data sheet and using the PSoC Designer integrated development environment (IDE). This data sheet is an overview of the enCoRe III LV and presents specific pin, register, and electrical specifications. enCoRe III LV is based on the architecture of the CY8C21x34. For in-depth information, along with detailed programming information, refer to the PSoC Programmable System-on-Chip Technical Reference Manual, which is available at http://www.cypress.com.

For up-to-date ordering, packaging, and electrical specification information, refer to the latest device data sheets on the web at http://www.cypress.com.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select user modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Pin Information

The enCoRe III LV device is available in 28-pin SSOP and 32-pin QFN packages. Every port pin (labeled with a “P”) is capable of Digital IO and connection to the common analog bus. However, Vss, V_{DD}, SMP, and XRES are not capable of Digital IO.

28-pin Part Pinout

Figure 3. CY7C60323-PVXC 28-pin Device

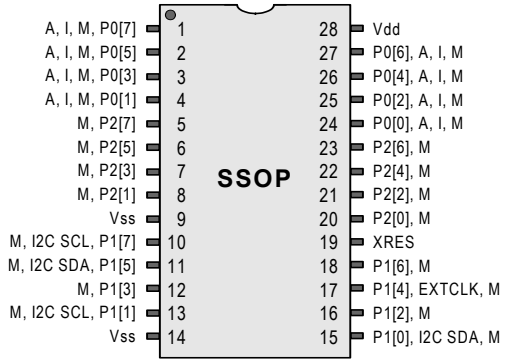


Table 2. Pin Definitions - CY7C60323-PVXC 28-pin Device

Pin No.	Type		Name	Description
	Digital	Analog		
1	IO	I, M	P0[7]	Analog column mux input.
2	IO	I, M	P0[5]	Analog column mux input and column output.
3	IO	I, M	P0[3]	Analog column mux input and column output, integrating input.
4	IO	I, M	P0[1]	Analog column mux input, integrating input.
5	IO	M	P2[7]	
6	IO	M	P2[5]	
7	IO	I, M	P2[3]	Direct switched capacitor block input.
8	IO	I, M	P2[1]	Direct switched capacitor block input.
9	Power		Vss	Ground connection.
10	IO	M	P1[7]	I^2C serial clock (SCL).
11	IO	M	P1[5]	I^2C serial data (SDA).
12	IO	M	P1[3]	
13	IO	M	P1[1]	I^2C SCL, ISSP-SCLK.
14	Power		Vss	Ground connection.
15	IO	M	P1[0]	I^2C SDA, ISSP-SDATA.
16	IO	M	P1[2]	
17	IO	M	P1[4]	Optional external clock input (EXTCLK).
18	IO	M	P1[6]	
19	Input		XRES	Active HIGH external reset with internal pull down.
20	IO	I, M	P2[0]	Direct switched capacitor block input.
21	IO	I, M	P2[2]	Direct switched capacitor block input.
22	IO	M	P2[4]	
23	IO	M	P2[6]	
24	IO	I, M	P0[0]	Analog column mux input
25	IO	I, M	P0[2]	Analog column mux input
26	IO	I, M	P0[4]	Analog column mux input
27	IO	I, M	P0[6]	Analog column mux input
28	Power		V_{DD}	Supply voltage.

LEGEND A = analog, I = input, O = output, and M = analog mux input.

32-pin Part Pinout

Figure 4. CY7C60323-LFXC 32-pin Device

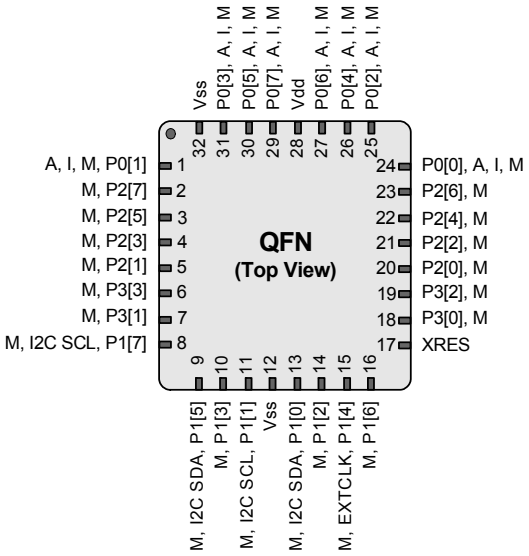


Figure 5. CY7C60333-LFXC 32-pin Device

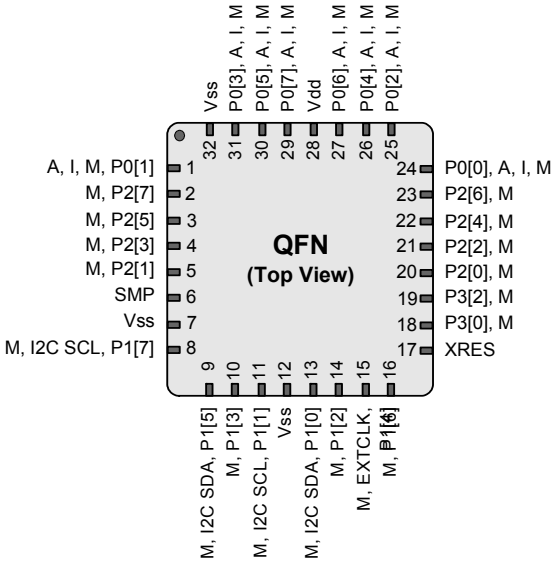


Table 5. Register Map 0 Table: User Space *(continued)*

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W	AMUXCFG	61	RW		A1		INT_MSK1	E1	RW
DBB00DR2	22	RW	PWM_CR	62	RW		A2		INT_VC	E2	RC
DBB00CR0	23	#		63			A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4			E4	
DBB01DR1	25	W		65			A5			E5	
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#	ADC0_CR	68	#		A8			E8	
DCB02DR1	29	W	ADC1_CR	69	#		A9			E9	
DCB02DR2	2A	RW		6A			AA			EA	
DCB02CR0	2B	#		6B			AB			EB	
DCB03DR0	2C	#	TMP_DR0	6C	RW		AC			EC	
DCB03DR1	2D	W	TMP_DR1	6D	RW		AD			ED	
DCB03DR2	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCB03CR0	2F	#	TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_D	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 6. Register Map 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASE10CR0	80	RW		C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASE11CR0	84	RW		C4	
PRT1DM1	05	RW		45			85			C5	
PRT1IC0	06	RW		46			86			C6	
PRT1IC1	07	RW		47			87			C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
	10			50			90		GDI_O_IN	D0	RW
	11			51			91		GDI_E_IN	D1	RW
	12			52			92		GDI_O_OU	D2	RW
	13			53			93		GDI_E_OU	D3	RW
	14			54			94			D4	
	15			55			95			D5	
	16			56			96			D6	
	17			57			97			D7	
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A			9A		MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5		ADC0_TR	E5	RW
DBB01OU	26	RW	AMD_CR1	66	RW		A6		ADC1_TR	E6	RW
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B		CLK_CR3	6B	RW		AB		ECO_TR	EB	W

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 6. Register Map 1 Table: Configuration Space *(continued)*

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA		FLS_PR1	FA	RW
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_CR	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

DC Electrical Characteristics

DC Chip-Level Specifications

Table 9 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ T_A ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 9. DC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DD}	Supply voltage	2.40	–	3.6	V	See Table 16 on page 20.
I_{DD3}	Supply current, IMO = 6 MHz using SLIMO mode.	–	1.2	2	mA	Conditions are V_{DD} = 3.3 V, T_A = 25 °C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz.
I_{DD27}	Supply current, IMO = 6 MHz using SLIMO mode.	–	1.1	1.5	mA	Conditions are V_{DD} = 2.55 V, T_A = 25 °C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz.
I_{SB27}	Sleep (Mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active. Mid temperature range.	–	2.6	4.	µA	V_{DD} = 2.55 V, 0 °C ≤ T_A ≤ 40 °C.
I_{SB}	Sleep (Mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active.	–	2.8	5	µA	V_{DD} = 3.3 V, 0 °C ≤ T_A ≤ 70 °C.
V_{REF}	Reference voltage (Bandgap)	1.28	1.30	1.32	V	Trimmed for appropriate V_{DD}. V_{DD} = 3.0 V to 3.6 V.
V_{REF27}	Reference voltage (Bandgap)	1.16	1.30	1.33	V	Trimmed for appropriate V_{DD}. V_{DD} = 2.4 V to 3.0 V.
AGND	Analog ground	V_{REF} – 0.003	V_{REF}	V_{REF} + 0.003	V	

DC GPIO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ T_A ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 10. 3.3 V DC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	V_{DD} – 1.0	–	–	V	I_{OH} = 3 mA, V_{DD} > 3.0 V
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 10 mA, V_{DD} > 3.0 V
I_{OH}	High level source current	3	–	–	mA	
I_{OL}	Low level sink current	10	–	–	mA	
V_{IL}	Input low level	–	–	0.8	V	V_{DD} = 3.0 to 3.6.
V_{IH}	Input high level	2.1	–		V	V_{DD} = 3.0 to 3.6.
V_H	Input hysteresis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA.
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.

Table 11. 2.7V DC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	V_{DD} – 0.4	–	–	V	I_{OH} = 2.5 mA (6.25 Typ), V_{DD} = 2.4 to 3.0 V (16 mA maximum, 50 mA Typ combined I_{OH} budget).
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 10 mA, V_{DD} = 2.4 to 3.0 V (90 mA maximum combined I_{OL} budget).
I_{OH}	High level source current	2.5	–	–	mA	
I_{OL}	Low level sink current	10	–	–	mA	
V_{IL}	Input low level	–	–	0.75	V	V_{DD} = 2.4 to 3.0.
V_{IH}	Input high level	2.0	–	–	V	V_{DD} = 2.4 to 3.0.
V_H	Input hysteresis	–	90	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.

DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ T_A ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

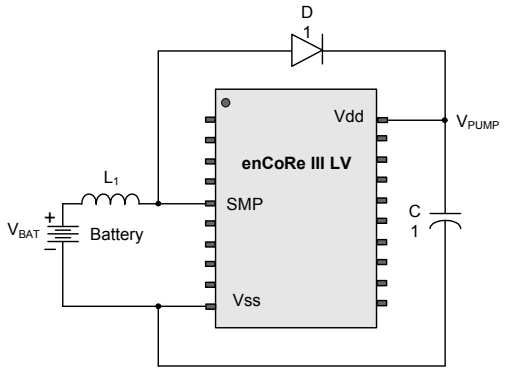
Table 12. 3.3-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	μV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 μA
I_{EBOA00}	Input leakage current (Port 0, Pin 0 analog pin)	–	50	–	nA	Gross tested to 1 μA
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0	–	V_{DD} – 1	V	
G_{OLOA}	Open loop gain	–	80	–	dB	
I_{SOA}	Amplifier supply current	–	10	30	μA	

Table 13. 2.7-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	μV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 μA
I_{EBOA00}	Input leakage current (Port 0, Pin 0 analog pin)	–	50	–	nA	Gross tested to 1 μA
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0	–	V_{DD} – 1	V	
G_{OLOA}	Open loop gain	–	80	–	dB	
I_{SOA}	Amplifier supply current	–	10	30	μA	

Figure 12. Basic Switch Mode Pump Circuit



DC Analog Mux Bus Specifications

Table 15 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ T_A ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70° C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 15. DC Analog Mux Bus Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{SW}	Switch resistance to common analog bus	–	–	400 800	Ω Ω	V_{DD} ≥ 2.7 V 2.4 V ≤ V_{DD} ≤ 2.7 V
R_{VDD}	Resistance of initialization switch to V_{DD}	–	–	800	Ω	

DC POR and LVD Specifications

Table 16 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ T_A ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 16. DC POR and LVD Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{PPOR0} V_{PPOR1}	V_{DD} value for PPOR Trip PORLEV[1:0] = 00b PORLEV[1:0] = 01b	 –	 2.36 2.82	 2.40 2.95	 V V	V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from Watchdog.
	V_{DD} value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b	2.40	2.45	2.51[3]	V	
V_{LVD1}	VM[2:0] = 001b	2.85	2.92	2.99[4]	V	
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD37}	VM[2:0] = 011b	3.06	3.13	3.20	V	
	V_{DD} value for PUMP Trip					
V_{PUMP0}	VM[2:0] = 000b	2.45	2.55	2.62[5]	V	
V_{PUMP1}	VM[2:0] = 001b	2.96	3.02	3.09	V	
V_{PUMP2}	VM[2:0] = 010b	3.03	3.10	3.16	V	
V_{PUMP3}	VM[2:0] = 011b	3.18	3.25	3.32[6]	V	

Notes
3. Always greater than 50 mV above VPPOR (PORLEV = 00) for falling supply.
4. Always greater than 50 mV above VPPOR (PORLEV = 01) for falling supply.
5. Always greater than 50 mV above VLVD0.
6. Always greater than 50 mV above VLVD3.

AC Electrical Characteristics

AC Chip-Level Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ T_A ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 19. 3.3 V AC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
F_{IMO24}	Internal main oscillator frequency for 24 MHz	23.4	24	24.6[10, 11]	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 11 on page 15. SLIMO mode = 0.
F_{IMO6}	Internal main oscillator frequency for 6 MHz	5.5	6	6.5[10, 11]	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 11 on page 15. SLIMO mode = 1.
F_{CPU2}	CPU frequency (3.3 V nominal)	0.093	12	12.3[10, 11]	MHz	SLIMO mode = 0.
F_{BLK33}	Digital block frequency (3.3 V nominal)	0	24	24.6[10, 12]	MHz	
F_{32K1}	Internal low speed oscillator frequency	15	32	64	kHz	
F_{32K_U}	Internal low speed oscillator untrimmed frequency	5	–	100	kHz	
DC_{ILO}	Internal low speed oscillator duty cycle	20	50	80	%	
T_{XRST}	External reset pulse width	10	–	–	µs	
DC24M	24 MHz duty cycle	40	50	60	%	
Step24M	24 MHz Trim step size	–	50	–	kHz	
Fout48M	48 MHz output frequency	46.8	48.0	49.2[11]	MHz	Trimmed. Using factory trim values.
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V / ms	
$T_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	
t_{jit_IMO}	24-MHz IMO cycle-to-cycle jitter (RMS)[13]	–	200	700	ps	
	24-MHz IMO long term N cycle-to-cycle jitter (RMS)[13]	–	300	900	ps	N = 32
	24-MHz IMO period jitter (RMS)[13]	–	100	400	ps	

Notes
10. Accuracy derived from Internal Main Oscillator with appropriate trim for V_{DD} range.
11. 3.0 V < V_{DD} < 3.6 V.
12. See the individual user module data sheets for information on maximum frequencies for user modules.
13. Refer to Cypress Jitter Specifications Application Note AN5054 “Understanding Datasheet Jitter Specifications for Cypress Timing Products” for more information.

AC Digital Block Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ T_A ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 24. 3.3 V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All Functions	Block input clock frequency	–	–	24.6	MHz	3.0 V < V_{DD} < 3.6 V.
Timer/ Counter/ PWM	Enable input pulse width	50[17]	–	–	ns	
	Input clock frequency	–	–	24.6	MHz	
Dead Band	Kill pulse width:					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50	–	–	ns	
	Disable mode	50	–	–	ns	
	Input clock frequency	–	–	24.6	MHz	3.0 V ≤ V_{DD} ≤ 3.6 V.
SPIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock frequency	–	–	4.1	MHz	Note for SPIS Input Clock Frequency: The input clock is the SPI SCLK in SPIS mode.
	Width of SS_ Negated between transmissions	50	–	–	ns	
Transmitter	Input clock frequency	–	–	24.6	MHz	The baud rate is equal to the input clock frequency divided by 8.
Receiver	Input clock frequency	–	–	24.6	MHz	The baud rate is equal to the input clock frequency divided by 8.

Table 25. 2.7 V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All Functions	Block input clock frequency	–	–	12.7	MHz	2.4 V ≤ V_{DD} ≤ 3.0 V.
Timer/ Counter/ PWM	Enable input clock width	100	–	–	ns	
	Input clock frequency	–	–	12.7	MHz	
Dead Band	Kill pulse width:					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	100	–	–	ns	
	Disable mode	100	–	–	ns	
	Input clock frequency	–	–	12.7	MHz	2.4 V ≤ V_{DD} < 3.0 V.
SPIM	Input clock frequency	–	–	6.35	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock frequency	–	–	4.1	MHz	Note for input clock frequency: The input clock is the SPI SCLK in SPIS mode.
	Width of SS_ Negated between transmissions	100	–	–	ns	
Transmitter	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.
Receiver	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.

Note
17. 50 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

AC I²C Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ T_A ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 29. AC Characteristics of the I²C SDA and SCL Pins for V_{DD} ≥ 3.0 V

Parameter	Description	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Set up time for a repeated START condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data hold time	0	–	0	–	µs
$T_{SUDATI2C}$	Data setup time	250	–	100[18]	–	ns
$T_{SUSTOI2C}$	Set up time for STOP condition	4.0	–	0.6	–	µs
T_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns

Table 30. 2.7 V AC Characteristics of the I²C SDA and SCL Pins (Fast-Mode not Supported)

Parameter	Description	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	–	–	kHz
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	–	–	µs
T_{LOWI2C}	LOW period of the SCL clock	4.7	–	–	–	µs
$T_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	–	–	µs
$T_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	–	–	µs
$T_{HDDATI2C}$	Data hold time	0	–	–	–	µs
$T_{SUDATI2C}$	Data setup time	250	–	–	–	ns
$T_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	–	–	µs
T_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	–	–	µs
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	–	–	ns

Note
18. A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU;DAT}$ ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

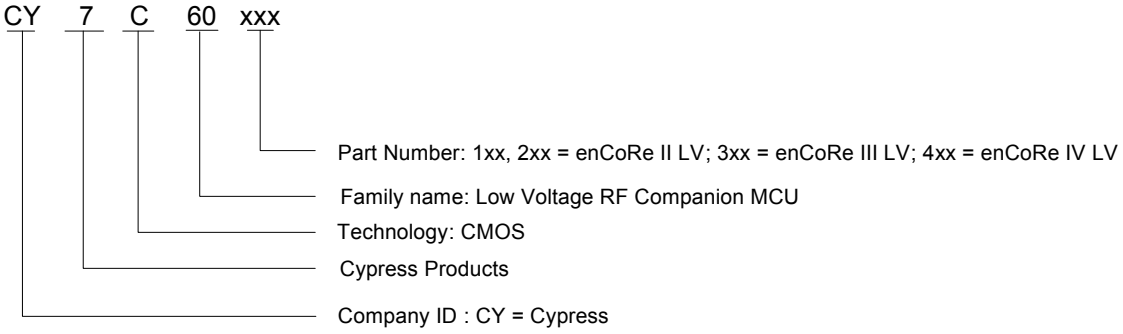
Ordering Information

The following table lists the CY7C603xx device's key package features and ordering codes

Table 33. CY7C603xx Device Key Features and Ordering Information

Package Type	Ordering Part Number	Flash Size	RAM Size	SMP	I/O
28-SSOP	CY7C60323-PVXC	8K	512	No	24
28-SSOP Tape and Reel	CY7C60323-PVXCT	8K	512	No	24
32-QFN SAWN	CY7C60323-LTXC	8K	512	No	28
32-QFN SAWN Tape and Reel	CY7C60323-LTXCT	8K	512	No	28

Ordering Code Definitions



Document Conventions

Units of Measure

Table 35 lists the units of measures.

Table 35. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
kB	1024 bytes	µH	microhenry
dB	decibels	µs	microseconds
°C	degree Celsius	ms	milliseconds
µF	microfarads	ns	nanoseconds
fF	femtofarads	ps	picoseconds
pF	picofarads	µV	microvolts
kHz	kilohertz	mV	millivolts
MHz	megahertz	mVpp	millivolts peak-to-peak
rt-Hz	root hertz	nV	nanovolts
kΩ	kilohms	V	volts
Ω	ohm	µW	microwatts
µA	microamperes	W	watts
mA	milliamperes	mm	millimeter
nA	nanoamperes	ppm	parts per million
pA	pikoamperes	%	percent

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are switched capacitor (SC) and continuous time (CT) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
Application Programming Interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.

Glossary *(continued)*

bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows the user to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.

Glossary *(continued)*

duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
flash	An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I^2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I^2C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls below a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the *slave device*.

Document History Page

Description Title: CY7C603xx, enCoRe™ III Low Voltage Document Number: 38-16018				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	339394	BON	See ECN	New Advance Data Sheet.
*A	399556	BHA	See ECN	Changed from Advance Information to Preliminary. Changed data sheet format. Removed CY7C604xx.
*B	461240	TYJ	See ECN	Modified Figure 10 to include 2.7 V Vdd at 12 MHz operation.
*C	470485	TYJ	See ECN	Corrected part numbers in section 4 to match with part numbers in Ordering Information. From CY7C60323-28PVXC, CY7C60323-56LFXC and CY7C60333-56LFXC to CY7C60323-PVXC, CY7C60323-LFXC and CY7C60333-LFXC respectively. Changed from Preliminary to Final data sheet.
*D	513713	KKVTMP	See ECN	Change title from Wireless enCoRe II to enCoRe III Low Voltage. Applied new template formatting.
*E	2197567	UVS / AESA	See ECN	Added 32-Pin Sawn QFN Pin Diagram, package diagram, and ordering information.
*F	2620679	CMCC / PYRS	12/12/2008	Added Packaging Handling information. Deleted note regarding link to amkor.com for MLF package dimensions.
*G	2852393	XUT	01/15/2010	Added Table of Contents. Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Replaced TRAMP (time) with SRPOWER_UP (slew rate) specification. Added I_{OH}, I_{OL}, DCILO, F32K_U, TPOWERUP, TERASEALL, TPROGRAM_HOT, and TPROGRAM_COLD specifications. Updated copyright and Sales, Solutions, and Legal Information URLs. Updated 28-Pin SSOP and 32-Pin QFN (PUNCH and SAWN) package diagrams.
*H	2892683	NJF	03/15/2010	Updated Cypress website links. Updated Development Kits. Updated 3.3 V AC Chip-Level Specifications and 2.7 V AC Chip-Level Specifications. Removed AC Analog Mux Bus Specs section. Updated 32-pin Sawn QFN package diagram. Removed inactive parts from Ordering Information.
*I	2911952	GNKK	04/13/2010	Updated revision in the footer.
*J	3014656	BHA	09/15/2010	Updated Logic Block Diagram to enCore III LV. Added Ordering Code Definitions Added Acronyms and Units of Measure. Updated to new template.
*K	3114976	NJF	12/19/10	Updated 3.3-V and 2.7-V AC Digital Block Specifications. Updated DC Operational Amplifier Specifications. Updated I^2C Timing Diagram. Added DC I^2C Specifications. Added UILO max limit. Added Tjit_IMO specification, removed existing jitter specifications. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications.
*L	3180466	CSAI	02/23/2011	Updated Packaging Information. Updated to new template.
*M	3210223	CSAI	03/30/2011	Removed prune parts CY7C60333-LTXC and CY7C60333-LTXCT from the datasheet.

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