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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	128KB
RAM Size	16KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 60K Gates, 1536D-Flip-Flops
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a2f060m3e-1fg256m

ProASIC3 FPGA Fabric

The SmartFusion cSoC family, based on the proven, low power, firm-error immune ProASIC®3 flash FPGA architecture, benefits from the advantages only flash-based devices offer:

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, high performance, and ease of use. Flash-based SmartFusion cSoCs are live at power-up and do not need to be loaded from an external boot PROM at each power-up. On-board security mechanisms prevent access to the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system programming (ISP) to support future design iterations and critical field upgrades, with confidence that valuable IP cannot be compromised or copied. Secure ISP can be performed using the industry standard AES algorithm with MAC data authentication on the device.

Low Power

Flash-based SmartFusion cSoCs exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. With SmartFusion cSoCs, there is no power-on current and no high current transition, both of which are common with SRAM-based FPGAs.

SmartFusion cSoCs also have low dynamic power consumption and support very low power time-keeping mode, offering further power savings.

Security

As the nonvolatile, flash-based SmartFusion cSoC family requires no boot PROM, there is no vulnerable external bitstream. SmartFusion cSoCs incorporate FlashLock®, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only a device with nonvolatile flash programming can offer.

SmartFusion cSoCs utilize a 128-bit flash-based key lock and a separate AES key to provide security for programmed IP and configuration data. The FlashROM data in Fusion devices can also be encrypted prior to loading. Additionally, the flash memory blocks can be programmed during runtime using the AES-128 block cipher encryption standard (FIPS Publication 192).

SmartFusion cSoCs with AES-based security are designed to provide protection for remote field updates over public networks, such as the Internet, and help to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. As an additional security measure, the FPGA configuration data of a programmed Fusion device cannot be read back, although secure design verification is possible. During design, the user controls and defines both internal and external access to the flash memory blocks.

Security, built into the FPGA fabric, is an inherent component of the SmartFusion cSoC family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. SmartFusion cSoCs, with FlashLock and AES security, are unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry standard security measures, making remote ISP feasible. A SmartFusion cSoC provides the highest security available for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based SmartFusion cSoCs do not require system configuration components such as electrically erasable programmable read-only memories (EEPROMs) or microcontrollers to load device configuration data during power-up. This reduces bill-of-materials costs and PCB area, and increases system security and reliability.

Live at Power-Up

Flash-based SmartFusion cSoCs are live at power-up (LAPU). LAPU SmartFusion cSoCs greatly simplify total system design and reduce total system cost by eliminating the need for complex programmable logic devices (CPLDs). SmartFusion LAPU clocking (PLLs) replace off-chip clocking resources. In addition, glitches and brownouts in system power will not corrupt the SmartFusion flash configuration. Unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables reduction or complete removal of expensive voltage monitor and brownout

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the A2F500-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

where

θ_{JA} = 18.6°C/W (taken from Table 2-6 on page 2-7).

T_A = 75.00°C

$$\text{Maximum Power Allowed} = \frac{100.00°C - 75.00°C}{18.6°C/W} = 1.61\ W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

Calculation for Heat Sink

For example, in a design implemented in an A2F500-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent T_a and T_j are given as follows:

T_J = 100.00°C

T_A = 70.00°C

From the datasheet:

θ_{JA} = 16.4°C/W

θ_{JC} = 7.5°C/W

Power Consumption of Various Internal Resources

Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs

Parameter	Definition	Power Supply		Device		Units
		Name	Domain	A2F060	A2F500	
PAC1	Clock contribution of a Global Rib	VCC	1.5 V	3.39	5.05	µW/MHz
PAC2	Clock contribution of a Global Spine	VCC	1.5 V	1.14	2.50	µW/MHz
PAC3	Clock contribution of a VersaTile row	VCC	1.5 V	1.15	1.15	µW/MHz
PAC4	Clock contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.12	0.12	µW/MHz
PAC5	First contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.07	0.07	µW/MHz
PAC6	Second contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.29	0.29	µW/MHz
PAC7	Contribution of a VersaTile used as a combinatorial module	VCC	1.5 V	0.29	0.29	µW/MHz
PAC8	Average contribution of a routing net	VCC	1.5 V	1.04	0.79	µW/MHz
PAC9	Contribution of an I/O input pin (standard dependent)	VCCxxxxIOBx/VCC	See Table 2-10 and Table 2-11 on page 2-11			
PAC10	Contribution of an I/O output pin (standard dependent)	VCCxxxxIOBx/VCC	See Table 2-12 and Table 2-13 on page 2-12			
PAC11	Average contribution of a RAM block during a read operation	VCC	1.5 V	25.00		µW/MHz
PAC12	Average contribution of a RAM block during a write operation	VCC	1.5 V	30.00		µW/MHz
PAC13	Dynamic Contribution for PLL	VCC	1.5 V	2.60		µW/MHz
PAC15	Contribution of NVM block during a read operation (F < 33MHz)	VCC	1.5 V	358.00		µW/MHz
PAC16	1st contribution of NVM block during a read operation (F > 33MHz)	VCC	1.5 V	12.88		mW
PAC17	2nd contribution of NVM block during a read operation (F > 33MHz)	VCC	1.5 V	4.80		µW/MHz
PAC18	Main Crystal Oscillator contribution	VCCMAINXTAL	3.3 V	1.98		mW
PAC19a	RC Oscillator contribution	VCCRCOSC	3.3 V	3.30		mW
PAC19b	RC Oscillator contribution	VCC	1.5 V	3.00		mW
PAC20a	Analog Block Dynamic Power Contribution of the ADC	VCC33ADCx	3.3 V	8.25		mW
PAC20b	Analog Block Dynamic Power Contribution of the ADC	VCC15ADCx	1.5 V	3.00		mW
PAC21	Low Power Crystal Oscillator contribution	VCCLPXTAL	3.3 V	33.00		µW
PAC22	MSS Dynamic Power Contribution – Running Drysthone at 100MHz[1]	VCC	1.5 V	67.50		mW
PAC23	Temperature Monitor Power Contribution	See Table 2-94 on page 2-79	–	1.23		mW
PAC24	Current Monitor Power Contribution	See Table 2-93 on page 2-78	–	1.03		mW

P_{PLL} = 0 W

Embedded Nonvolatile Memory Dynamic Contribution—P_{eNVM}

SoC Mode

The eNVM dynamic power consumption is a piecewise linear function of frequency.

$P_{eNVM} = N_{eNVM\text{-}BLOCKS} * \beta_4 * P_{AC15} * F_{READ\text{-}eNVM}$ when $F_{READ\text{-}eNVM} \leq 33$ MHz,

$P_{eNVM} = N_{eNVM\text{-}BLOCKS} * \beta_4 * (P_{AC16} + P_{AC17} * F_{READ\text{-}eNVM})$ when $F_{READ\text{-}eNVM} > 33$ MHz

Where:

$N_{eNVM\text{-}BLOCKS}$ is the number of eNVM blocks used in the design.

β_4 is the eNVM enable rate for read operations. Default is 0 (eNVM mainly in idle state).

$F_{READ\text{-}eNVM}$ is the eNVM read clock frequency.

Standby Mode and Time Keeping Mode

P_{eNVM} = 0 W

Main Crystal Oscillator Dynamic Contribution—$P_{XTL\text{-}OSC}$

SoC Mode

$P_{XTL\text{-}OSC} = P_{AC18}$

Standby Mode

$P_{XTL\text{-}OSC}$ = 0 W

Time Keeping Mode

$P_{XTL\text{-}OSC}$ = 0 W

Low Power Oscillator Crystal Dynamic Contribution—$P_{LPXTAL\text{-}OSC}$

Operating, Standby, and Time Keeping Mode

$P_{LPXTAL\text{-}OSC} = P_{AC21}$

RC Oscillator Dynamic Contribution—$P_{RC\text{-}OSC}$

SoC Mode

$P_{RC\text{-}OSC} = P_{AC19A} + P_{AC19B}$

Standby Mode and Time Keeping Mode

$P_{RC\text{-}OSC}$ = 0 W

Analog System Dynamic Contribution—P_{AB}

SoC Mode

$P_{AB} = P_{AC23} * N_{TM} + P_{AC24} * N_{CM} + P_{AC25} * N_{ABPS} + P_{AC26} * N_{SDD} + P_{AC27} * N_{COMP} + P_{ADC} * N_{ADC} + P_{VR}$

Where:

N_{CM} is the number of current monitor blocks

N_{TM} is the number of temperature monitor blocks

N_{SDD} is the number of sigma-delta DAC blocks

N_{ABPS} is the number of ABPS blocks

N_{ADC} is the number of ADC blocks

N_{COMP} is the number of comparator blocks

$P_{VR} = P_{AC28}$

$P_{ADC} = P_{AC20A} + P_{AC20B}$

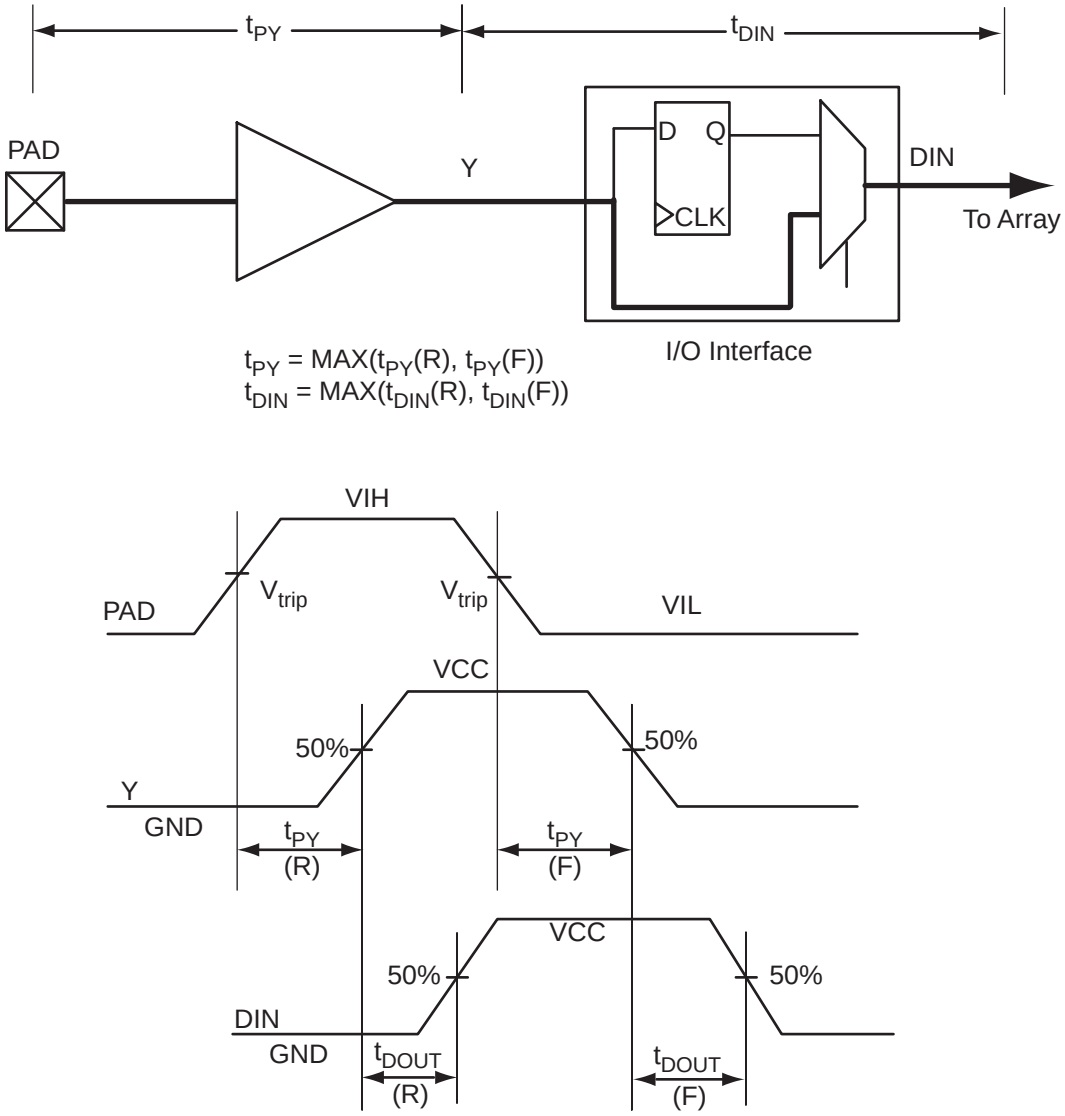

Figure 2-4 • Input Buffer Timing Model and Delays (example)

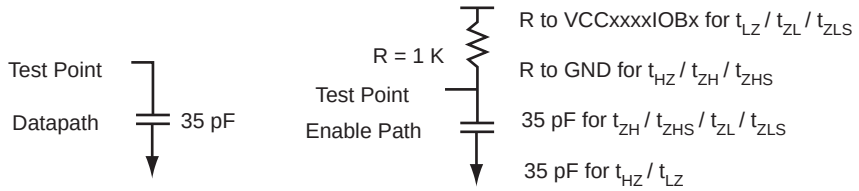

Figure 2-7 • AC Loading

Table 2-38 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	35

Note: *Measuring point = V_{trip}. See Table 2-22 on page 2-25 for a complete table of trip points.

Timing Characteristics

Table 2-45 • 2.5 V LVCMOS High Slew
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 2.3 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.57	8.67	0.04	1.32	0.41	7.89	8.67	2.72	2.32	10.09	10.87	ns
	–1	0.47	7.22	0.03	1.10	0.34	6.57	7.22	2.27	1.94	8.41	9.06	ns
8 mA	Std.	0.57	5.19	0.04	1.32	0.41	5.10	5.19	3.11	3.03	7.30	7.40	ns
	–1	0.47	4.33	0.03	1.10	0.34	4.25	4.33	2.59	2.52	6.09	6.16	ns
12 mA	Std.	0.62	3.64	0.04	1.32	0.41	3.71	3.46	3.37	3.47	5.91	5.66	ns
	–1	0.52	3.03	0.03	1.10	0.34	3.09	2.88	2.81	2.90	4.93	4.72	ns
16 mA	Std.	0.62	3.44	0.04	1.32	0.41	3.50	3.09	3.43	3.59	5.70	5.29	ns
	–1	0.52	2.86	0.03	1.10	0.34	2.92	2.57	2.85	2.99	4.75	4.41	ns
24 mA	Std.	0.62	3.16	0.04	1.32	0.41	3.22	2.48	3.50	4.03	5.43	4.68	ns
	–1	0.52	2.64	0.03	1.10	0.34	2.68	2.06	2.92	3.35	4.52	3.90	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-46 • 2.5 V LVCMOS Low Slew
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 2.3 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.57	11.25	0.04	1.32	0.41	11.45	11.25	2.72	2.22	13.65	13.45	ns
	–1	0.47	9.37	0.03	1.10	0.34	9.54	9.37	2.27	1.85	11.37	11.21	ns
8 mA	Std.	0.57	8.15	0.04	1.32	0.41	8.30	7.73	3.11	2.92	10.50	9.94	ns
	–1	0.47	6.79	0.03	1.10	0.34	6.92	6.44	2.59	2.43	8.75	8.28	ns
12 mA	Std.	0.62	6.34	0.04	1.32	0.41	6.46	5.91	3.37	3.36	8.66	8.11	ns
	–1	0.52	5.28	0.03	1.10	0.34	5.38	4.92	2.81	2.80	7.22	6.76	ns
16 mA	Std.	0.62	5.92	0.04	1.32	0.41	6.03	5.52	3.42	3.48	8.23	7.72	ns
	–1	0.52	4.93	0.03	1.10	0.34	5.02	4.60	2.85	2.90	6.86	6.43	ns
24 mA	Std.	0.62	5.55	0.04	1.32	0.41	5.65	5.51	3.50	3.90	7.86	7.71	ns
	–1	0.52	4.62	0.03	1.10	0.34	4.71	4.59	2.92	3.25	6.55	6.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-47 • 2.5 V LVCMOS High Slew
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 2.3 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
8 mA	Std.	0.23	2.52	0.09	1.27	1.49	0.23	2.57	2.34	2.34	2.48	ns
	–1	0.19	2.10	0.08	1.06	1.24	0.19	2.14	1.95	1.95	2.07	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Timing Characteristics

Table 2-51 • 1.8 V LVCMOS High Slew
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.62	11.85	0.04	1.22	0.41	9.22	11.85	2.80	1.70	11.42	14.05	ns
	–1	0.52	9.87	0.03	1.02	0.34	7.68	9.87	2.33	1.42	9.52	11.71	ns
4 mA	Std.	0.62	6.91	0.04	1.22	0.41	5.92	6.91	3.26	2.85	8.13	9.12	ns
	–1	0.52	5.76	0.03	1.02	0.34	4.94	5.76	2.72	2.38	6.77	7.60	ns
6 mA	Std.	0.62	4.46	0.04	1.22	0.41	4.27	4.46	3.58	3.40	6.48	6.66	ns
	–1	0.52	3.71	0.03	1.02	0.34	3.56	3.71	2.98	2.84	5.40	5.55	ns
8 mA	Std.	0.62	3.95	0.04	1.22	0.41	4.02	3.93	3.65	3.55	6.23	6.14	ns
	–1	0.52	3.29	0.03	1.02	0.34	3.35	3.28	3.04	2.96	5.19	5.12	ns
12 mA	Std.	0.62	3.62	0.04	1.22	0.41	3.68	3.06	3.75	4.09	5.89	5.26	ns
	–1	0.52	3.01	0.03	1.02	0.34	3.07	2.55	3.12	3.41	4.91	4.39	ns
16 mA	Std.	0.62	3.62	0.04	1.22	0.41	3.68	3.06	3.75	4.09	5.89	5.26	ns
	–1	0.52	3.01	0.03	1.02	0.34	3.07	2.55	3.12	3.41	4.91	4.39	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-52 • 1.8 V LVCMOS Low Slew
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.62	15.25	0.04	1.22	0.41	14.43	15.25	2.80	1.65	16.63	17.46	ns
	–1	0.52	12.71	0.03	1.02	0.34	12.02	12.71	2.34	1.37	13.86	14.55	ns
4 mA	Std.	0.62	10.43	0.04	1.22	0.41	10.62	10.31	3.27	2.75	12.82	12.51	ns
	–1	0.52	8.69	0.03	1.02	0.34	8.85	8.59	2.72	2.29	10.69	10.42	ns
6 mA	Std.	0.62	8.21	0.04	1.22	0.41	8.36	7.75	3.58	3.30	10.57	9.96	ns
	–1	0.52	6.84	0.03	1.02	0.34	6.97	6.46	2.98	2.75	8.81	8.30	ns
8 mA	Std.	0.62	7.66	0.04	1.22	0.41	7.80	7.22	3.65	3.44	10.01	9.43	ns
	–1	0.52	6.38	0.03	1.02	0.34	6.50	6.02	3.04	2.87	8.34	7.86	ns
12 mA	Std.	0.62	7.24	0.04	1.22	0.41	7.38	7.23	3.75	3.96	9.58	9.43	ns
	–1	0.52	6.04	0.03	1.02	0.34	6.15	6.02	3.13	3.30	7.98	7.86	ns
16 mA	Std.	0.62	7.24	0.04	1.22	0.41	7.38	7.23	3.75	3.96	9.58	9.43	ns
	–1	0.52	6.04	0.03	1.02	0.34	6.15	6.02	3.13	3.30	7.98	7.86	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Input Register

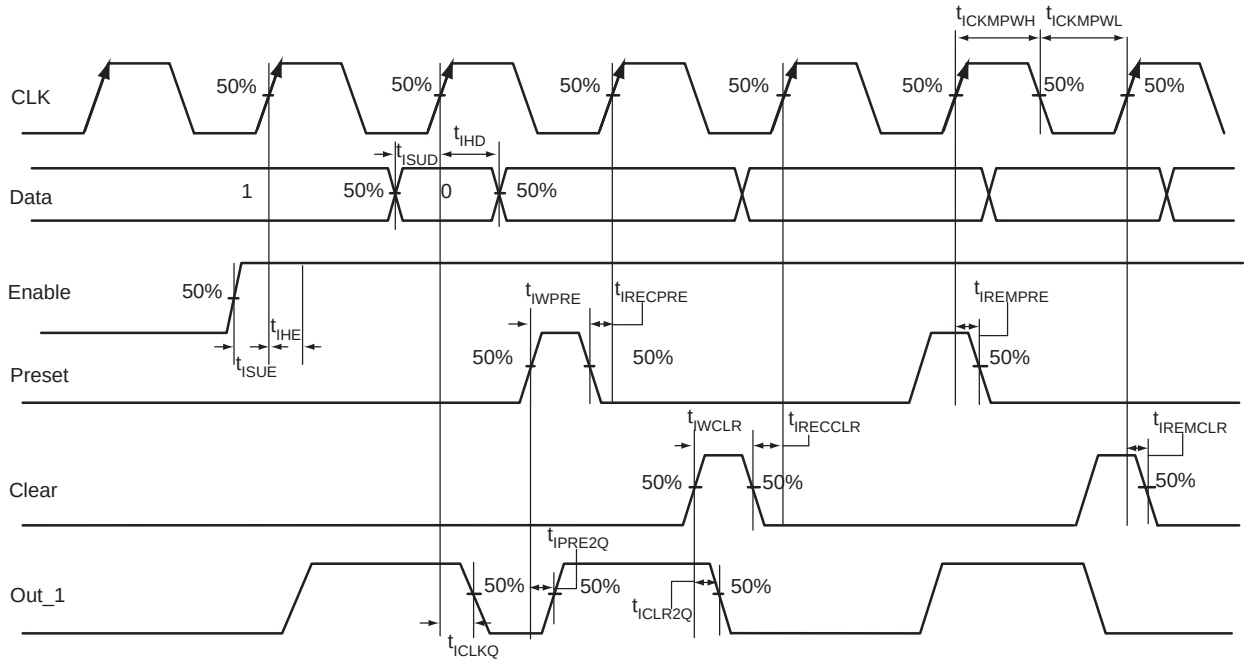

Figure 2-17 • Input Register Timing Diagram

Timing Characteristics

Table 2-72 • Input Data Register Propagation Delays
Worst Military-Case Conditions: T J = 125°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.25	0.30	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.28	0.33	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.39	0.47	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.48	0.58	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.48	0.58	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	0.28	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	0.28	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.26	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.26	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.42	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.32	0.38	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The SmartFusion library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide.

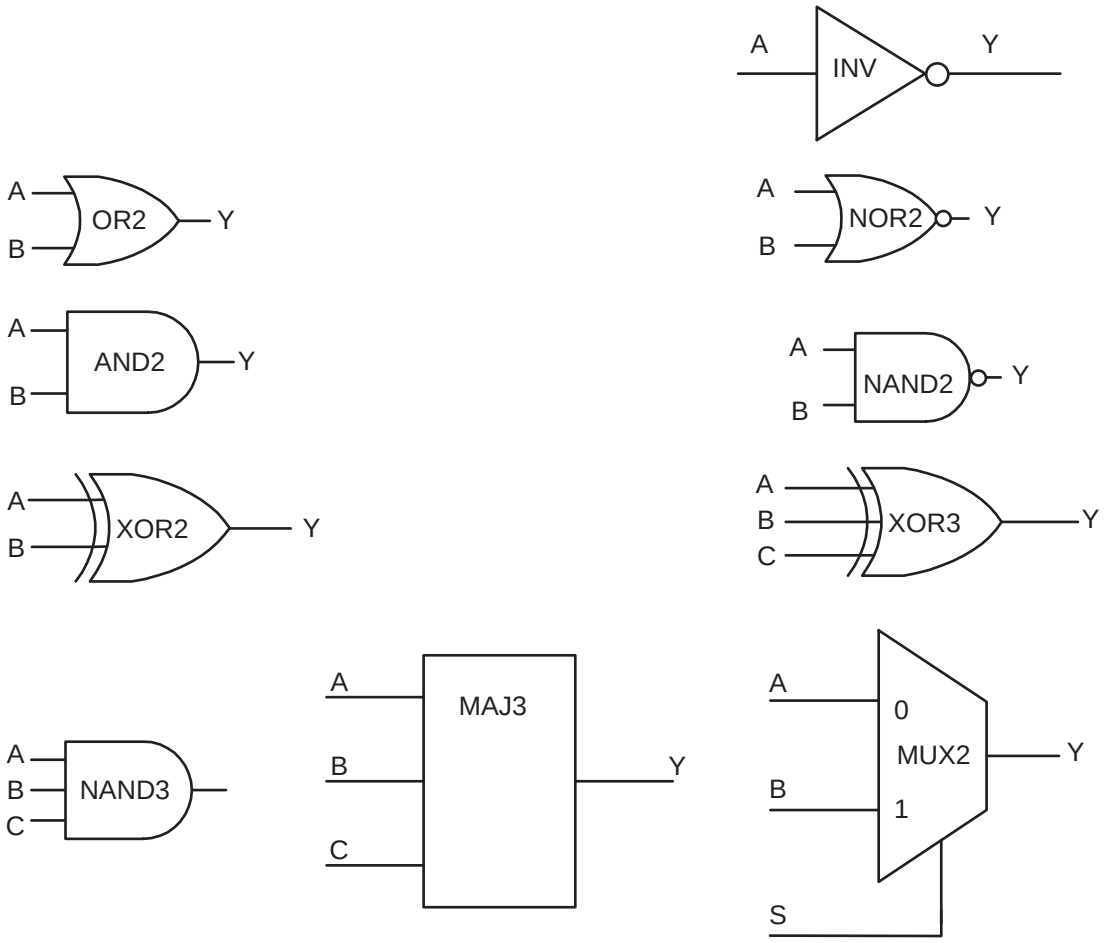

Figure 2-24 • Sample of Combinatorial Cells

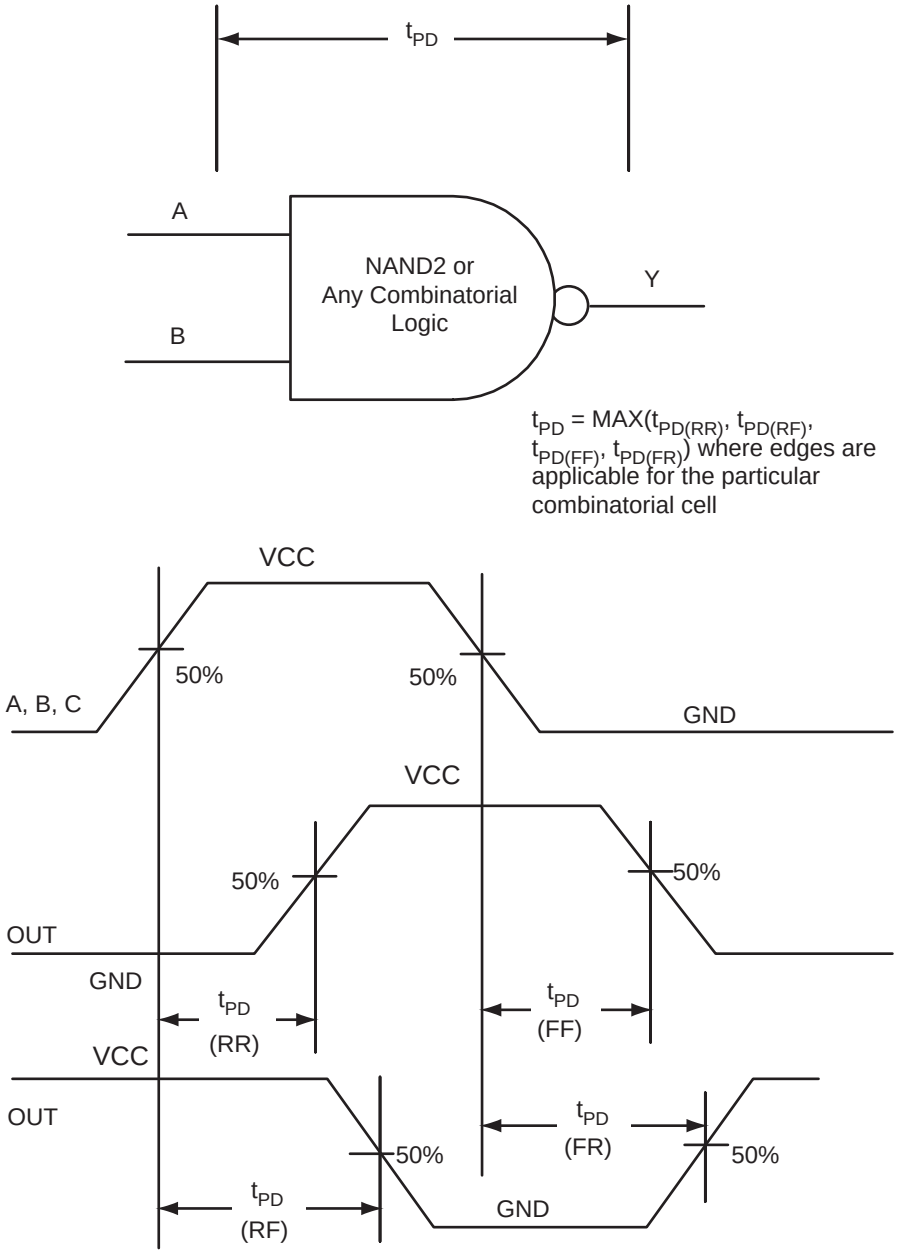

Figure 2-25 • Timing Model and Waveforms

Embedded FlashROM (eFROM)

Electrical Characteristics

Table 2-91 describes the eFROM maximum performance

Table 2-91 • FlashROM Access Time, Worse Military-Case Conditions: T_J = 125°C, VCC = 1.425 V

Parameter	Description	–1	Std.	Units
F_{max}	Maximum Clock frequency	15.00	15.00	MHz

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-20 for more details.

Timing Characteristics

Table 2-92 • JTAG 1532
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.53	0.63	ns
t_{DIHD}	Test Data Input Hold Time	1.07	1.25	ns
t_{TMSSU}	Test Mode Select Setup Time	0.53	0.63	ns
t_{TMDHD}	Test Mode Select Hold Time	1.07	1.25	ns
t_{TCK2Q}	Clock to Q (data out)	5.33	6.27	ns
t_{RSTB2Q}	Reset to Q (data out)	21.31	25.07	ns
F_{TCKMAX}	TCK Maximum Frequency	26.00	30.59	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.00	0.00	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.21	0.25	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-95 • ADC Specifications (continued)

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input leakage current	–40°C to +100°C		1		µA
Power supply rejection ratio	DC	44	53		dB
ADC power supply operational current requirements	VCC33ADCx			2.5	mA
	VCC15A			2	mA

Note: All 3.3 V supplies are tied together and varied from 3.0 V to 3.6 V. 1.5 V supplies are held constant.

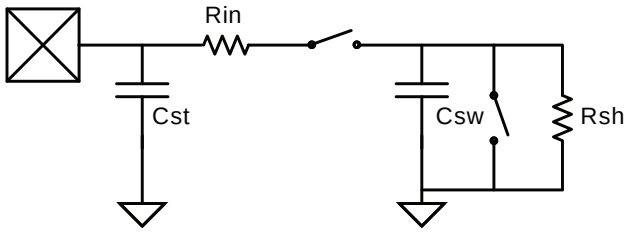

Figure 2-43 • ADC Input Model

Table 2-96 • VAREF Stabilization Time

VAREF Capacitor Value (µF)	Required Settling Time for 8-Bit and 10-Bit Mode (ms)	Required Settling Time for 12-Bit Mode (ms)
0.01	1	1
0.1	3	4
0.2	6	8
0.3	10	11
0.5	17	20
0.7	18	21
1	32	37
2.2	62	73
3.3	99	117
10	275	325
22	635	751
47	1318	1557

Analog Sigma-Delta Digital to Analog Converter (DAC)

Unless otherwise noted, sigma-delta DAC performance is specified at 25°C with nominal power supply voltages, using the internal sigma-delta modulators with 16-bit inputs, HCLK = 100 MHz, modulator inputs updated at a 100 KHz rate, in voltage output mode with an external 160 pF capacitor to ground, after trimming and digital [pre-]compensation.

Table 2-99 • Analog Sigma-Delta DAC

Specification	Test Conditions	Min.	Typ.	Max.	Units
Resolution		8		24	Bits
Output range			0 to 2.56		V
	Current output mode		0 to 256		µA
Output Impedance		6	10	12	KΩ
	Current output mode	10			MΩ
Output voltage compliance	Current output mode		0–3.0		V
	–40ºC to +100ºC	0–2.7		0–3.4	V
Gain error	Voltage output mode		0.3	±2	%
	–40ºC to +100ºC		0.3	±2	%
	–55ºC to +125ºC		0.3	±6	%
	Current output mode		0.3	±2	%
	–40ºC to +100ºC		0.3	±2	%
	–55ºC to +125ºC		0.3	±6	%
Output referred offset	DACBYTE0 = h'00 (8-bit)		0.25	±1	mV
	–40ºC to +100ºC		1	±2.5	mV
	Current output mode		0.3	±1	µA
	–40ºC to +100ºC		1	±2.5	µA
Integral non-linearity	RMS deviation from BFSL		0.1	0.4	% FS*
Differential non-linearity			0.05	0.4	% FS*
Analog settling time			Refer to Figure 2-44 on page 2-87		µs
Power supply rejection ratio	DC, full scale output	33	34		dB

Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.

Re-Programming the eNVM Bl ocks Using the Cortex-M3

In this mode the Cortex-M3 is executing the eNVM programming algorithm from eSRAM. Since individual pages (132 bytes) of the eNVM can be write-protected, the programming algorithm software can be protected from inadvertent erasure. When reprogramming the eNVM, both MSS I/Os and FPGA I/Os are available as interfaces for sourcing the new eNVM image. The SoC Products Group provides working example projects for SoftConsole, IAR, and Keil development environments. These can be downloaded via the SoC Products Group Firmware Catalog.

Alternately, the eNVM can be reprogrammed by the Cortex-M3 via the IAP driver. This is necessary when using an encrypted image.

Secure Programming

For background, refer to the "Security in Low Power Flash Devices" chapter of the Fusion FPGA Fabric User's Guide on the SoC Products Group website. SmartFusion ISP behaves identically to Fusion ISP. IAP of SmartFusion cSoCs is accomplished by using the IAP driver. Only the FPGA fabric and the eNVM can be reprogrammed with the protection of security measures by using the IAP driver.

Typical Programming and Erase Times

Table 4-3 documents the typical programming and erase times for two components of SmartFusion cSoCs, FPGA fabric and eNVM, using the SoC Products Group's FlashPro hardware and software. These times will be different for other ISP and IAP methods. The Program action in FlashPro software includes erase, program, and verify to complete.

The typical programming (including erase) time per page of the eNVM is 8 ms.

Table 4-3 • Typical Programming and Erase Times

	FPGA Fabric (seconds)	eNVM (seconds)
Device	A2F500	A2F500
Erase	21	N/A
Program	15	26
Verify	16	42

References

User's Guides

DirectC User's Guide

http://www.microsemi.com/soc/documents/DirectC_UG.pdf

Fusion FPGA Fabric User's Guide

http://www.microsei.com/soc/documents/Fusion_UG.pdf

Chapters:

"In-System Programming (ISP) of Actel's Low-Power Flash Devices Using FlashPro4/3/3X"

"Security in Low Power Flash Devices"

"Programming Flash Devices"

"Microprocessor Programming of Actel's Low-Power Flash Devices"

JTAG Pins

SmartFusion cSoCs have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the SmartFusion cSoC part must be supplied to allow JTAG signals to transition the SmartFusion cSoC. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRSTB pin could be tied to GND.

Name	Type	Polarity/ Bus Size	Description
JTAGSEL	In	1	JTAG controller selection Depending on the state of the JTAGSEL pin, an external JTAG controller will either see the FPGA fabric TAP/auxiliary TAP (High) or the Cortex-M3 JTAG debug interface (Low). The JTAGSEL pin should be connected to an external pull-up resistor such that the default configuration selects the FPGA fabric TAP.
TCK	In	1	Test clock Serial input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, it is recommended to tie off TCK to GND or V_{JTAG} through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state. Note that to operate at all V_{JTAG} voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 5-1 on page 5-10 for more information. Can be left floating when unused.
TDI	In	1	Test data Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.
TDO	Out	1	Test data Serial output for JTAG boundary scan, ISP, and UJTAG usage.
TMS	In	HIGH	Test mode select The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin. Can be left floating when unused.
TRSTB	In	HIGH	Boundary scan reset pin The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the TAP is held in reset mode. The resistor values must be chosen from Table 5-1 on page 5-10 and must satisfy the parallel resistance value requirement. The values in Table 5-1 on page 5-10 correspond to the resistor recommended when a single device is used. The values correspond to the equivalent parallel resistor when multiple devices are connected via a JTAG chain. In critical applications, an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases, it is recommended that you tie off TRST to GND through a resistor placed close to the FPGA pin. The TRSTB pin also resets the serial wire JTAG – debug port (SWJ-DP) circuitry within the Cortex-M3. Can be left floating when unused.

Name	Type	Description	Associated With	
			ADC/SDD	SCB
TM0	In	SCB 0 / low side of current monitor / comparator Negative input / high side of temperature monitor. See the Temperature Monitor section.	ADC0	SCB0
TM1	In	SCB 1 / low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC0	SCB1
TM2	In	SCB 2 / low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC1	SCB2
TM3	In	SCB 3 low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC1	SCB3
TM4	In	SCB 4 low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC2	SCB4
SDD0	Out	Output of SDD0 See the Sigma-Delta Digital-to-Analog Converter (DAC) section in the SmartFusion Programmable Analog User's Guide.	SDD0	N/A
SDD1	Out	Output of SDD1	SDD1	N/A
SDD2	Out	Output of SDD2	SDD2	N/A

Note: Unused analog inputs should be grounded. This aids in shielding and prevents an undesired coupling path.

Table 5-2 • Relationships Between Signal s in the Analog Front-End

Pin	ADC Channel	Dir.-In Option	Prescaler	Current Mon.	Temp. Mon.	Compar.	LVTTL	SDD MUX	SDD
SDD2	ADC2_CH15								SDD2_OUT
TM0	ADC0_CH4	Yes		CM0_L	TM0_IO	CMP0_N			
TM1	ADC0_CH8	Yes		CM1_L	TM1_IO	CMP2_N			
TM2	ADC1_CH4	Yes		CM2_L	TM2_IO	CMP4_N			
TM3	ADC1_CH8	Yes		CM3_L	TM3_IO	CMP6_N			
TM4	ADC2_CH4	Yes		CM4_L	TM4_IO	CMP8_N			

Notes:

1. ABPSx_IN: Input to active bipolar prescaler channel x.
2. CMx_H/L: Current monitor channel x, high/low side.
3. TMx_IO: Temperature monitor channel x.
4. CMPx_P/N: Comparator channel x, positive/negative input.
5. LVTTLx_IN: LVTTL I/O channel x.
6. SDDMx_OUT: Output from sigma-delta DAC MUX channel x.
7. SDDx_OUT: Direct output from sigma-delta DAC channel x.

Pin No.	FG256	
	A2F060 Function	A2F500 Function
L6	GND	GND
L7	VCC	VCC
L8	GND	GND
L9	VCC	VCC
L10	GND	GND
L11	VCCMSSIOB2	VCCMSSIOB2
L12	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24
L13	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27
L14	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26
L15	SPI_1_DI/GPIO_25	SPI_1_DI/GPIO_25
L16	GND	GND
M1	GPIO_5/IO28RSB4V0	MAC_TXD[0]/IO65RSB4V0
M2	GPIO_6/IO27RSB4V0	MAC_TXD[1]/IO64RSB4V0
M3	GPIO_7/IO26RSB4V0	MAC_RXD[0]/IO63RSB4V0
M4	GND	GND
M5	NC	ADC3
M6	NC	GND15ADC0
M7	GND33ADC0	GND33ADC1
M8	GND33ADC0	GND33ADC1
M9	ADC7	ADC4
M10	GNDTM0	GNDTM1
M11	ADC6	TM2
M12	ADC5	CM2
M13	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19
M14	VCCMSSIOB2	VCCMSSIOB2
M15	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18
M16	SPI_0_DI/GPIO_17	SPI_0_DI/GPIO_17
N1	GPIO_8/IO25RSB4V0	MAC_RXD[1]/IO62RSB4V0
N2	VCCMSSIOB4	VCCMSSIOB4
N3	VCC15A	VCC15A
N4	VCC33AP	VCC33AP
N5	NC	ABPS3
N6	ADC4	TM1

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin No.	FG256	
	A2F060 Function	A2F500 Function
R8	VCC15ADC0	VCC15ADC1
R9	ADC10	ADC7
R10	ABPS1	ABPS7
R11	NC	ABPS4
R12	MAINXIN	MAINXIN
R13	MAINXOUT	MAINXOUT
R14	LPXIN	LPXIN
R15	LPXOUT	LPXOUT
R16	VCC33A	VCC33A
T1	NCAP	NCAP
T2	ADC1	ABPS1
T3	ADC2	CM0
T4	NC	GNDTM0
T5	NC	ADC0
T6	NC	VAREF0
T7	NC	GND33ADC0
T8	GND15ADC0	GND15ADC1
T9	VAREF0	VAREF1
T10	ABPS0	ABPS6
T11	NC	ABPS5
T12	NC	SDD1
T13	GNDVAREF	GNDVAREF
T14	GNDMAINXTAL	GNDMAINXTAL
T15	VCCLPXTAL	VCCLPXTAL
T16	PU_N	PU_N

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.