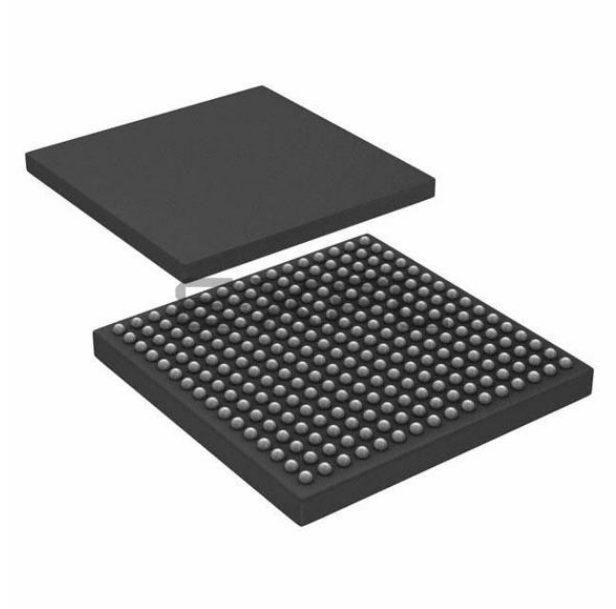

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	128KB
RAM Size	16KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 60K Gates, 1536D-Flip-Flops
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a2f060m3e-1fgg256m

Power per I/O Pin

Table 2-10 • **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins**

	VCCFPGAIOBx (V)	Static Power PDC7 (mW)	Dynamic Power PAC9 (µW/MHz)
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	17.55
2.5 V LVCMOS	2.5	–	5.97
1.8 V LVCMOS	1.8	–	2.88
1.5 V LVCMOS (JESD8-11)	1.5	–	2.33
3.3 V PCI	3.3	–	19.21
3.3 V PCI-X	3.3	–	19.21
Differential			
LVDS	2.5	2.25	0.82
LVPECL	3.3	5.74	1.16

Table 2-11 • **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to MSS I/O Banks**

	VCCMSSIOBx (V)	Static Power PDC7 (mW)	Dynamic Power PAC9 (µW/MHz)
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	17.21
3.3 V LVCMOS / 3.3 V LVCMOS – Schmitt trigger	3.3	–	20.00
2.5 V LVCMOS	2.5	–	5.55
2.5 V LVCMOS – Schmitt trigger	2.5	–	7.03
1.8 V LVCMOS	1.8	–	2.61
1.8 V LVCMOS – Schmitt trigger	1.8	–	2.72
1.5 V LVCMOS (JESD8-11)	1.5	–	1.98
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	1.93

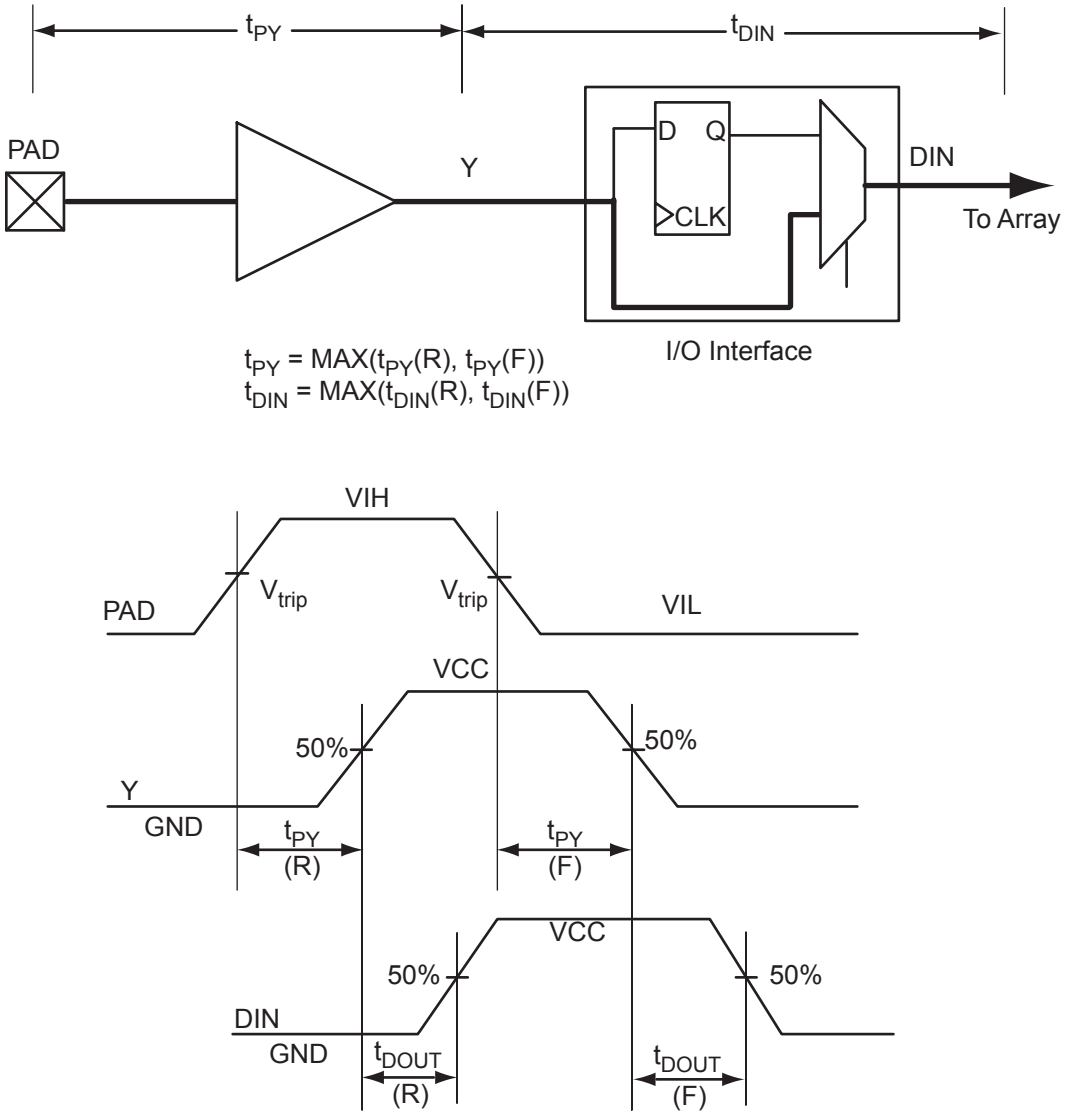

Figure 2-4 • **Input Buffer Timing Model and Delays (example)**

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-19 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Military Conditions—Software Default Settings Applicable to FPGA I/O Banks

I/O Standard	Drive Strgth.	Slew Rate	VIL		VIH		VOL	VOH	IOL[1]	IOH[1]
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * VCCxxxxIOBx	0.65* VCCxxxxIOBx	3.6	0.45	VCCxxxxIOBx – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * VCCxxxxIOBx	0.65* VCCxxxxIOBx	3.6	0.25 * VCCxxxxIOBx	0.75* VCCxxxxIOBx	12	12
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Notes:

1. *Currents are measured at 125°C junction temperature.*
2. *Output slew rate can be extracted by the IBIS Models.*

Table 2-20 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Military Conditions—Software Default Settings Applicable to MSS I/O Banks

I/O Standard	Drive Strgth.	Slew Rate	VIL		VIH		VOL	VOH	IOL[1]	IOH[1]
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	–0.3	0.8	2	3.6	0.4	2.4	8	8
2.5 V LVCMOS	8 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8 V LVCMOS	4 mA	High	–0.3	0.35* VCCxxxxIOBx	0.65* VCCxxxxIOBx	3.6	0.45	VCCxxxxIOBx – 0.45	4	4
1.5 V LVCMOS	2 mA	High	–0.3	0.35* VCCxxxxIOBx	0.65* VCCxxxxIOBx	3.6	0.25* VCCxxxxIOBx	0.75* VCCxxxxIOBx	2	2

Notes:

1. *Currents are measured at 125°C junction temperature.*
2. *Output slew rate can be extracted by the IBIS Models.*

Table 2-30 • I/O Short Currents IOSH/IOSL Applicable to FPGA I/O Banks

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	127	132
	24 mA	181	268
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
	16 mA	87	83
	24 mA	124	169
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	51	45
	12 mA	74	91
	16 mA	74	91
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
	6 mA	39	32
	8 mA	55	66
	12 mA	55	66
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

*Note: *T_J = 100°C.*

Table 2-31 • I/O Short Currents IOSH/IOSL Applicable to MSS I/O Banks

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	54	51
2.5 V LVCMOS	8 mA	37	32
1.8 V LVCMOS	4 mA	22	17
1.5 V LVCMOS	2 mA	16	13

*Note: *T_J = 100°C*

Table 2-53 • 1.8 V LVCMOS High Slew
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
4 mA	Std.	0.23	2.97	0.09	1.17	1.75	0.23	3.02	2.92	2.36	2.41	ns
	–1	0.19	2.47	0.08	0.98	1.46	0.19	2.52	2.43	1.97	2.00	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by SoC Products Group Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-12. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, SmartFusion cSoCs also support bus LVDS structure and multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

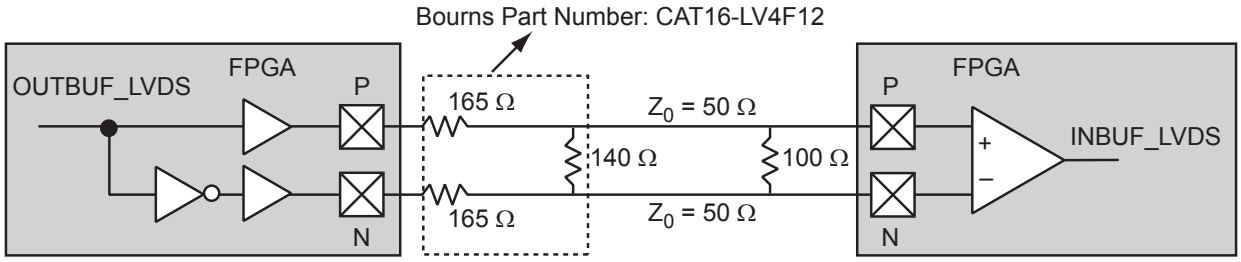

Figure 2-12 • **LVDS Circuit Diagram and Board-Level Implementation**

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-14. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

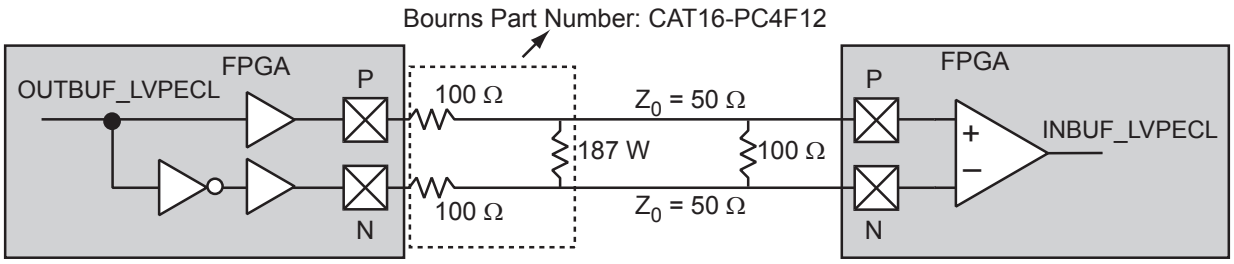

Figure 2-14 • **LVPECL Circuit Diagram and Board-Level Implementation**

Table 2-67 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCFPGAIOBx	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

Table 2-68 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.64	1.94	Cross point	–

*Note: *Measuring point = Vtrip. See Table 2-22 on page 2-25 for a complete table of trip points.*

Timing Characteristics

Table 2-69 • **LVPECL**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCFPGAIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.62	1.88	0.04	1.38	ns
–1	0.52	1.57	0.03	1.15	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Main and Lower Power Crystal Oscillator

The tables below describes the electrical characteristics of the main and low power crystal oscillator.

Table 2-84 • **Electrical Characteristics of the Main Crystal Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
	Operating frequency	Using external crystal	0.032		20	MHz
		Using ceramic resonator	0.5		8	MHz
		Using RC Network	0.032		4	MHz
	Output duty cycle			50		%
	Output jitter	With 10 MHz crystal		1		ns RMS
IDYNXTAL	Operating current	RC		0.6		mA
		0.032–0.2		0.6		mA
		0.2–2.0		0.6		mA
		2.0–20.0		0.6		mA
ISTBXTAL	Standby current of crystal oscillator			10		µA
PSRRXTAL	Power supply noise tolerance			0.5		Vp-p
VIHXTAL	Input logic level High		90% of VCC			V
VILXTAL	Input logic level Low				10% of VCC	V
	Startup time	RC [tested at 3.24 MHz]		300	550	ns
		0.032–0.2 [tested at 32 KHz]		500	3,000	ms
		0.2–2.0 [tested at 2 MHz]		8	15	ms
		2.0–20.0 [tested at 20 MHz]		160	180	ns

Table 2-85 • **Electrical Characteristics of the Low Power Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
	Operating frequency			32		KHz
	Output duty cycle			50		%
	Output jitter			30		ns RMS
IDYNXTAL	Operating current	32 KHz		10		µA
ISTBXTAL	Standby current of crystal oscillator			2		µA
PSRRXTAL	Power supply noise tolerance			0.5		Vp-p
VIHXTAL	Input logic level High		90% of VCC			V
VILXTAL	Input logic level Low				10% of VCC	V
	Startup time	Test load used: 20 pF		2.5		s
		Test load used: 30 pF		3.7	13	s

Embedded FlashROM (eFROM)

Electrical Characteristics

Table 2-91 describes the eFROM maximum performance

Table 2-91 • **FlashROM Access Time, Worse Military-Case Conditions: T_J = 125°C, VCC = 1.425 V**

Parameter	Description	–1	Std.	Units
F_{max}	Maximum Clock frequency	15.00	15.00	MHz

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-20 for more details.

Timing Characteristics

Table 2-92 • **JTAG 1532**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.53	0.63	ns
t_{DIHD}	Test Data Input Hold Time	1.07	1.25	ns
t_{TMSSU}	Test Mode Select Setup Time	0.53	0.63	ns
t_{TMDHD}	Test Mode Select Hold Time	1.07	1.25	ns
t_{TCK2Q}	Clock to Q (data out)	5.33	6.27	ns
t_{RSTB2Q}	Reset to Q (data out)	21.31	25.07	ns
F_{TCKMAX}	TCK Maximum Frequency	26.00	30.59	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.00	0.00	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.21	0.25	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Analog Bipolar Prescaler (ABPS)

With the ABPS set to its high range setting (GDEC = 00), a hypothetical input voltage in the range –15.36 V to +15.36 V is scaled and offset by the ABPS input amplifier to match the ADC full range of 0 V to 2.56 V using a nominal gain of –0.08333 V/V. However, due to reliability considerations, the voltage applied to the ABPS input should never be outside the range of –11.5 V to +14.4 V, restricting the usable ADC input voltage to 2.238 V to 0.080 V and the corresponding 12-bit output codes to the range of 3581 to 128 (decimal), respectively.

Unless otherwise noted, ABPS performance is specified at 25°C with nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 100 KHz sampling frequency, after trimming and digital compensation; and applies to all ranges.

Table 2-97 • **ABPS Performance Specifications**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input voltage range (for driving ADC over its full range)	GDEC[1:0] = 11		±2.56		V
	GDEC[1:0] = 10		±5.12		V
	GDEC[1:0] = 01		±10.24		V
	GDEC[1:0] = 00 (limited by maximum rating)		See note 1		V
Analog gain (from input pad to ADC input)	GDEC[1:0] = 11		–0.5		V/V
	GDEC[1:0] = 10		–0.25		V/V
	GDEC[1:0] = 01		–0.125		V/V
	GDEC[1:0] = 00		–0.0833		V/V
Gain error		–2.8	–0.4	0.7	%
	–40ºC to +100ºC	–2.8	–0.4	0.7	%
	–55ºC to +125ºC	–4	–0.4	4	%
Input referred offset voltage					
	GDEC[1:0] = 11	–0.31	–0.07	0.31	% FS*
	–55ºC to +125ºC	–1.7		1.7	% FS*
	GDEC[1:0] = 10	–0.34	–0.07	0.34	% FS*
	–55ºC to +125ºC	–1.6		1.6	% FS*
	GDEC[1:0] = 01	–0.61	–0.07	0.35	% FS*
	–55ºC to +125ºC	–1.6		1.6	% FS*
	GDEC[1:0] = 00	–0.39	–0.07	0.35	% FS*
	–55ºC to +125ºC	–1.6		1.6	% FS*
SINAD		53	56		dB
Non-linearity	RMS deviation from BFSL			0.5	% FS*

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

Inter-Integrated Circuit (I^2C) Characteristics

This section describes the DC and switching of the I^2C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, refer to Figure 2-48 on page 2-93.

Table 2-102 • I^2C Characteristics
Military-Case Conditions: T_J = 125ºC, VDD = 1.425 V, –1 Speed Grade

Parameter	Definition	Condition	Value	Unit
V_{IL}	Minimum input low voltage	–	See Table 2-37 on page 2-31	–
	Maximum input low voltage	–	See Table 2-37	–
V_{IH}	Minimum input high voltage	–	See Table 2-37	–
	Maximum input high voltage	–	See Table 2-37	–
V_{OL}	Maximum output voltage low	I_{OL} = 8 mA	See Table 2-37	–
I_{IL}	Input current high	–	See Table 2-37	–
I_{IH}	Input current low	–	See Table 2-37	–
V_{hyst}	Hysteresis of Schmitt trigger inputs	–	See Table 2-33 on page 2-30	V
T_{FALL}	Fall time [2]	VIHmin to VILMax, C_{load} = 400 pF	15.0	ns
		VIHmin to VILMax, C_{load} = 100 pF	4.0	ns
T_{RISE}	Rise time [2]	VILMax to VIHmin, C_{load} = 400pF	19.5	ns
		VILMax to VIHmin, C_{load} = 100pF	5.2	ns
Cin	Pin capacitance	VIN = 0, f = 1.0 MHz	8.0	pF
$R_{pull-up}$	Output buffer maximum pull-down Resistance [1]	–	50	Ω
$R_{pull-down}$	Output buffer maximum pull-up Resistance [1]	–	150	Ω
D_{max}	Maximum data rate	Fast mode	400	Kbps
t_{LOW}	Low period of I2C_x_SCL [3]	–	1	pclk cycles
t_{HIGH}	High period of I2C_x_SCL [3]	–	1	pclk cycles
$t_{HD;STA}$	START hold time [3]	–	1	pclk cycles
$t_{SU;STA}$	START setup time [3]	–	1	pclk cycles
$t_{HD;DAT}$	DATA hold time [3]	–	1	pclk cycles
$t_{SU;DAT}$	DATA setup time [3]	–	1	pclk cycles

Notes:

1. *These maximum values are provided for information only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *These values are provided for a load of 100 pF and 400 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website at http://www.microsemi.com/soc/download/ibis/default.aspx.*
3. *For allowable Pclk configurations, refer to the Inter-Integrated Circuit (I^2C) Peripherals section in the SmartFusion Microcontroller Subsystem User's Guide.*

3 – SmartFusion Development Tools

Designing with SmartFusion cSoCs involves three different types of design: FPGA design, embedded design and analog design. These roles can be filled by three different designers, two designers or even a single designer, depending on company structure and project complexity.

Types of Design Tools

Microsemi has developed design tools and flows to meet the needs of these three types of designers so they can work together smoothly on a single project (Figure 3-1).

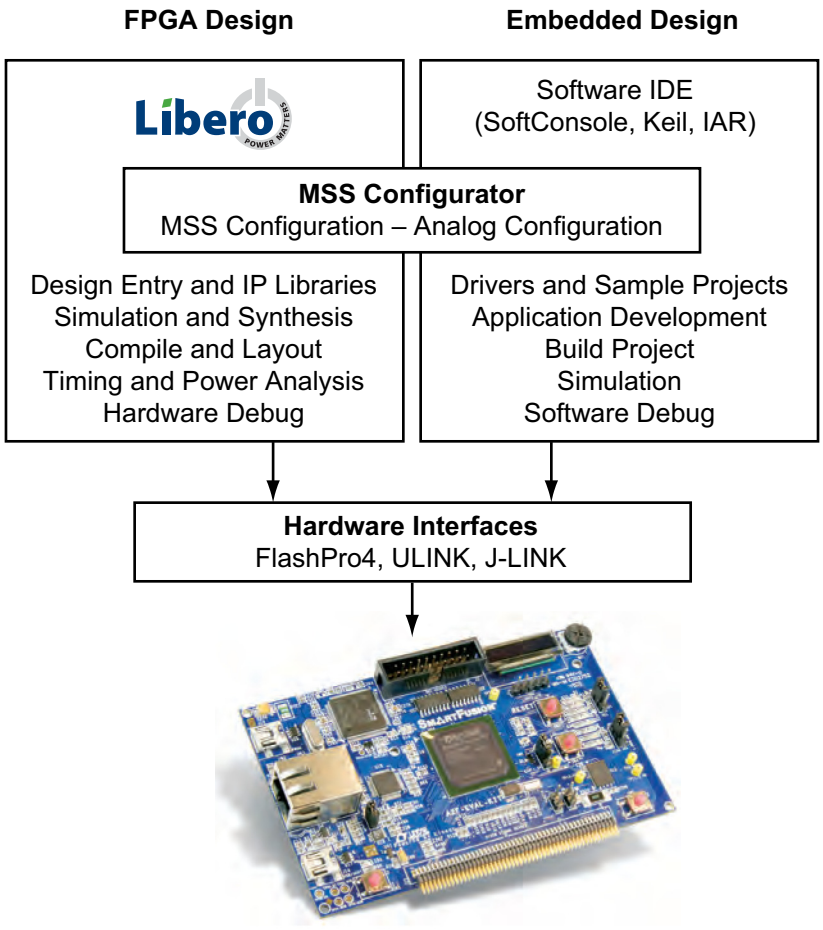

Figure 3-1 • **Three Design Roles**

FPGA Design

Libero System-on-Chip (SoC) software is Microsemi's comprehensive software toolset for designing with all Microsemi FPGAs and cSoCs. Libero SoC includes industry-leading synthesis, simulation and debug tools from Synopsys® and Mentor Graphics®, as well as innovative timing and power optimization and analysis.

Special Function Pins

Name	Type	Polarity/Bus Size	Description
NC			No connect This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.
DC			Do not connect. This pin should not be connected to any signals on the PCB. These pins should be left unconnected.
LPXIN	In	1	Low power 32 KHz crystal oscillator. Input from the 32 KHz oscillator. Pin for connecting a low power 32 KHz watch crystal. If not used, the LPXIN pin can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
LPXOUT	In	1	Low power 32 KHz crystal oscillator. Output to the 32 KHz oscillator. Pin for connecting a low power 32 KHz watch crystal. If not used, the LPXOUT pin can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
MAINXIN	In	1	Main crystal oscillator circuit. Input to the crystal oscillator circuit. Pin for connecting an external crystal, ceramic resonator, or RC network. When using an external crystal or ceramic oscillator, external capacitors are also recommended. Refer to documentation from the crystal oscillator manufacturer for proper capacitor value. If using an external RC network or clock input, MAINXIN should be grounded for better noise immunity. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
MAINXOUT	Out	1	Main crystal oscillator circuit. Output from the crystal oscillator circuit. Pin for connecting external crystal or ceramic resonator. When using an external crystal or ceramic oscillator, external capacitors are also recommended. Refer to documentation from the crystal oscillator manufacturer for proper capacitor value. If using external RC network or clock input, MAINXIN should be grounded and MAINXOUT left unconnected. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
NCAP		1	Negative capacitor connection. This is the negative terminal of the charge pump. A capacitor, with a 2.2 µF recommended value, is required to connect between PCAP and NCAP. Analog charge pump capacitors are not needed if none of the analog SCB features are used and none of the SDDs are used. In that case it should be left unconnected.

Name	Type	Polarity/Bus Size	Description
PCAP		1	Positive Capacitor connection. This is the positive terminal of the charge pump. A capacitor, with a 2.2 µF recommended value, is required to connect between PCAP and NCAP. If this pin is not used, it must be left unconnected/floating. In this case, no capacitor is needed. Analog charge pump capacitors are not needed if none of the analog SCB features are used, and none of the SDDs are used.
PTBASE		1	Pass transistor base connection This is the control signal of the voltage regulator. This pin should be connected to the base of an external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.
PTEM		1	Pass transistor emitter connection. This is the feedback input of the voltage regulator. This pin should be connected to the emitter of an external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.
MSS_RESET_N		Low	Low Reset signal which can be used as an external reset and can also be used as a system level reset under control of the Cortex-M3 processor. MSS_RESET_N is an output asserted low after power-on reset. The direction of MSS_RESET_N changes during the execution of the Microsemi System Boot when chip-level reset is enabled. The Microsemi System Boot reconfigures MSS_RESET_N to become a reset input signal when chip-level reset is enabled. It has an internal pull-up so it can be left floating. In the current software, the MSS_RESET_N is modeled as an external input signal only.
PU_N	In	Low	Push-button is the connection for the external momentary switch used to turn on the 1.5 V voltage regulator and can be floating if not used.

Pin No.	FG256	
	A2F060 Function	A2F500 Function
C2	VCCPLL0	VCCPLL0
C3	EMC_BYTEN[0]/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO07NDB0V0
C4	VCCFPGAIOB0	VCCFPGAIOB0
C5	EMC_CS0_N/IO01NDB0V0	EMC_CS0_N/GAB0/IO05NDB0V0
C6	EMC_CS1_N/IO01PDB0V0	EMC_CS1_N/GAB1/IO05PDB0V0
C7	GND	GND
C8	EMC_AB[8]/IO08NDB0V0	EMC_AB[8]/IO13NDB0V0
C9	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO11PDB0V0
C10	VCCFPGAIOB0	VCCFPGAIOB0
C11	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO17PDB0V0
C12	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO18PDB0V0
C13	GND	GND
C14	GCC0/IO18NPB0V0	GBA2/IO27PPB1V0
C15	GCB0/IO19NDB0V0	GCA2/IO28PDB1V0
C16	GCB1/IO19PDB0V0	IO28NDB1V0
D1	VCCFPGAIOB5	VCCFPGAIOB5
D2	VCOMPLA0	VCOMPLA0
D3	GND	GND
D4	GNDQ	GNDQ
D5	EMC_CLK/IO00NDB0V0	EMC_CLK/GAA0/IO02NDB0V0
D6	EMC_RW_N/IO00PDB0V0	EMC_RW_N/GAA1/IO02PDB0V0
D7	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO12NDB0V0
D8	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO12PDB0V0
D9	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO11NDB0V0
D10	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO19NDB0V0
D11	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO19PDB0V0
D12	GNDQ	GNDQ
D13	GCC1/IO18PPB0V0	GBB2/IO27NPB1V0
D14	GCA0/IO20NDB0V0	GCB2/IO33PDB1V0
D15	GCA1/IO20PDB0V0	IO33NDB1V0
D16	VCCFPGAIOB1	VCCFPGAIOB1
E1	EMC_DB[13]/IO44PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
E2	EMC_DB[12]/IO44NDB5V0	EMC_DB[12]/IO87NDB5V0

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin No.	FG256	
	A2F060 Function	A2F500 Function
N7	NC	GND33ADC0
N8	VCC33ADC0	VCC33ADC1
N9	ADC8	ADC5
N10	CM0	CM3
N11	GNDAQ	GNDAQ
N12	VAREFOUT	VAREFOUT
N13	NC	GNDSDD1
N14	NC	VCC33SDD1
N15	GND	GND
N16	SPI_0_DO/GPIO_16	SPI_0_DO/GPIO_16
P1	GNDSDD0	GNDSDD0
P2	VCC33SDD0	VCC33SDD0
P3	VCC33N	VCC33N
P4	GNDA	GNDA
P5	GNDAQ	GNDAQ
P6	NC	CM1
P7	NC	ADC2
P8	NC	VCC15ADC0
P9	ADC9	ADC6
P10	TM0	TM3
P11	GNDA	GNDA
P12	VCCMAINXTAL	VCCMAINXTAL
P13	GNDLPXTAL	GNDLPXTAL
P14	VDDBAT	VDDBAT
P15	PTEM	PTEM
P16	PTBASE	PTBASE
R1	PCAP	PCAP
R2	SDD0	SDD0
R3	ADC0	ABPS0
R4	ADC3	TM0
R5	NC	ABPS2
R6	NC	ADC1
R7	NC	VCC33ADC0

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin No.	FG256	
	A2F060 Function	A2F500 Function
R8	VCC15ADC0	VCC15ADC1
R9	ADC10	ADC7
R10	ABPS1	ABPS7
R11	NC	ABPS4
R12	MAINXIN	MAINXIN
R13	MAINXOUT	MAINXOUT
R14	LPXIN	LPXIN
R15	LPXOUT	LPXOUT
R16	VCC33A	VCC33A
T1	NCAP	NCAP
T2	ADC1	ABPS1
T3	ADC2	CM0
T4	NC	GNDTM0
T5	NC	ADC0
T6	NC	VAREF0
T7	NC	GND33ADC0
T8	GND15ADC0	GND15ADC1
T9	VAREF0	VAREF1
T10	ABPS0	ABPS6
T11	NC	ABPS5
T12	NC	SDD1
T13	GNDVAREF	GNDVAREF
T14	GNDMAINXTAL	GNDMAINXTAL
T15	VCCLPXTAL	VCCLPXTAL
T16	PU_N	PU_N

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

FG484	
Pin Number	A2F500 Function
R19	NC
R20	NC
R21	VCCFPGAIOB1
R22	NC
T1	GND
T2	VCCMSSIOB4
T3	GPIO_8/IO48RSB4V0
T4	GPIO_11/IO66RSB4V0
T5	GND
T6	MAC_CLK
T7	VCCMSSIOB4
T8	VCC33SDD0
T9	VCC15A
T10	GNDAQ
T11	GND33ADC0
T12	ADC7
T13	TM4
T14	VAREF2
T15	VAREFOUT
T16	VCCMSSIOB2
T17	SPI_1_DO/GPIO_24
T18	GND
T19	NC
T20	NC
T21	VCCMSSIOB2
T22	GND
U1	GND
U2	GPIO_5/IO51RSB4V0
U3	GPIO_10/IO67RSB4V0
U4	VCCMSSIOB4
U5	MAC_RXD[1]/IO62RSB4V0
U6	NC
U7	VCC33AP
U8	VCC33N
U9	CM1
U10	VAREF0
U11	GND33ADC1

FG484	
Pin Number	A2F500 Function
U12	ADC4
U13	GNDTM2
U14	ADC11
U15	GNDVAREF
U16	VCC33SDD1
U17	SPI_0_DO/GPIO_16
U18	UART_0_RXD/GPIO_21
U19	VCCMSSIOB2
U20	I2C_1_SCL/GPIO_31
U21	I2C_0_SCL/GPIO_23
U22	GND
V1	GPIO_0/IO56RSB4V0
V2	GPIO_6/IO50RSB4V0
V3	GPIO_9/IO47RSB4V0
V4	MAC_MDIO/IO58RSB4V0
V5	MAC_RXD[0]/IO63RSB4V0
V6	GND
V7	SDD0
V8	ABPS1
V9	ADC2
V10	VCC33ADC0
V11	ADC6
V12	ADC5
V13	ABPS5
V14	ADC8
V15	GND33ADC2
V16	NC
V17	GND
V18	SPI_0_DI/GPIO_17
V19	SPI_1_DI/GPIO_25
V20	UART_1_TXD/GPIO_28
V21	I2C_0_SDA/GPIO_22
V22	I2C_1_SDA/GPIO_30
W1	GPIO_2/IO54RSB4V0
W2	GPIO_7/IO49RSB4V0
W3	GND
W4	MAC_CRSDV/IO60RSB4V0

6 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the SmartFusion datasheet.

Revision	Changes	Page
Revision 2 (March 2015)	Updated information about unused MSS I/O configuration in "User I/O Naming Conventions" (SAR 62994).	5-6
Revision 1 (September 2012)	The status was changed from Preliminary to Production for A2F060 and A2F500 in the "SmartFusion cSoC Device Status" table (SAR 41135).	III