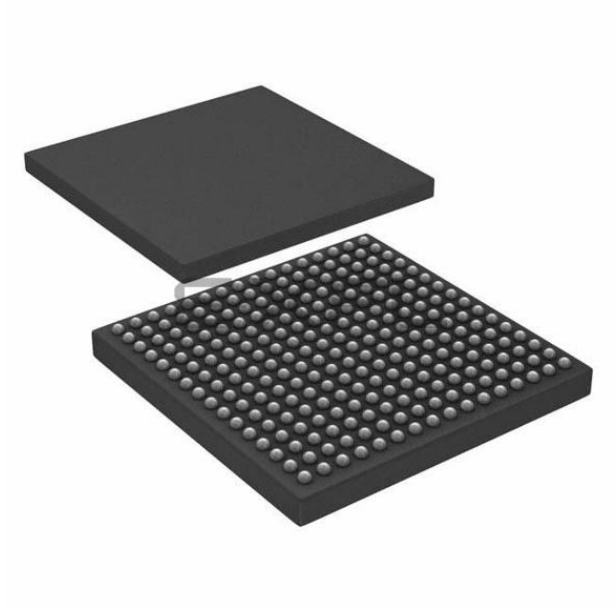

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	128KB
RAM Size	16KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Speed	80MHz
Primary Attributes	ProASIC®3 FPGA, 60K Gates, 1536D-Flip-Flops
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a2f060m3e-fg256m

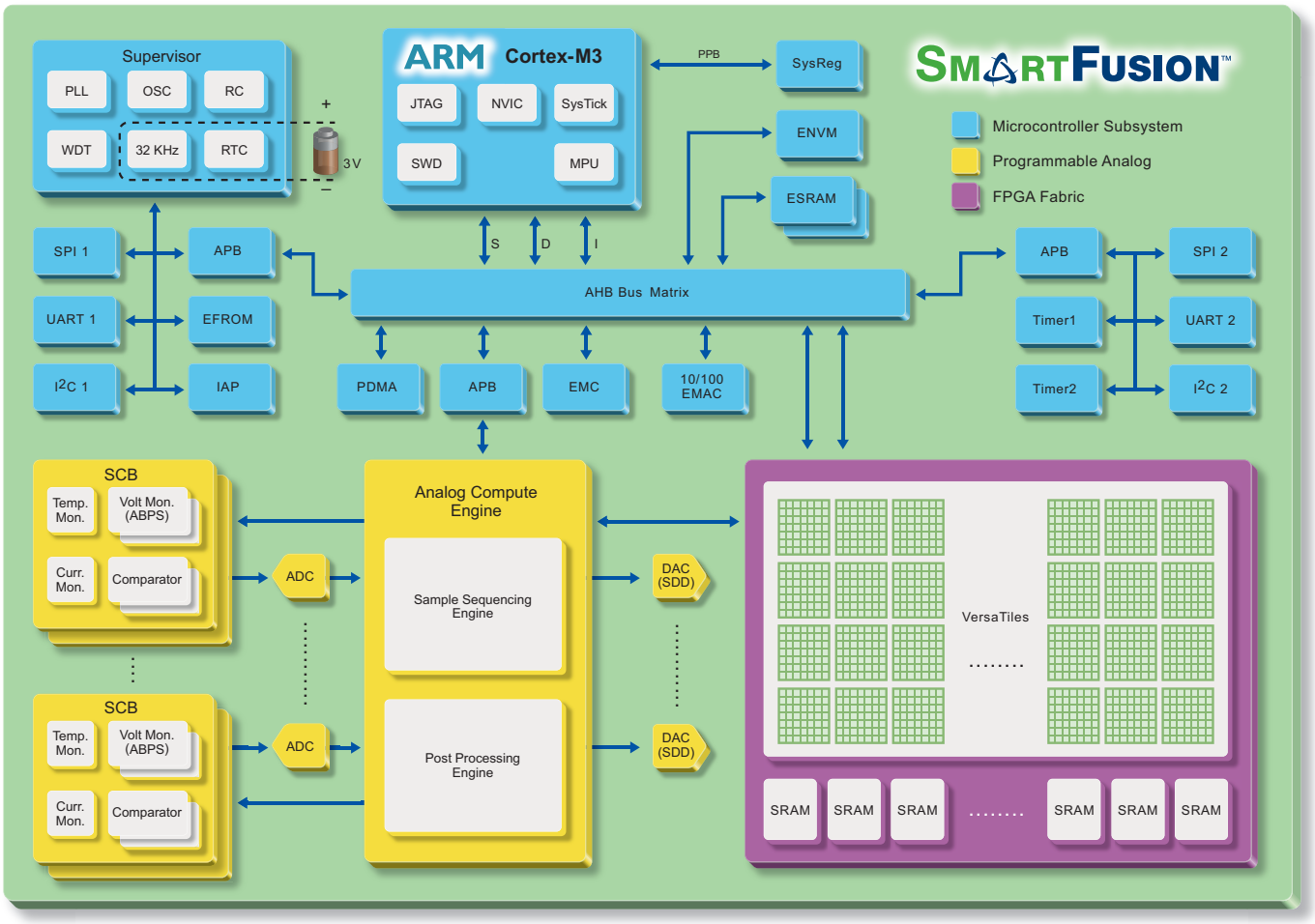
SmartFusion cSoC Family Product Table

SmartFusion® cSoC		A2F060	A2F500
FPGA Fabric	System Gates	60,000	500,000
	Tiles (D-flip-flops)	1,536	11,520
	RAM Blocks (4,608 bits)	8	24
Microcontroller Subsystem (MSS)	Flash (Kbytes)	128	512
	SRAM (Kbytes)	16	64
	Cortex-M3 with memory protection unit (MPU)	Yes	
	10/100 Ethernet MAC	No	Yes
	External Memory Controller (EMC)	24-bit address,16-bit data	
	DMA	8 Ch	
	I^2C	2	
	SPI	2	
	16550 UART	2	
	32-Bit Timer	2	
	PLL	1	2[1]
	32 KHz Low Power Oscillator	1	
	100 MHz On-Chip RC Oscillator	1	
	Main Oscillator (32 KHz to 20 MHz)	1	
Programmable Analog	ADCs (8-/10-/12-bit SAR)	1	3[3]
	DACs (12-bit sigma-delta)	1	3[3]
	Signal Conditioning Blocks (SCBs)	1	5[3]
	Comparator[2]	2	10[3]
	Current Monitors[2]	1	5[3]
	Temperature Monitors[2]	1	5[3]
	Bipolar High Voltage Monitors[2]	2	10[3]

Notes:

1. *Two PLLs are available in FG484 (one PLL in FG256).*
2. *These functions share I/O pins and may not all be available at the same time. See the "Analog Front-End Overview" section in the SmartFusion Programmable Analog User's Guide for details.*
3. *Available on FG484 only.*

SmartFusion cSoC Block Diagram



Legend:

SDD – Sigma-delta DAC
SCB – Signal conditioning block
PDMA – Peripheral DMA
IAP – In-application programming
ABPS – Active bipolar prescaler
WDT – Watchdog Timer
SWD – Serial Wire Debug

Table of Contents

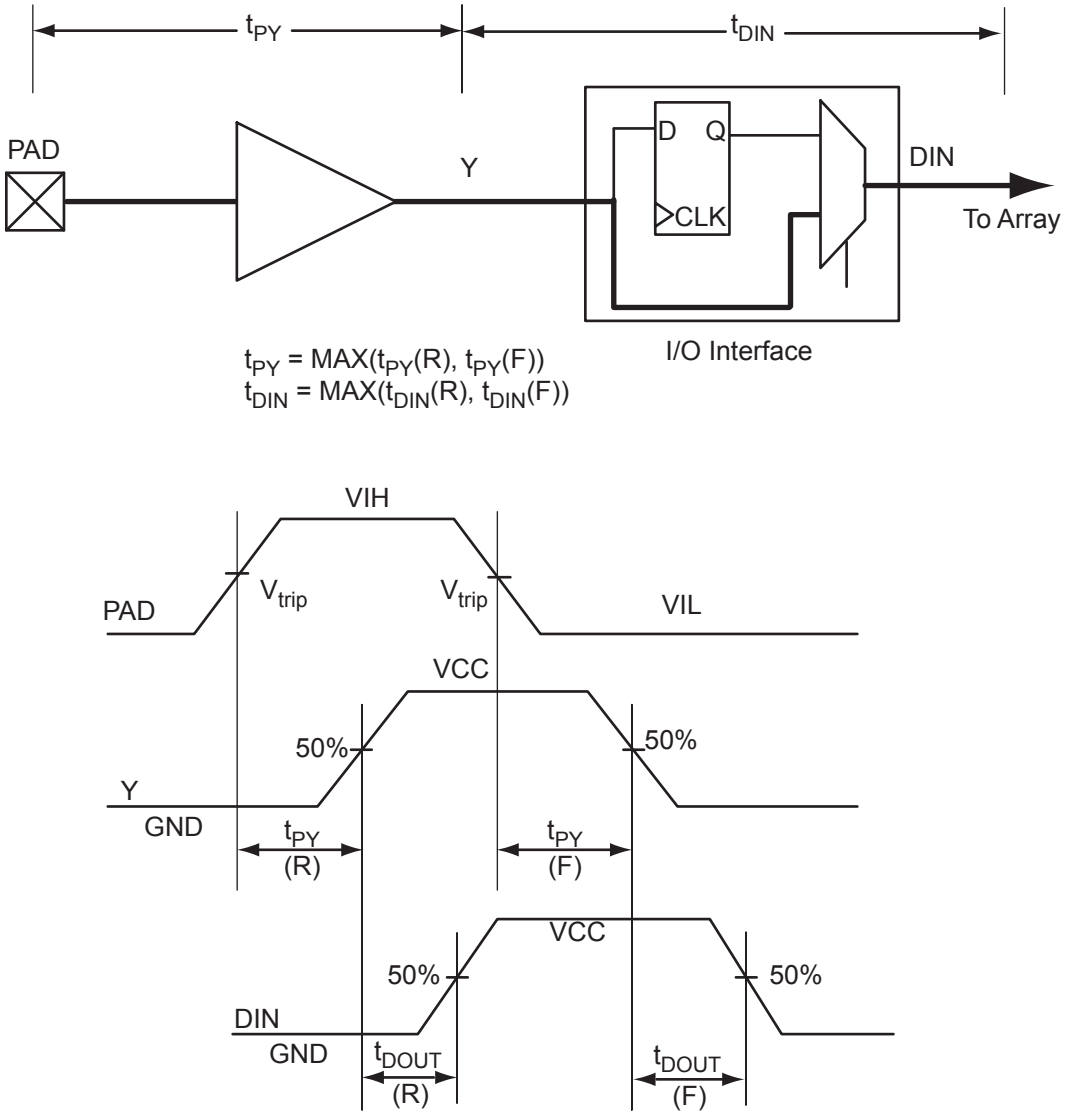


Figure 2-4 • **Input Buffer Timing Model and Delays (example)**

**Table 2-28 • I/O Output Buffer Maximum Resistances[1]
Applicable to MSS I/O Banks**

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	8mA	50	150
2.5 V LVCMOS	8 mA	50	100
1.8 V LVCMOS	4 mA	100	112
1.5 V LVCMOS	2 mA	200	224

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / IOLspec
3. $R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / IOHspec

**Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values**

	$R_{(WEAK\ PULL\text{-}UP)}$[1] (Ω)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ω)	
VCCxxxxIOBx	Min.	Max.	Min.	Max.
3.3 V	10 k	90 k	10 k	90 k
2.5 V	11 k	100 k	12 k	105 k
1.8 V	18 k	110 k	17 k	150 k
1.5 V	19 k	150 k	19 k	180 k

Notes:

1. $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / $I_{(WEAK\ PULL\text{-}DOWN\text{-}MIN)}$
2. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / $I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-54 • Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.575	0.25* VCCxxxxIOBx	0.75 * VCCxxxxIOBx	2	2	16	13	15	15
4 mA	–0.3	0.35* VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.575	0.25* VCCxxxxIOBx	0.75 * VCCxxxxIOBx	4	4	33	25	15	15
6 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.575	0.25* VCCxxxxIOBx	0.75 * VCCxxxxIOBx	6	6	39	32	15	15
8 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.575	0.25* VCC	0.75 * VCCxxxxIOBx	8	8	55	66	15	15
12 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.575	0.25 * VCCxxxxIOBx	0.75 * VCCxxxxIOBx	12	12	55	66	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-55 • Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.575	0.25 * VCCxxxxIOBx	0.75 * VCCxxxxIOBx	2	2	16	13	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

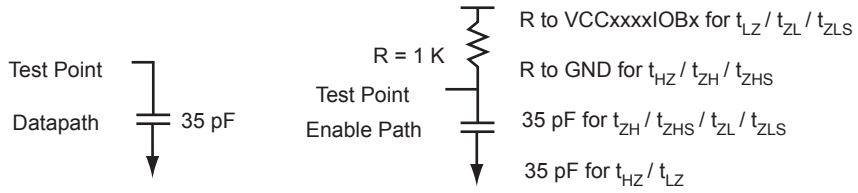


Figure 2-10 • AC Loading

Table 2-56 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	1.5	0.75	–	35

*Note: *Measuring point = Vtrip. See Table 2-22 on page 2-25 for a complete table of trip points.*

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-60 • Minimum and Maximum DC Input and Output Levels

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
Per PCI specification	Per PCI curves										15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; SoC Products Group loadings for enable path characterization are described in Figure 2-11.

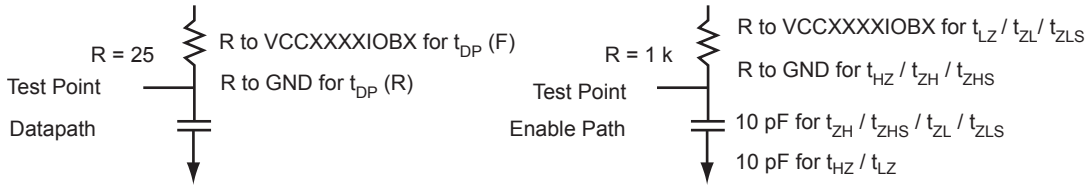


Figure 2-11 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the datapath; SoC Products Group loading for tristate is described in Table 2-61.

Table 2-61 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	3.3	0.285 * VCCxxxxIOBx for $t_{DP(R)}$ 0.615 * VCCxxxxIOBx for $t_{DP(F)}$	–	10

*Note: *Measuring point = Vtrip. See Table 2-22 on page 2-25 for a complete table of trip points.*

Timing Characteristics

Table 2-62 • 3.3 V PCI
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.62	2.72	0.04	0.88	0.41	2.77	2.02	3.28	3.62	4.97	4.22	ns
–1	0.52	2.26	0.03	0.73	0.34	2.30	1.68	2.73	3.02	4.14	3.52	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-63 • 3.3 V PCI-X
Worst Military-Case Conditions: T_J =125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.62	2.72	0.04	0.83	0.41	2.77	2.02	3.28	3.62	4.97	4.22	ns
–1	0.52	2.26	0.03	0.69	0.34	2.30	1.68	2.73	3.02	4.14	3.52	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-64 • LVDS Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCFPGAIOBx	Supply voltage	2.375	2.5	2.625	V
VOL	Output low voltage	0.9	1.075	1.25	V
VOH	Output high voltage	1.25	1.425	1.6	V
I_{OL}[1]	Output lower current	0.65	0.91	1.16	mA
I_{OH}[1]	Output high current	0.65	0.91	1.16	mA
VI	Input voltage	0		2.925	V
I_{IH}[2]	Input high leakage current			15	µA
I_{IL}[2]	Input low leakage current			15	µA
V_{ODIFF}	Differential output voltage	250	350	450	mV
V_{OCM}	Output common mode voltage	1.125	1.25	1.375	V
V_{ICM}	Input common mode voltage	0.05	1.25	2.35	V
V_{IDIFF}	Input differential voltage	100	350		mV

Notes:

1. *IOL/IOH defined by VODIFF/(resistor network).*
2. *Currents are measured at 125°C junction temperature.*

Table 2-65 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.075	1.325	Cross point	–

*Note: *Measuring point = Vtrip. See Table 2-22 on page 2-25 for a complete table of trip points.*

Timing Characteristics

Table 2-66 • LVDS
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCFPGAIOBx = 2.3 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.62	1.96	0.04	1.63	ns
–1	0.52	1.63	0.03	1.36	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-71 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

*Note: *See Figure 2-16 on page 2-48 for more information.*

Output Register

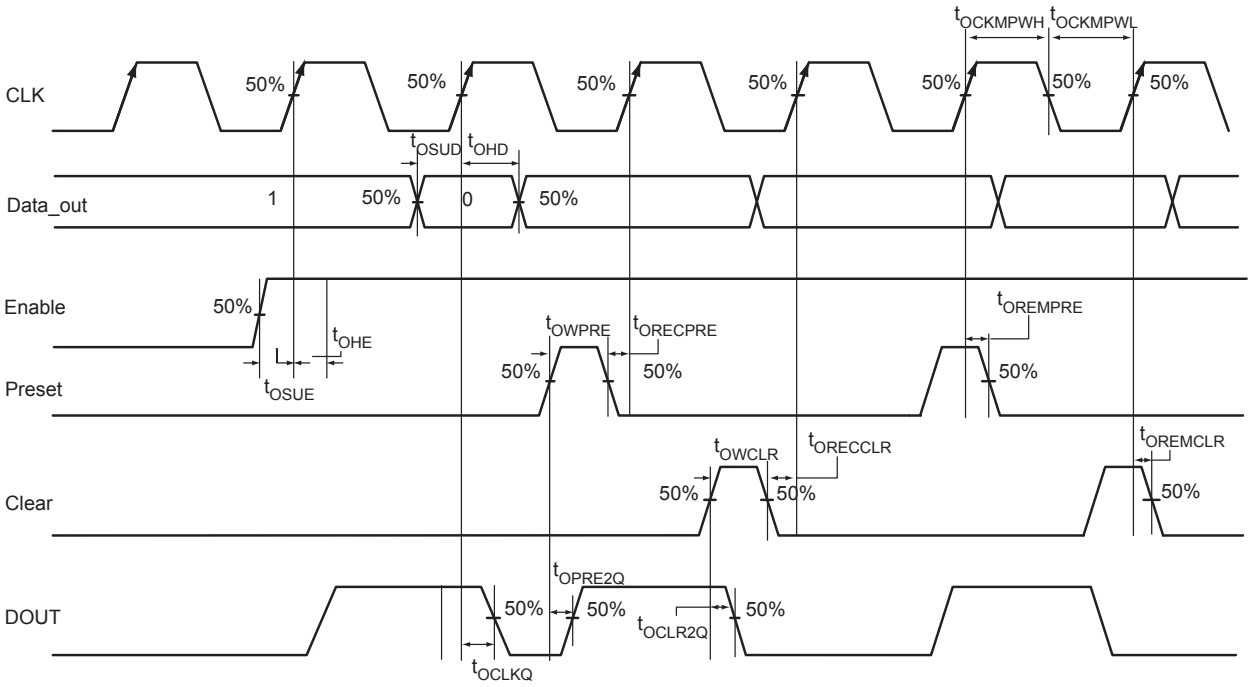


Figure 2-18 • **Output Register Timing Diagram**

Timing Characteristics

Table 2-73 • **Output Data Register Propagation Delays**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.62	0.75	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.33	0.40	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.46	0.56	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.85	1.02	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.85	1.02	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	0.28	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	0.28	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.26	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.26	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.42	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.38	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

DDR Module Specifications

Input DDR Module

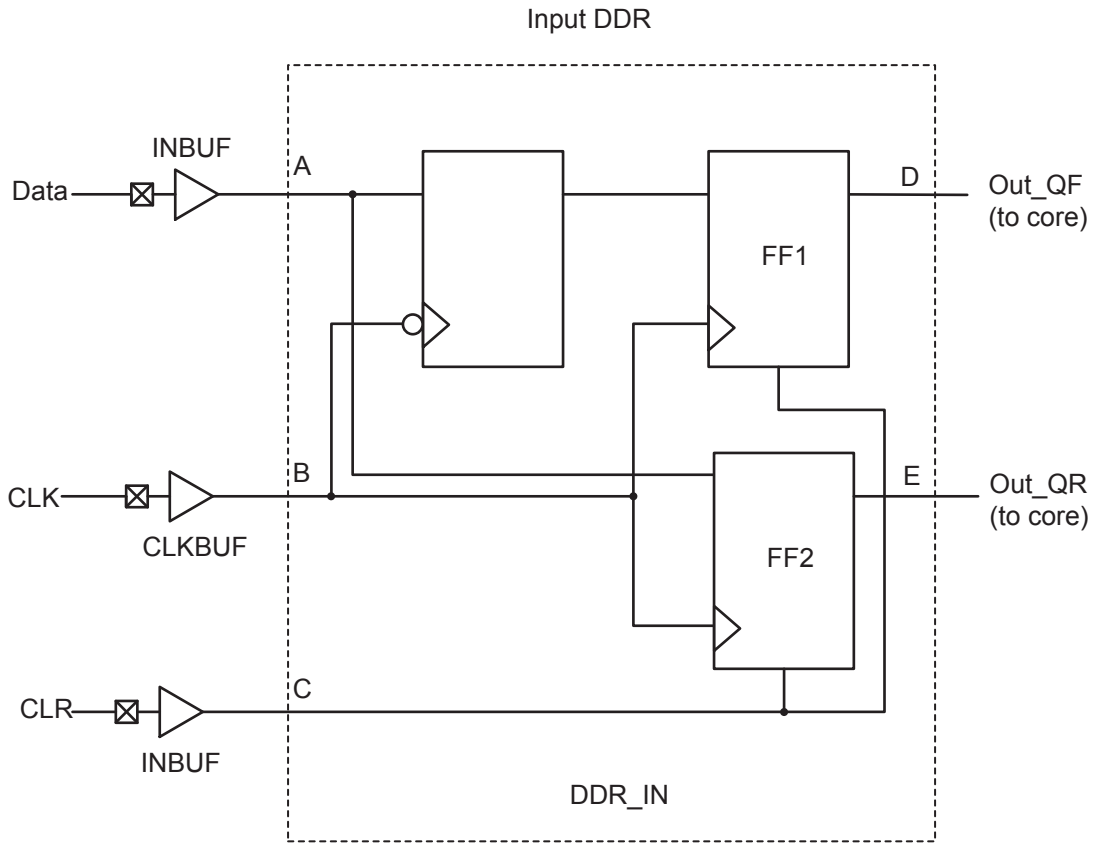


Figure 2-20 • **Input DDR Timing Model**

Table 2-75 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The SmartFusion library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide*.

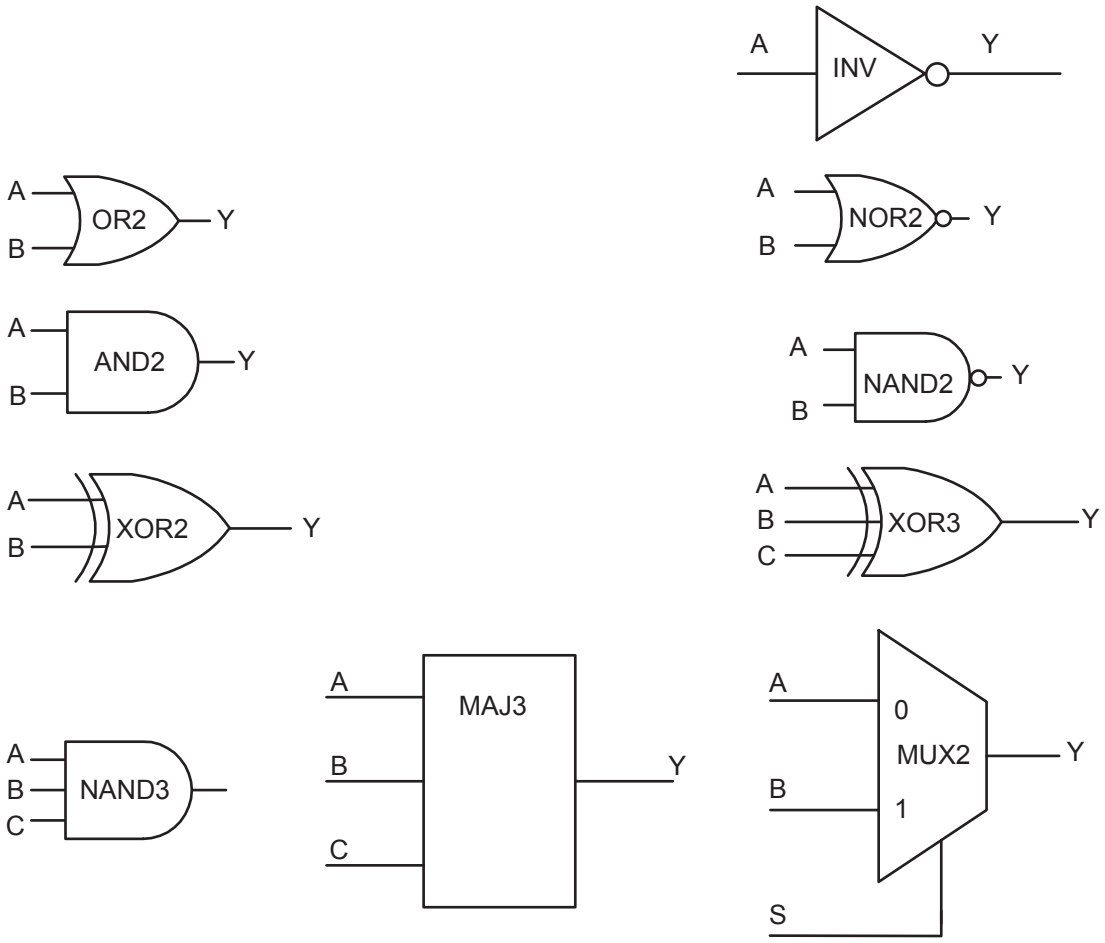


Figure 2-24 • **Sample of Combinatorial Cells**

Timing Waveforms

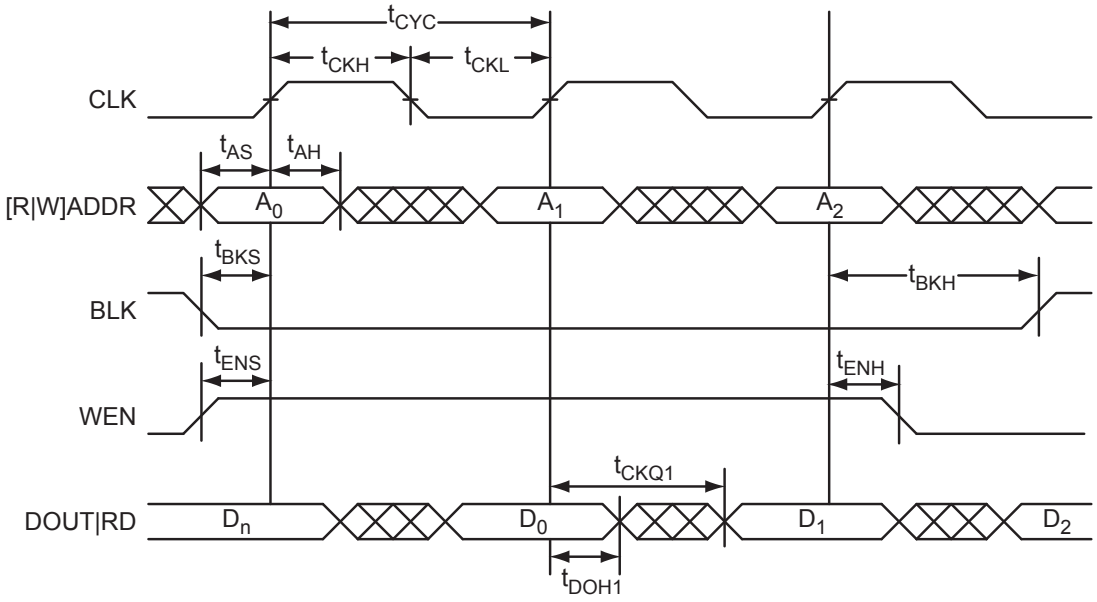


Figure 2-31 • **RAM Read for Pass-Through Output. Applicable to both RAM4K9 and RAM512x18**.

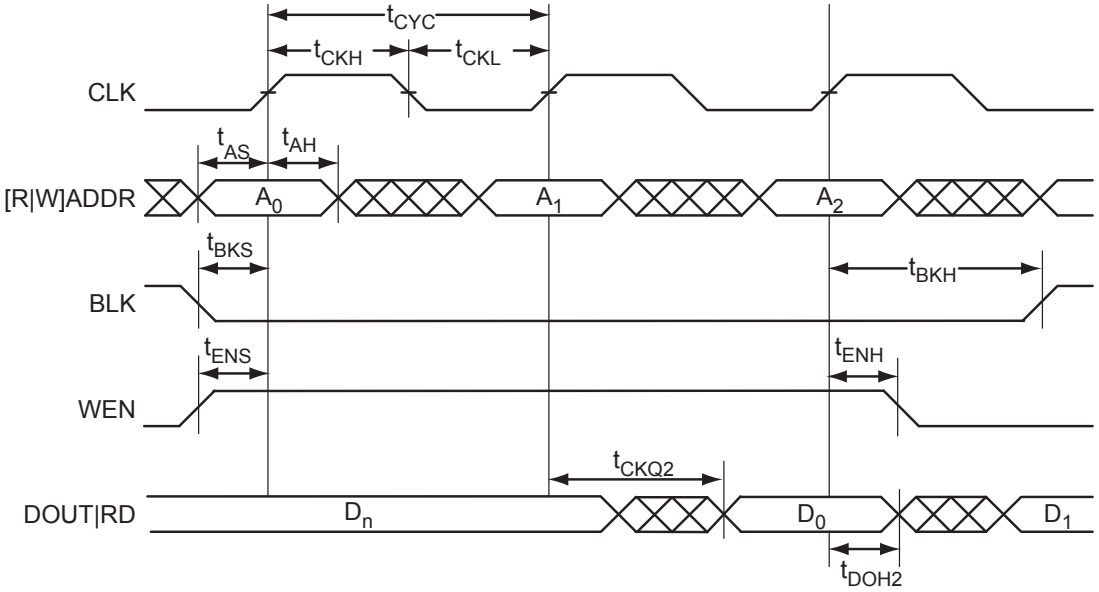


Figure 2-32 • **RAM Read for Pipelined Output Applicable to both RAM4K9 and RAM512x18.**

Analog-to-Digital Converter (ADC)

Unless otherwise noted, ADC direct input performance is specified at 25°C with nominal power supply voltages, with the output measured using the external voltage reference with the internal ADC in 12-bit mode and 500 KHz sampling frequency, after trimming and digital compensation.

Table 2-95 • **ADC Specifications**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input voltage range (for driving ADC over its full range)			2.56		V
Gain error			±0.4	±0.7	%
	–55ºC to +125ºC		±0.4	±0.7	%
Input referred offset voltage			±1	±2	mV
	–55ºC to +125ºC		±1	±4	mV
Integral non-linearity (INL)	RMS deviation from BFSL				
	12-bit mode		1.71		LSB
	10-bit mode		0.60	1.00	LSB
	8-bit mode		0.2	0.33	LSB
Differential non-linearity (DNL)	12-bit mode		2.4		LSB
	10-bit mode		0.80	0.94	LSB
	8-bit mode		0.2	0.23	LSB
Signal to noise ratio		62	64		dB
Effective number of bits (ENOB) $ENOB = \frac{SINAD - 1.76\ dB}{6.02\ dB/bit}$ *EQ 10*	–1 dBFS input				
	12-bit mode 10 KHz	9.9	10		Bits
	12-bit mode 100 KHz	9.9	10		Bits
	10-bit mode 10 KHz	9.5	9.6		Bits
	10-bit mode 100 KHz	9.5	9.6		Bits
	8-bit mode 10 KHz	7.8	7.9		Bits
	8-bit mode 100 KHz	7.8	7.9		Bits
Full power bandwidth	At –3 dB; –1 dBFS input	300			KHz
Analog settling time	To 0.1% of final value (with 1 Kohm source impedance and with ADC load)		2		µs
Input capacitance	Switched capacitance (ADC sample capacitor)		12	15	pF
	Cs: Static capacitance (Figure 2-43 on page 2-82)				
	CM[n] input		5	7	pF
	TM[n] input		5	7	pF
	ADC[n] input		5	7	pF
Input resistance	Rin: Series resistance (Figure 2-43)		2		KΩ
	Rsh: Shunt resistance, exclusive of switched capacitance effects (Figure 2-43)	10			MΩ

Note: All 3.3 V supplies are tied together and varied from 3.0 V to 3.6 V. 1.5 V supplies are held constant.

Table 2-95 • ADC Specifications (continued)

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input leakage current	–40°C to +100°C		1		µA
Power supply rejection ratio	DC	44	53		dB
ADC power supply operational current requirements	VCC33ADCx			2.5	mA
	VCC15A			2	mA

Note: All 3.3 V supplies are tied together and varied from 3.0 V to 3.6 V. 1.5 V supplies are held constant.

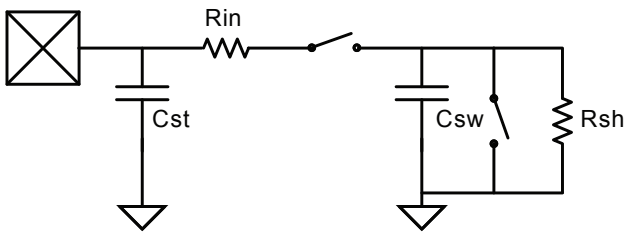


Figure 2-43 • ADC Input Model

Table 2-96 • VAREF Stabilization Time

VAREF Capacitor Value (µF)	Required Settling Time for 8-Bit and 10-Bit Mode (ms)	Required Settling Time for 12-Bit Mode (ms)
0.01	1	1
0.1	3	4
0.2	6	8
0.3	10	11
0.5	17	20
0.7	18	21
1	32	37
2.2	62	73
3.3	99	117
10	275	325
22	635	751
47	1318	1557

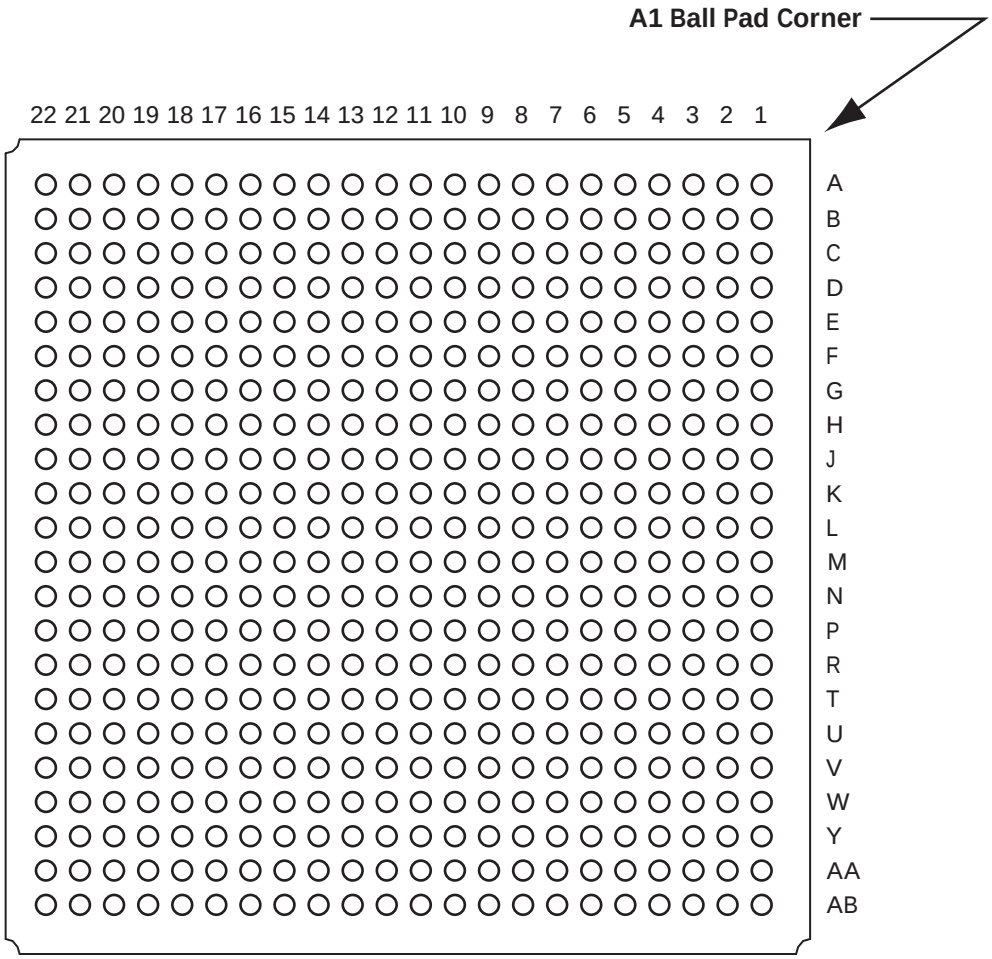
Name	Type	Description	Associated With	
			ADC/SDD	SCB
TM0	In	SCB 0 / low side of current monitor / comparator Negative input / high side of temperature monitor. See the Temperature Monitor section.	ADC0	SCB0
TM1	In	SCB 1 / low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC0	SCB1
TM2	In	SCB 2 / low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC1	SCB2
TM3	In	SCB 3 low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC1	SCB3
TM4	In	SCB 4 low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC2	SCB4
SDD0	Out	Output of SDD0 See the Sigma-Delta Digital-to-Analog Converter (DAC) section in the *SmartFusion Programmable Analog User's Guide*.	SDD0	N/A
SDD1	Out	Output of SDD1	SDD1	N/A
SDD2	Out	Output of SDD2	SDD2	N/A

Note: Unused analog inputs should be grounded. This aids in shielding and prevents an undesired coupling path.

Pin No.	FG256	
	A2F060 Function	A2F500 Function
E3	GFA2/IO42PDB5V0	GFA2/IO85PDB5V0
E4	EMC_DB[10]/IO43NPB5V0	EMC_DB[10]/IO86NPB5V0
E5	GNDQ	GNDQ
E6	GND	GND
E7	VCCFPGAIOB0	VCCFPGAIOB0
E8	GND	GND
E9	VCCFPGAIOB0	VCCFPGAIOB0
E10	GND	GND
E11	VCCFPGAIOB0	VCCFPGAIOB0
E12	GCB2/IO22PDB1V0	GCA1/IO36PDB1V0
E13	VCCFPGAIOB1	VCCFPGAIOB1
E14	GCA2/IO21PDB1V0	GCB1/IO34PDB1V0
E15	GCC2/IO23PDB1V0	GDC1/IO38PDB1V0
E16	IO23NDB1V0	GDC0/IO38NDB1V0
F1	EMC_DB[9]/IO40PDB5V0	EMC_DB[9]/GEC1/IO80PDB5V0
F2	GND	GND
F3	GFB2/IO42NDB5V0	GFB2/IO85NDB5V0
F4	VCCFPGAIOB5	VCCFPGAIOB5
F5	EMC_DB[11]/IO43PPB5V0	EMC_DB[11]/IO86PPB5V0
F6	VCCFPGAIOB5	VCCFPGAIOB5
F7	GND	GND
F8	VCC	VCC
F9	GND	GND
F10	VCC	VCC
F11	GND	GND
F12	IO22NDB1V0	GCA0/IO36NDB1V0
F13	NC	GNDQ
F14	IO21NDB1V0	GCB0/IO34NDB1V0
F15	GND	GND
F16	VCCENVM	VCCENVM
G1	EMC_DB[8]/IO40NDB5V0	EMC_DB[8]/GEC0/IO80NDB5V0
G2	EMC_DB[7]/IO39PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
G3	EMC_DB[6]/IO39NDB5V0	EMC_DB[6]/GEB0/IO79NDB5V0

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

FG484



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

FG484	
Pin Number	A2F500 Function
R19	NC
R20	NC
R21	VCCFPGAIOB1
R22	NC
T1	GND
T2	VCCMSSIOB4
T3	GPIO_8/IO48RSB4V0
T4	GPIO_11/IO66RSB4V0
T5	GND
T6	MAC_CLK
T7	VCCMSSIOB4
T8	VCC33SDD0
T9	VCC15A
T10	GNDAQ
T11	GND33ADC0
T12	ADC7
T13	TM4
T14	VAREF2
T15	VAREFOUT
T16	VCCMSSIOB2
T17	SPI_1_DO/GPIO_24
T18	GND
T19	NC
T20	NC
T21	VCCMSSIOB2
T22	GND
U1	GND
U2	GPIO_5/IO51RSB4V0
U3	GPIO_10/IO67RSB4V0
U4	VCCMSSIOB4
U5	MAC_RXD[1]/IO62RSB4V0
U6	NC
U7	VCC33AP
U8	VCC33N
U9	CM1
U10	VAREF0
U11	GND33ADC1

FG484	
Pin Number	A2F500 Function
U12	ADC4
U13	GNDTM2
U14	ADC11
U15	GNDVAREF
U16	VCC33SDD1
U17	SPI_0_DO/GPIO_16
U18	UART_0_RXD/GPIO_21
U19	VCCMSSIOB2
U20	I2C_1_SCL/GPIO_31
U21	I2C_0_SCL/GPIO_23
U22	GND
V1	GPIO_0/IO56RSB4V0
V2	GPIO_6/IO50RSB4V0
V3	GPIO_9/IO47RSB4V0
V4	MAC_MDIO/IO58RSB4V0
V5	MAC_RXD[0]/IO63RSB4V0
V6	GND
V7	SDD0
V8	ABPS1
V9	ADC2
V10	VCC33ADC0
V11	ADC6
V12	ADC5
V13	ABPS5
V14	ADC8
V15	GND33ADC2
V16	NC
V17	GND
V18	SPI_0_DI/GPIO_17
V19	SPI_1_DI/GPIO_25
V20	UART_1_TXD/GPIO_28
V21	I2C_0_SDA/GPIO_22
V22	I2C_1_SDA/GPIO_30
W1	GPIO_2/IO54RSB4V0
W2	GPIO_7/IO49RSB4V0
W3	GND
W4	MAC_CRSDV/IO60RSB4V0