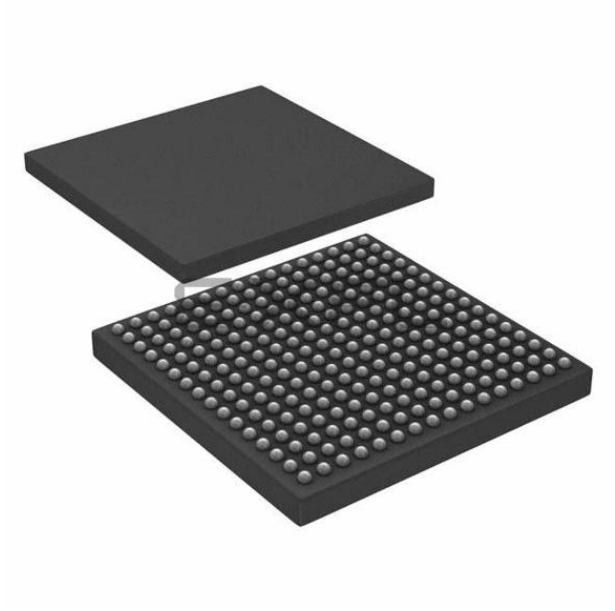

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	128KB
RAM Size	16KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Speed	80MHz
Primary Attributes	ProASIC®3 FPGA, 60K Gates, 1536D-Flip-Flops
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a2f060m3e-fgg256m

SmartFusion cSoC Family Product Table

SmartFusion® cSoC		A2F060	A2F500
FPGA Fabric	System Gates	60,000	500,000
	Tiles (D-flip-flops)	1,536	11,520
	RAM Blocks (4,608 bits)	8	24
Microcontroller Subsystem (MSS)	Flash (Kbytes)	128	512
	SRAM (Kbytes)	16	64
	Cortex-M3 with memory protection unit (MPU)	Yes	
	10/100 Ethernet MAC	No	Yes
	External Memory Controller (EMC)	24-bit address,16-bit data	
	DMA	8 Ch	
	I^2C	2	
	SPI	2	
	16550 UART	2	
	32-Bit Timer	2	
	PLL	1	2[1]
	32 KHz Low Power Oscillator	1	
	100 MHz On-Chip RC Oscillator	1	
	Main Oscillator (32 KHz to 20 MHz)	1	
Programmable Analog	ADCs (8-/10-/12-bit SAR)	1	3[3]
	DACs (12-bit sigma-delta)	1	3[3]
	Signal Conditioning Blocks (SCBs)	1	5[3]
	Comparator[2]	2	10[3]
	Current Monitors[2]	1	5[3]
	Temperature Monitors[2]	1	5[3]
	Bipolar High Voltage Monitors[2]	2	10[3]

Notes:

1. *Two PLLs are available in FG484 (one PLL in FG256).*
2. *These functions share I/O pins and may not all be available at the same time. See the "Analog Front-End Overview" section in the SmartFusion Programmable Analog User's Guide for details.*
3. *Available on FG484 only.*

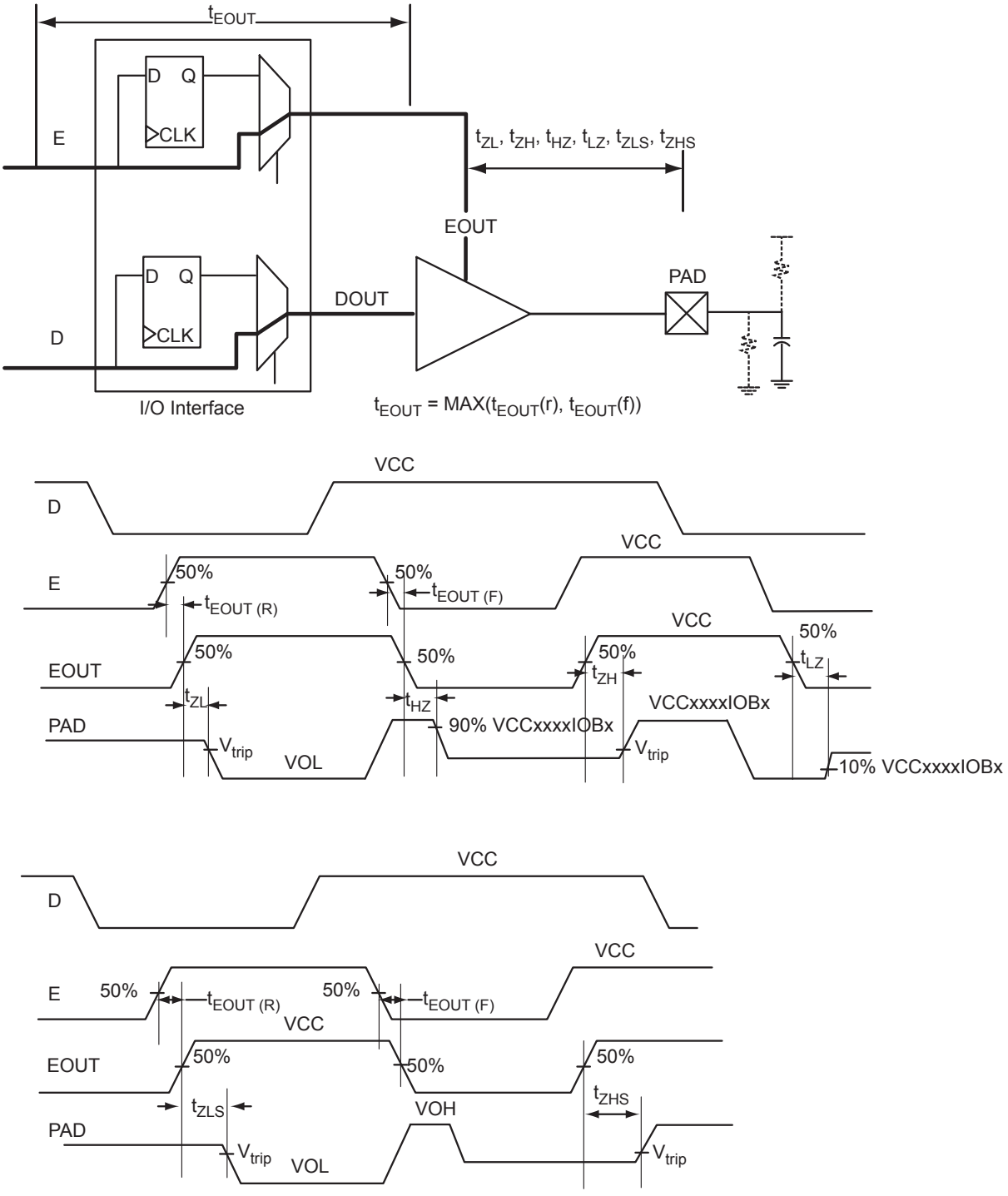

Figure 2-6 • **Tristate Output Buffer Timing Model and Delays (example)**

Table 2-21 • Summary of Maximum and Minimum DC Input Levels Applicable to Military Conditions in all I/O Bank Types

DC I/O Standards	Military*	
	IIL	IIH
	µA	µA
3.3 V LVTTL / 3.3 V LVCMOS	15	15
2.5 V LVCMOS	15	15
1.8 V LVCMOS	15	15
1.5 V LVCMOS	15	15
3.3 V PCI	15	15
3.3 V PCI-X	15	15

*Note: *Military temperature Range: –55°C to 125°C.*

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-22 • Summary of AC Measuring Points Applicable to All I/O Bank Types

Standard	Measuring Trip Point (V_{trip})
3.3 V LVTTL / 3.3 V LVCMOS	1.4 V
2.5 V LVCMOS	1.2 V
1.8 V LVCMOS	0.90 V
1.5 V LVCMOS	0.75 V
3.3 V PCI	0.285 * VCCxxxxIOBx (RR)
	0.615 * VCCxxxxIOBx (FF)
3.3 V PCI-X	0.285 * VCCxxxxIOBx (RR)
	0.615 * VCCxxxxIOBx (FF)
LVDS	Cross point
LVPECL	Cross point

Table 2-23 • I/O AC Parameter Definitions

Parameter	Parameter Definition
t_{DP}	Data to pad delay through the output buffer
t_{PY}	Pad to data delay through the input buffer
t_{DOUT}	Data to output buffer delay through the I/O interface
t_{EOUT}	Enable to output buffer tristate control delay through the I/O interface
t_{DIN}	Input buffer to data delay through the I/O interface
t_{HZ}	Enable to pad delay through the output buffer—High to Z
t_{ZH}	Enable to pad delay through the output buffer—Z to High
t_{LZ}	Enable to pad delay through the output buffer—Low to Z
t_{ZL}	Enable to pad delay through the output buffer—Z to Low
t_{ZHS}	Enable to pad delay through the output buffer with delayed enable—Z to High
t_{ZLS}	Enable to pad delay through the output buffer with delayed enable—Z to Low

Table 2-24 • Summary of I/O Timing Characteristics—Software Default Settings –1 Speed Grade, Worst Military-Case Conditions: T_J = 125°C, Worst Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx (per standard) Applicable to FPGA I/O Banks, Assigned to EMC I/O Pins

I/O Standard	Drive Strength	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	35	–	0.52	3.01	0.03	0.86	0.34	3.06	2.39	2.74	3.02	4.90	4.22	ns
2.5 V LVCMOS	12 mA	High	35	–	0.52	3.03	0.03	1.10	0.34	3.09	2.88	2.81	2.90	4.93	4.72	ns
1.8 V LVCMOS	12 mA	High	35	–	0.52	3.01	0.03	1.02	0.34	3.07	2.55	3.12	3.41	4.91	4.39	ns
1.5 V LVCMOS	12 mA	High	35	–	0.52	3.47	0.03	1.20	0.34	3.54	2.98	3.32	3.50	5.37	4.82	ns
3.3 V PCI	Per PCI spec	High	10	25[1]	0.52	2.26	0.03	0.73	0.34	2.30	1.68	2.73	3.02	4.14	3.52	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25[1]	0.52	2.26	0.03	0.69	0.34	2.30	1.68	2.73	3.02	4.14	3.52	ns
LVDS	24 mA	High	–	–	0.52	1.63	0.03	1.36	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.52	1.57	0.03	1.15	–	–	–	–	–	–	–	ns

Notes:

1. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-41 for connectivity. This resistor is not required during normal operation.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings –1 Speed Grade, Worst Military-Case Conditions: T_J = 125°C, Worst Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx (per standard) Applicable to MSS I/O Banks

I/O Standard	Drive Strength	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	10	–	0.19	2.06	0.08	0.84	1.16	0.19	2.10	1.66	1.96	2.19	ns
2.5 V LVCMOS	8 mA	High	10	–	0.19	2.10	0.08	1.06	1.24	0.19	2.14	1.95	1.95	2.07	ns
1.8 V LVCMOS	4 mA	High	10	–	0.19	2.47	0.08	0.98	1.46	0.19	2.52	2.43	1.97	2.00	ns
1.5 V LVCMOS	2 mA	High	10	–	0.19	2.89	0.08	1.14	1.66	0.19	2.94	2.86	2.00	1.98	ns

Notes:

1. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-41 for connectivity. This resistor is not required during normal operation.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Timing Characteristics

Table 2-51 • 1.8 V LVCMOS High Slew
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.62	11.85	0.04	1.22	0.41	9.22	11.85	2.80	1.70	11.42	14.05	ns
	–1	0.52	9.87	0.03	1.02	0.34	7.68	9.87	2.33	1.42	9.52	11.71	ns
4 mA	Std.	0.62	6.91	0.04	1.22	0.41	5.92	6.91	3.26	2.85	8.13	9.12	ns
	–1	0.52	5.76	0.03	1.02	0.34	4.94	5.76	2.72	2.38	6.77	7.60	ns
6 mA	Std.	0.62	4.46	0.04	1.22	0.41	4.27	4.46	3.58	3.40	6.48	6.66	ns
	–1	0.52	3.71	0.03	1.02	0.34	3.56	3.71	2.98	2.84	5.40	5.55	ns
8 mA	Std.	0.62	3.95	0.04	1.22	0.41	4.02	3.93	3.65	3.55	6.23	6.14	ns
	–1	0.52	3.29	0.03	1.02	0.34	3.35	3.28	3.04	2.96	5.19	5.12	ns
12 mA	Std.	0.62	3.62	0.04	1.22	0.41	3.68	3.06	3.75	4.09	5.89	5.26	ns
	–1	0.52	3.01	0.03	1.02	0.34	3.07	2.55	3.12	3.41	4.91	4.39	ns
16 mA	Std.	0.62	3.62	0.04	1.22	0.41	3.68	3.06	3.75	4.09	5.89	5.26	ns
	–1	0.52	3.01	0.03	1.02	0.34	3.07	2.55	3.12	3.41	4.91	4.39	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-52 • 1.8 V LVCMOS Low Slew
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.62	15.25	0.04	1.22	0.41	14.43	15.25	2.80	1.65	16.63	17.46	ns
	–1	0.52	12.71	0.03	1.02	0.34	12.02	12.71	2.34	1.37	13.86	14.55	ns
4 mA	Std.	0.62	10.43	0.04	1.22	0.41	10.62	10.31	3.27	2.75	12.82	12.51	ns
	–1	0.52	8.69	0.03	1.02	0.34	8.85	8.59	2.72	2.29	10.69	10.42	ns
6 mA	Std.	0.62	8.21	0.04	1.22	0.41	8.36	7.75	3.58	3.30	10.57	9.96	ns
	–1	0.52	6.84	0.03	1.02	0.34	6.97	6.46	2.98	2.75	8.81	8.30	ns
8 mA	Std.	0.62	7.66	0.04	1.22	0.41	7.80	7.22	3.65	3.44	10.01	9.43	ns
	–1	0.52	6.38	0.03	1.02	0.34	6.50	6.02	3.04	2.87	8.34	7.86	ns
12 mA	Std.	0.62	7.24	0.04	1.22	0.41	7.38	7.23	3.75	3.96	9.58	9.43	ns
	–1	0.52	6.04	0.03	1.02	0.34	6.15	6.02	3.13	3.30	7.98	7.86	ns
16 mA	Std.	0.62	7.24	0.04	1.22	0.41	7.38	7.23	3.75	3.96	9.58	9.43	ns
	–1	0.52	6.04	0.03	1.02	0.34	6.15	6.02	3.13	3.30	7.98	7.86	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Timing Characteristics

Table 2-57 • 1.5 V LVCMOS High Slew
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.4 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 m	Std.	0.62	8.35	0.04	1.44	0.41	6.89	8.35	3.42	2.77	9.09	10.55	ns
	–1	0.52	6.95	0.03	1.20	0.34	5.74	6.95	2.85	2.31	7.58	8.79	ns
4 mA	Std.	0.62	5.31	0.04	1.44	0.41	4.94	5.31	3.78	3.41	7.15	7.51	ns
	–1	0.52	4.42	0.03	1.20	0.34	4.12	4.42	3.15	2.85	5.95	6.26	ns
6 mA	Std.	0.62	4.67	0.04	1.44	0.41	4.65	4.67	3.86	3.58	6.85	6.88	ns
	–1	0.52	3.89	0.03	1.20	0.34	3.87	3.89	3.22	2.98	5.71	5.73	ns
8 mA	Std.	0.62	4.17	0.04	1.44	0.41	4.24	3.58	3.98	4.20	6.45	5.78	ns
	–1	0.52	3.47	0.03	1.20	0.34	3.54	2.98	3.32	3.50	5.37	4.82	ns
12 mA	Std.	0.62	4.17	0.04	1.44	0.41	4.24	3.58	3.98	4.20	6.45	5.78	ns
	–1	0.52	3.47	0.03	1.20	0.34	3.54	2.98	3.32	3.50	5.37	4.82	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-58 • 1.5 V LVCMOS Low Slew
Worst Military-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.4 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.62	12.80	0.04	1.44	0.41	13.04	12.53	3.43	2.65	15.24	14.73	ns
	–1	0.52	10.67	0.03	1.20	0.34	10.87	10.44	2.86	2.21	12.70	12.28	ns
4 mA	Std.	0.62	10.18	0.04	1.44	0.41	10.37	9.38	3.79	3.28	12.57	11.59	ns
	–1	0.52	8.48	0.03	1.20	0.34	8.64	7.82	3.16	2.74	10.48	9.66	ns
6 mA	Std.	0.62	9.49	0.04	1.44	0.41	9.67	8.75	3.87	3.45	11.87	10.95	ns
	–1	0.52	7.91	0.03	1.20	0.34	8.05	7.29	3.22	2.87	9.89	9.13	ns
8 mA	Std.	0.62	9.04	0.04	1.44	0.41	9.21	8.76	3.99	4.05	11.41	10.96	ns
	–1	0.52	7.53	0.03	1.20	0.34	7.67	7.30	3.33	3.37	9.51	9.13	ns
12 mA	Std.	0.62	9.04	0.04	1.44	0.41	9.21	8.76	3.99	4.05	11.41	10.96	ns
	–1	0.52	7.53	0.03	1.20	0.34	7.67	7.30	3.33	3.37	9.51	9.13	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-59 • 1.5 V LVCMOS High Slew
Worst Military-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.4 25 V,
Worst-Case VCCxxxxIOBx = 1.4 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.23	3.47	0.09	1.37	2.00	0.23	3.53	3.43	2.40	2.37	ns
	–1	0.19	2.89	0.08	1.14	1.66	0.19	2.94	2.86	2.00	1.98	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

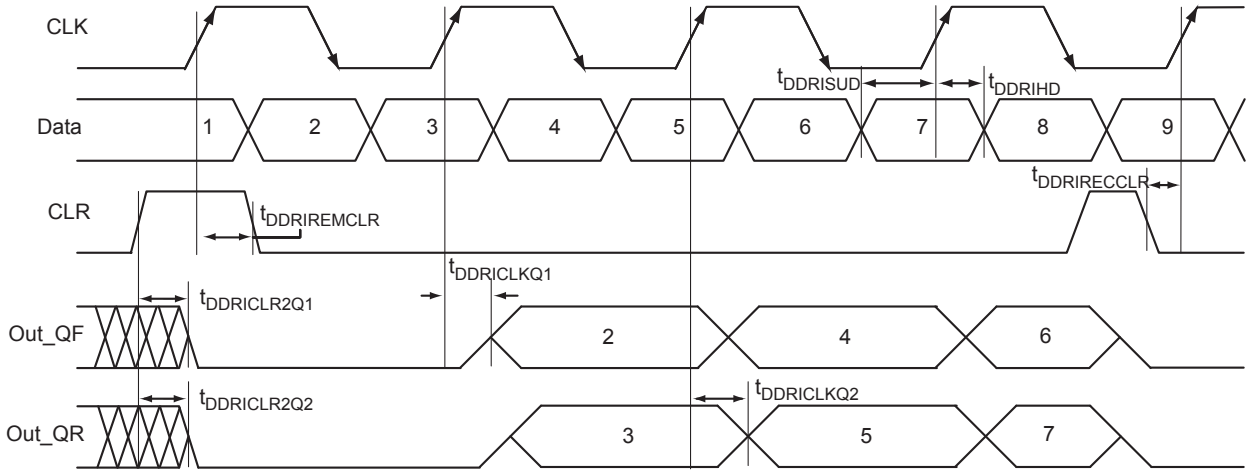

Figure 2-21 • **Input DDR Timing Diagram**

Timing Characteristics

Table 2-76 • **Input DDR Propagation Delays**
Worst Military-Case Conditions: T_J = 85°C, Worst Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.41	0.49	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.29	0.35	ns
$t_{DDRISUD}$	Data Setup for Input DDR	0.30	0.36	ns
t_{DDRIHD}	Data Hold for Input DDR	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.60	0.72	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.49	0.59	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal time for Input DDR	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery time for Input DDR	0.24	0.28	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.22	0.26	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.36	0.42	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.32	0.38	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	350	350	MHz

Note: For derating values at specific junction temperature and voltage-supply levels, refer to Table 2-7 on page 2-9 for derating values.

Timing Characteristics

Table 2-79 • Combinatorial Cell Propagation Delays
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.42	0.51	ns
AND2	Y = A · B	t_{PD}	0.50	0.60	ns
NAND2	Y = !(A · B)	t_{PD}	0.50	0.60	ns
OR2	Y = A + B	t_{PD}	0.51	0.62	ns
NOR2	Y = !(A + B)	t_{PD}	0.51	0.62	ns
XOR2	Y = A ⊕ B	t_{PD}	0.78	0.94	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	0.74	0.88	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.92	1.11	ns
MUX2	Y = A !S + B S	t_{PD}	0.54	0.64	ns
AND3	Y = A · B · C	t_{PD}	0.59	0.71	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

VersaTile Specifications as a Sequential Module

The SmartFusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide*.

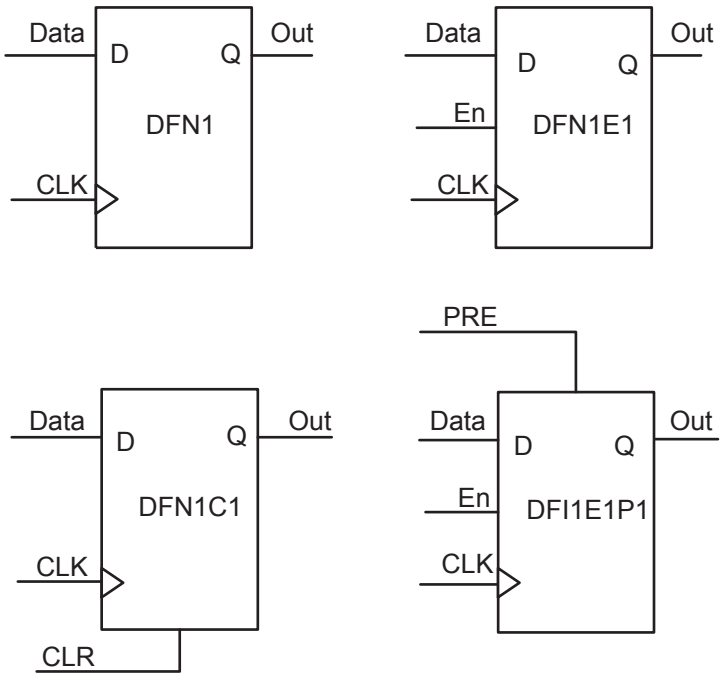

Figure 2-26 • Sample of Sequential Cells

Global Resource Characteristics

A2F500 Clock Tree Topology

Clock delays are device-specific. Figure 2-28 is an example of a global tree used for clock routing. The global tree presented in Figure 2-28 is driven by a CCC located on the west side of the A2F500 device. It is used to drive all D-flip-flops in the device.

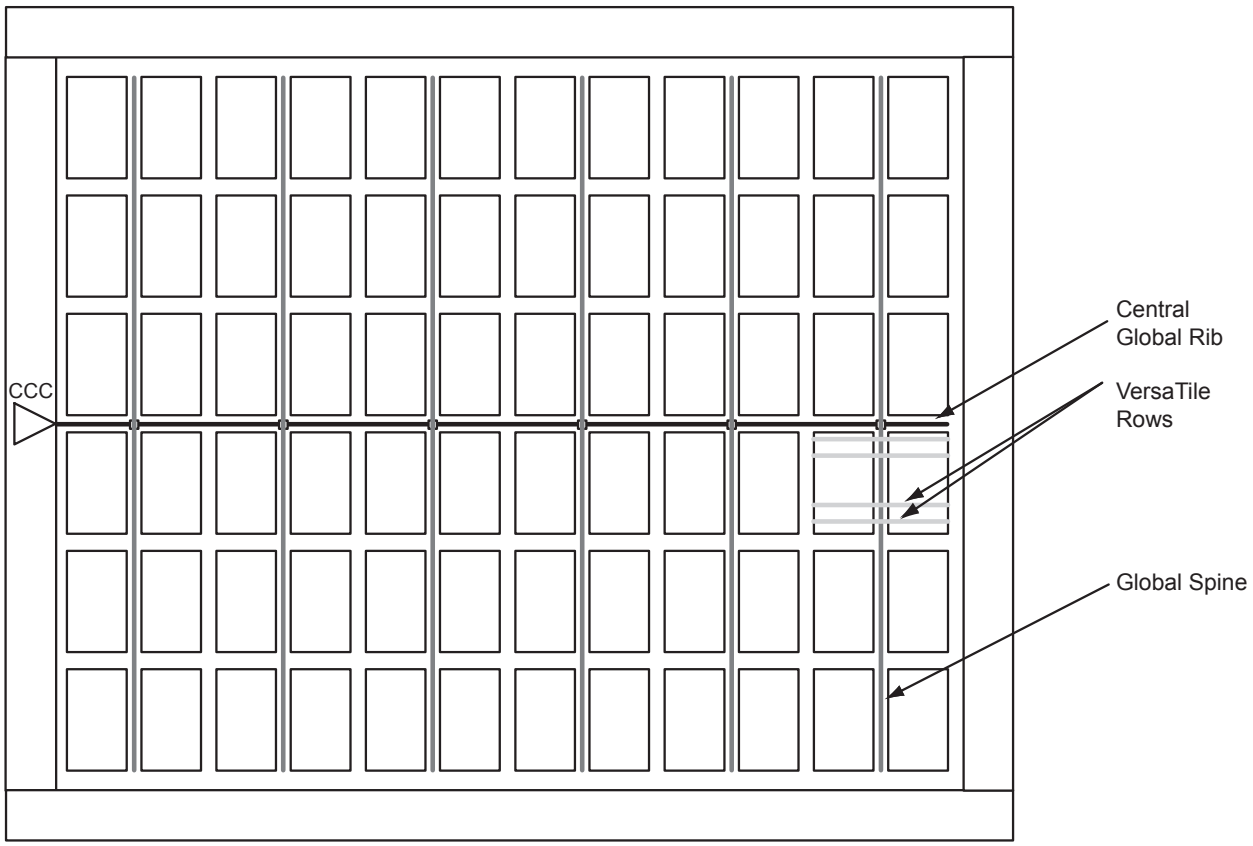

***Figure 2-28* • Example of Global Tree Use in an A2F500 Device for Clock Routing**

Timing Waveforms

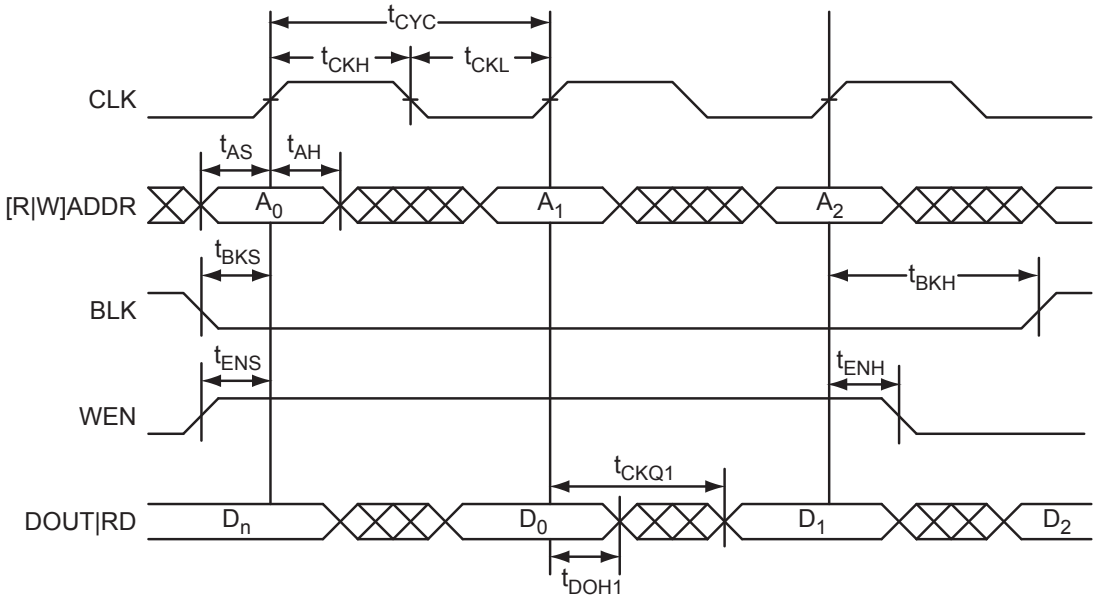

Figure 2-31 • **RAM Read for Pass-Through Output. Applicable to both RAM4K9 and RAM512x18**.

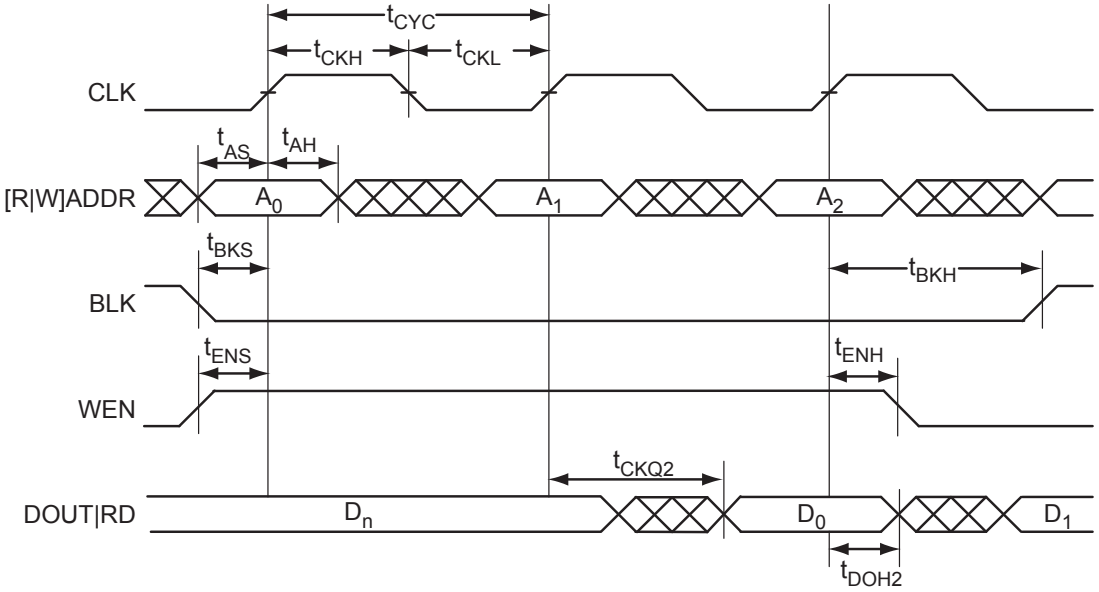

Figure 2-32 • **RAM Read for Pipelined Output Applicable to both RAM4K9 and RAM512x18.**

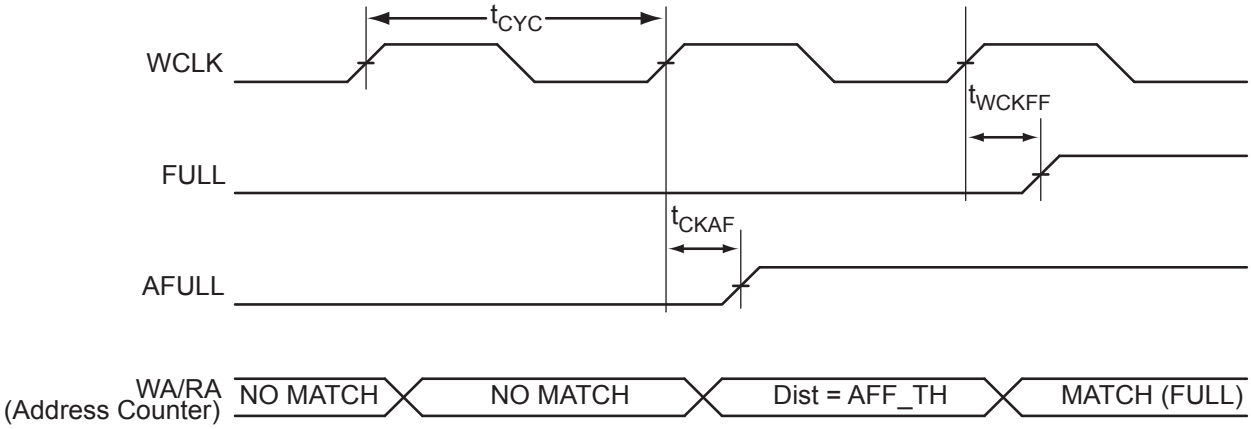

Figure 2-39 • **FIFO FULL Flag and AFULL Flag Assertion**

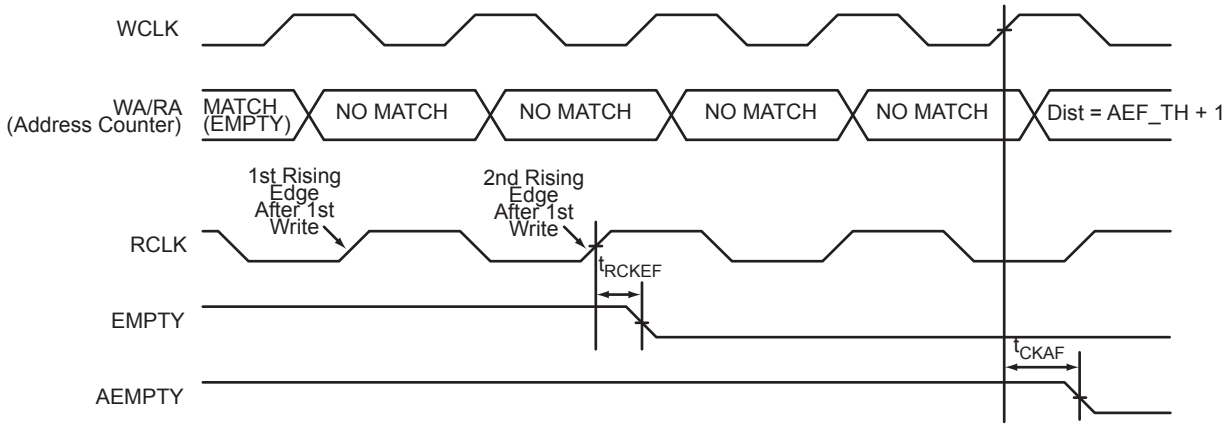

Figure 2-40 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

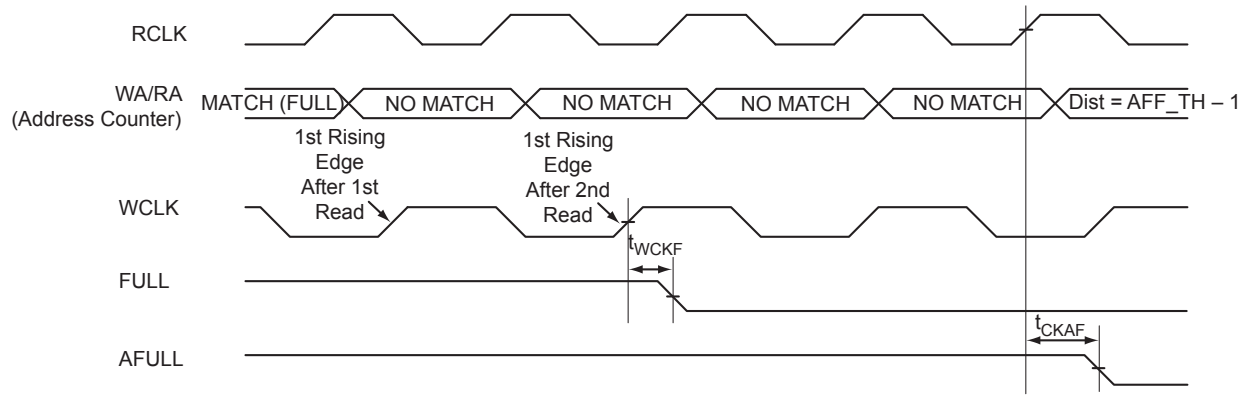

Figure 2-41 • **FIFO FULL Flag and AFULL Flag Deassertion**

Embedded FlashROM (eFROM)

Electrical Characteristics

Table 2-91 describes the eFROM maximum performance

Table 2-91 • **FlashROM Access Time, Worse Military-Case Conditions: T_J = 125°C, VCC = 1.425 V**

Parameter	Description	–1	Std.	Units
F_{max}	Maximum Clock frequency	15.00	15.00	MHz

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-20 for more details.

Timing Characteristics

Table 2-92 • **JTAG 1532**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.53	0.63	ns
t_{DIHD}	Test Data Input Hold Time	1.07	1.25	ns
t_{TMSSU}	Test Mode Select Setup Time	0.53	0.63	ns
t_{TMDHD}	Test Mode Select Hold Time	1.07	1.25	ns
t_{TCK2Q}	Clock to Q (data out)	5.33	6.27	ns
t_{RSTB2Q}	Reset to Q (data out)	21.31	25.07	ns
F_{TCKMAX}	TCK Maximum Frequency	26.00	30.59	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.00	0.00	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.21	0.25	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Comparator

Unless otherwise specified, performance is specified at 25°C with nominal power supply voltages.

Table 2-98 • **Comparator Performance Specifications**

Specification	Test Conditions		Min.	Typ.	Max.	Units
Input voltage range	Minimum			0		V
	Maximum			2.56		V
Input offset voltage	HYS[1:0] = 00 (no hysteresis)			±1	±3	mV
Input bias current	Comparator 1, 3, 5, 7, 9 (measured at 2.56 V)			40	60	nA
	Comparator 0, 2, 4, 6, 8 (measured at 2.56 V)			150	300	nA
Input resistance			10			MΩ
Power supply rejection ratio	DC (0 – 10 KHz)		50	60		dB
Propagation delay	100 mV overdrive					
	HYS[1:0] = 00					
	(no hysteresis)			15	18	ns
	100 mV overdrive					
	HYS[1:0] = 10					
	(with hysteresis)			25	30	ns
Hysteresis (± refers to rising and falling threshold shifts, respectively)	HYS[1:0] = 00	Typical (25°C)	0	0	±5	mV
		Across all corners (–55ºC to +125ºC)	0		±5	mV
	HYS[1:0] = 01	Typical (25°C)	±3	± 16	±30	mV
		Across all corners (–55ºC to +125ºC)	0		±36	mV
	HYS[1:0] = 10	Typical (25°C)	±19	± 31	±48	mV
		Across all corners (–40ºC to +100ºC)	±12		±54	mV
		Across all corners (–55ºC to +125ºC)	±5		±54	mV
	HYS[1:0] = 11	Typical (25°C)	±80	± 105	±190	mV
		Across all corners (–40ºC to +100ºC)	±80		±194	mV
		Across all corners (–55ºC to +125ºC)	±60		±194	mV
Comparator current requirements (per comparator)	VCC33A = 3.3 V (operational mode); COMP_EN = 1					
	VCC33A			150	165	µA
	VCC33AP			140	165	µA
	VCC15A			1	15	µA

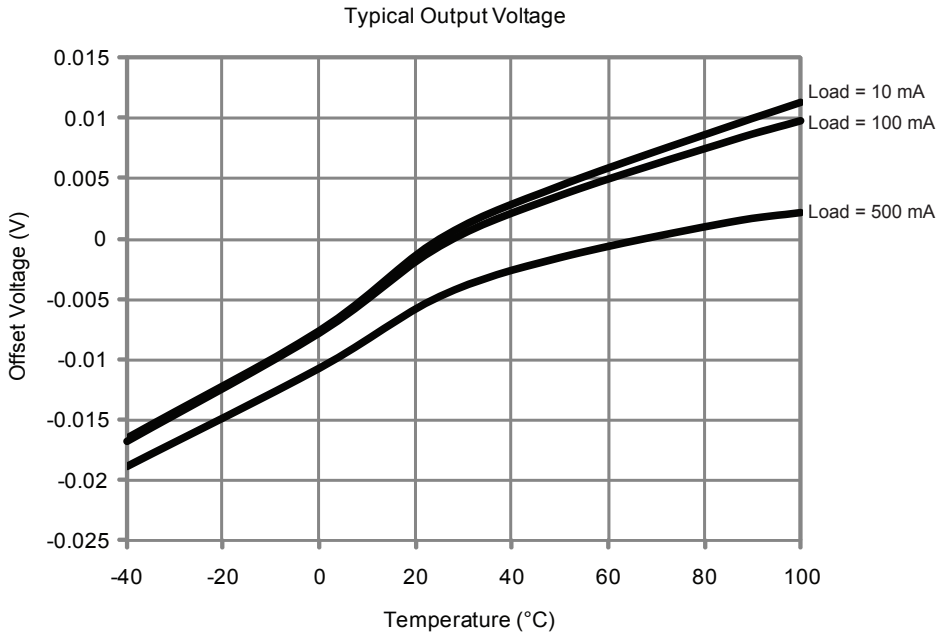

Figure 2-45 • **Typical Output Voltage**

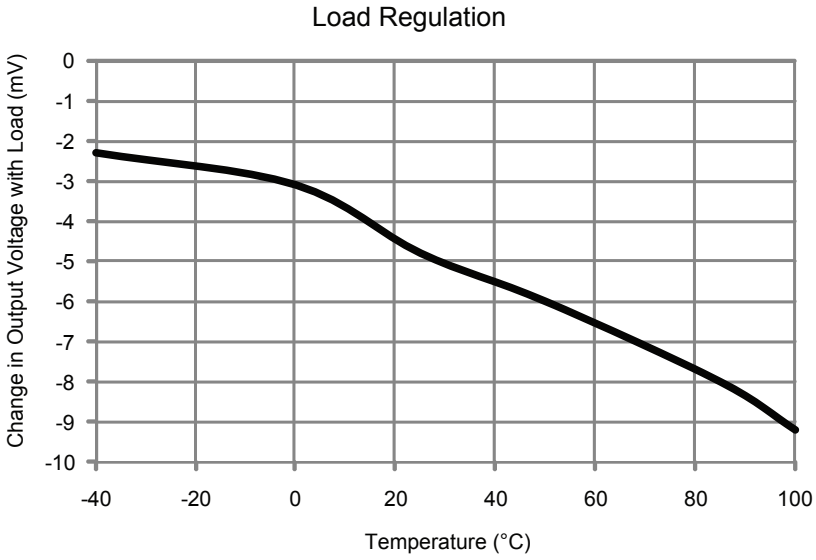

Figure 2-46 • **Load Regulation**

Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to Figure 2-47 on page 2-91.

***Table 2-101* • SPI Characteristics**
Military-Case Conditions: T_J =125ºC, VDD = 1.425 V, –1 Speed Grade

Symbol	Description and Condition	A2F060	A2F500	Unit
sp1	SPI_x_CLK minimum period			
	SPI_x_CLK = PCLK/2	20	20	ns
	SPI_x_CLK = PCLK/4	40	40	ns
	SPI_x_CLK = PCLK/8	80	80	ns
	SPI_x_CLK = PCLK/16	0.16	0.16	µs
	SPI_x_CLK = PCLK/32	0.32	0.32	µs
	SPI_x_CLK = PCLK/64	0.64	0.64	µs
	SPI_x_CLK = PCLK/128	1.28	1.28	µs
	SPI_x_CLK = PCLK/256	2.56	2.56	µs
sp2	SPI_x_CLK minimum pulse width high			
	SPI_x_CLK = PCLK/2	10	10	ns
	SPI_x_CLK = PCLK/4	20	20	ns
	SPI_x_CLK = PCLK/8	40	40	ns
	SPI_x_CLK = PCLK/16	0.08	0.08	µs
	SPI_x_CLK = PCLK/32	0.16	0.16	µs
	SPI_x_CLK = PCLK/64	0.32	0.32	µs
	SPI_x_CLK = PCLK/128	0.64	0.64	µs
	SPI_x_CLK = PCLK/256	1.28	1.28	us
sp3	SPI_x_CLK minimum pulse width low			
	SPI_x_CLK = PCLK/2	10	10	ns
	SPI_x_CLK = PCLK/4	20	20	ns
	SPI_x_CLK = PCLK/8	40	40	ns
	SPI_x_CLK = PCLK/16	0.08	0.08	µs
	SPI_x_CLK = PCLK/32	0.16	0.16	µs
	SPI_x_CLK = PCLK/64	0.32	0.32	µs
	SPI_x_CLK = PCLK/128	0.64	0.64	µs
	SPI_x_CLK = PCLK/256	1.28	1.28	µs
sp4	SPI_x_CLK, SPI_x_DO, SPI_x_SS rise time (10%-90%) [1]	4.7	4.7	ns
sp5	SPI_x_CLK, SPI_x_DO, SPI_x_SS fall time (10%-90%) [1]	3.4	3.4	ns

Notes:

1. *These values are provided for a load of 35 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion Microcontroller Subsystem User's Guide.*

SmartFusion Ecosystem

The Microsemi SoC Products Group has a long history of supplying comprehensive FPGA development tools and recognizes the benefit of partnering with industry leaders to deliver the optimum usability and productivity to customers. Taking the same approach with processor development, Microsemi has partnered with key industry leaders in the microcontroller space to provide the robust SmartFusion ecosystem.

Microsemi is partnering with Keil and IAR to provide Software IDE support to SmartFusion system designers. The result is a robust solution that can be easily adopted by developers who are already doing embedded design. The learning path is straightforward for FPGA designers.

Support for the SoC Products Group device and ecosystem resources is represented in Figure 3-3.

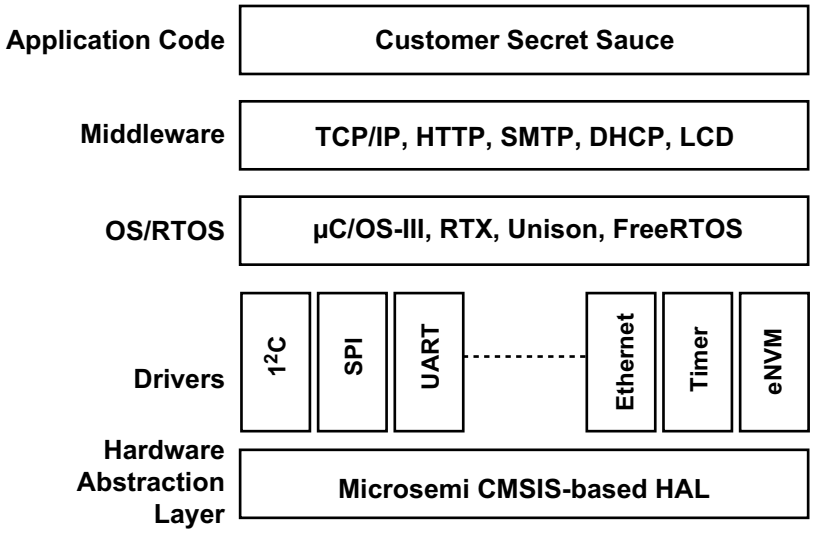

Figure 3-3 • **SmartFusion Ecosystem**

Figure 3-3 shows the SmartFusion stack with examples of drivers, RTOS, and middleware from Microsemi and partners. By leveraging the SmartFusion stack, designers can decide at which level to add their own customization to their design, thus speeding time to market and reducing overhead in the design.

ARM

Because an ARM processor was chosen for SmartFusion cSoCs, Microsemi's customers can benefit from the extensive ARM ecosystem. By building on Microsemi supplied hardware abstraction layer (HAL) and drivers, third party vendors can easily port RTOS and middleware for the SmartFusion cSoC.

- ARM Cortex-M Series Processors
- ARM Cortex-M3 Processor Resource
- ARM Cortex-M3 Technical Reference Manual
- *ARM Cortex-M3 Processor Software Development for ARM7TDMI Processor Programmers* White Paper

4 – SmartFusion Programming

SmartFusion cSoCs have three separate flash areas that can be programmed:

1. The FPGA fabric
2. The embedded nonvolatile memories (eNVMs)
3. The embedded flash ROM (eFROM)

There are essentially three methodologies for programming these areas:

1. In-system programming (ISP)
2. In-application programming (IAP)
   – FPGA fabric, eNVM, and eFROM
3. Pre-programming (non-ISP)

Programming, whether ISP or IAP methodologies are employed, can be done in two ways:

1. Securely using the on chip AES decryption logic
2. In plain text

In-System Programming

In-System Programming is performed with the aid of external JTAG programming hardware. Table 4-1 describes the JTAG programming hardware that will program a SmartFusion cSoC and Table 4-2 defines the JTAG pins that provide the interface for the programming hardware.

***Table 4-1* • Supported JTAG Programming Hardware**

Dongle	Source	JTAG	SWD[1]	SWV[2]	Program FPGA	Program eFROM	Program eNVM
FlashPro3/4	SoC Products Group	Yes	No	No	Yes	Yes	Yes
ULINK Pro	Keil	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes
ULINK2	Keil	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes
IAR J-Link	IAR	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes

Notes:

1. *SWD = ARM Serial Wire Debug*
2. *SWV = ARM Serial Wire Viewer*
3. *Planned support*

***Table 4-2* • JTAG Pin Descriptions**

Pin Name	Description
JTAGSEL	ARM Cortex-M3 or FPGA test access port (TAP) controller selection
TRSTB	Test reset bar
TCK	Test clock
TMS	Test mode select
TDI	Test data input
TDO	Test data output

Special Function Pins

Name	Type	Polarity/Bus Size	Description
NC			No connect This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.
DC			Do not connect. This pin should not be connected to any signals on the PCB. These pins should be left unconnected.
LPXIN	In	1	Low power 32 KHz crystal oscillator. Input from the 32 KHz oscillator. Pin for connecting a low power 32 KHz watch crystal. If not used, the LPXIN pin can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
LPXOUT	In	1	Low power 32 KHz crystal oscillator. Output to the 32 KHz oscillator. Pin for connecting a low power 32 KHz watch crystal. If not used, the LPXOUT pin can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
MAINXIN	In	1	Main crystal oscillator circuit. Input to the crystal oscillator circuit. Pin for connecting an external crystal, ceramic resonator, or RC network. When using an external crystal or ceramic oscillator, external capacitors are also recommended. Refer to documentation from the crystal oscillator manufacturer for proper capacitor value. If using an external RC network or clock input, MAINXIN should be grounded for better noise immunity. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
MAINXOUT	Out	1	Main crystal oscillator circuit. Output from the crystal oscillator circuit. Pin for connecting external crystal or ceramic resonator. When using an external crystal or ceramic oscillator, external capacitors are also recommended. Refer to documentation from the crystal oscillator manufacturer for proper capacitor value. If using external RC network or clock input, MAINXIN should be grounded and MAINXOUT left unconnected. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
NCAP		1	Negative capacitor connection. This is the negative terminal of the charge pump. A capacitor, with a 2.2 µF recommended value, is required to connect between PCAP and NCAP. Analog charge pump capacitors are not needed if none of the analog SCB features are used and none of the SDDs are used. In that case it should be left unconnected.

Name	Type	Description	Associated With	
			ADC/SDD	SCB
TM0	In	SCB 0 / low side of current monitor / comparator Negative input / high side of temperature monitor. See the Temperature Monitor section.	ADC0	SCB0
TM1	In	SCB 1 / low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC0	SCB1
TM2	In	SCB 2 / low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC1	SCB2
TM3	In	SCB 3 low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC1	SCB3
TM4	In	SCB 4 low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC2	SCB4
SDD0	Out	Output of SDD0 See the Sigma-Delta Digital-to-Analog Converter (DAC) section in the *SmartFusion Programmable Analog User's Guide*.	SDD0	N/A
SDD1	Out	Output of SDD1	SDD1	N/A
SDD2	Out	Output of SDD2	SDD2	N/A

Note: Unused analog inputs should be grounded. This aids in shielding and prevents an undesired coupling path.