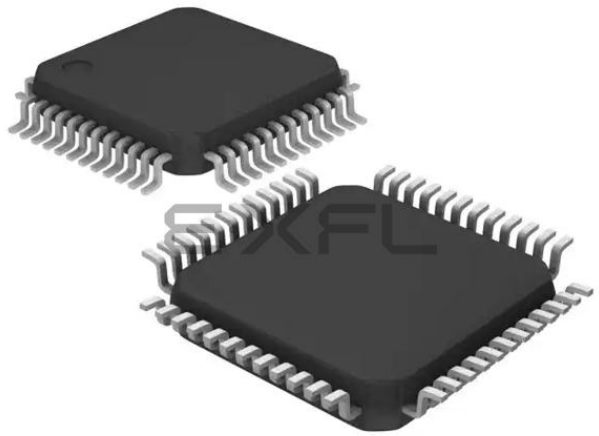

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m058lan

LIST OF FIGURES

2 FEATURES

- Core
  - ARM® Cortex™-M0 core runs up to 50 MHz.
  - One 24-bit system timer.
  - Supports low power sleep mode.
  - A single-cycle 32-bit hardware multiplier.
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority.
  - Supports Serial Wire Debug (SWD) interface and 2 watchpoints/4 breakpoints.
- Built-in LDO for Wide Operating Voltage Range: 2.5V to 5.5V
- Memory
  - 32KB/64KB Flash memory for program memory (APROM)
  - 4KB Flash memory for data memory (DataFlash)
  - 4KB Flash memory for loader (LDROM)
  - 4KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
  - External 4~24 MHz high speed crystal input
  - Internal 22.1184 MHz high speed oscillator (trimmed to 1% accuracy)
  - Internal 10 kHz low speed oscillator for Watchdog Timer
  - PLL allows CPU operation up to the maximum 50MHz
- I/O Port
  - Up to 40 general-purpose I/O (GPIO) pins for LQFP-48 package
  - Four I/O modes:
    - Quasi bi-direction

4 SELECTION TABLE

NuMicro M051™ Series Selection Guide

Part No.	APROM	RAM	Data Flash	LDROM	I/O	Timer	Connectivity			PWM	ADC	EBI	ISP ICP	Package
							UART	SPI	I2C					
M058LAN	32KB	4KB	4KB	4KB	40	4x32-bit	2	2	1	8	8x12-bit	v	v	LQFP48
M058ZAN	32KB	4KB	4KB	4KB	24	4x32-bit	2	1	1	5	5x12-bit		v	QFN 33
M0516LAN	64KB	4KB	4KB	4KB	40	4x32-bit	2	2	1	8	8x12-bit	v	v	LQFP48
M0516ZAN	64KB	4KB	4KB	4KB	24	4x32-bit	2	1	1	5	5x12-bit		v	QFN 33

Table 4–1 NuMicro™ M051 Series Product Selection Guide

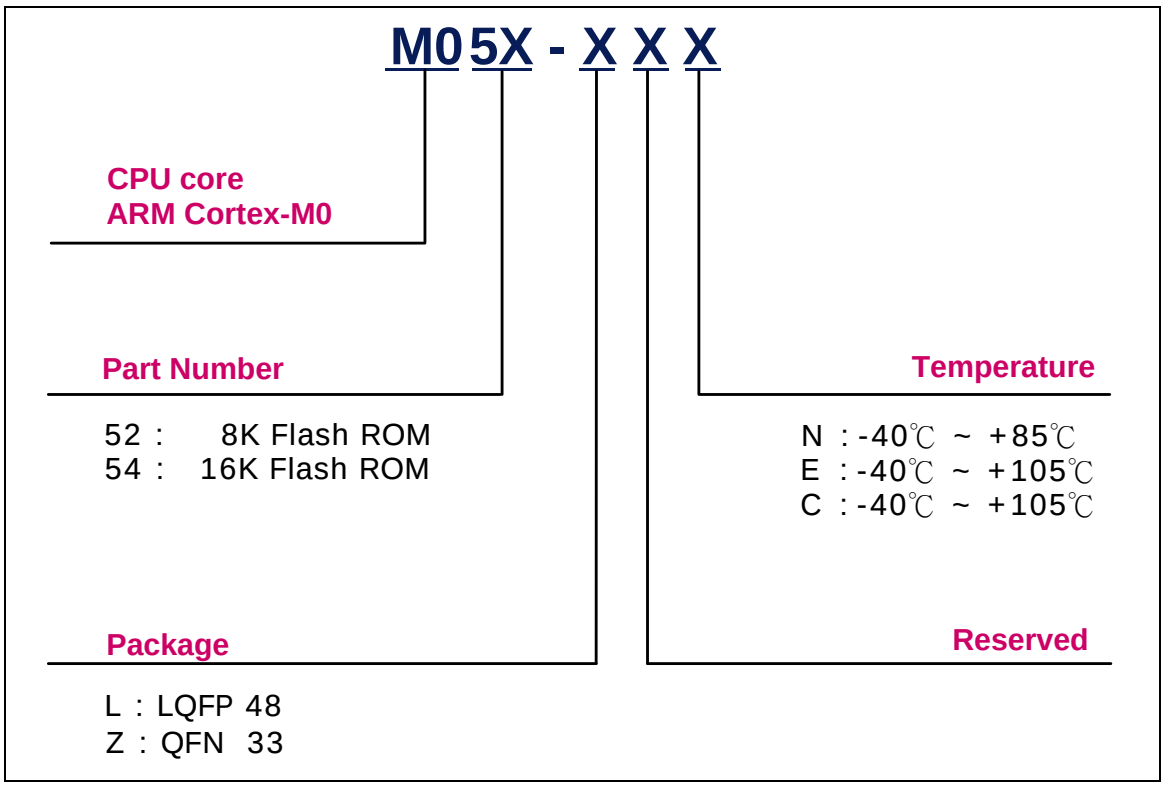

Figure 4–1 NuMicro M051™ Naming Rule

5.3 Pin Description

Pin number		Symbol	Alternate Function		Type[1]	Description
QFN33	LQFP48		1	2		
11	16	XTAL1			I (ST)	**CRYSTAL1:** This is the input pin to the internal inverting amplifier. The system clock is from external crystal or resonator when FOSC[1:0] (CONFIG3[1:0]) are both logic 1 by default.
10	15	XTAL2			O	**CRYSTAL2:** This is the output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1.
27	41	VDD			P	**POWER SUPPLY:** Supply voltage **Digital** V_{DD} for operation.
12 33	17	VSS			P	**GROUND: Digital** Ground potential.
28	42	AVDD			P	**POWER SUPPLY:** Supply voltage **Analog** AV_{DD} for operation.
4	6	AVSS			P	**GROUND: Analog** Ground potential.
13	18	LDO_CAP			P	**LDO:** LDO output pin **Note: It needs to be connected with a 10uF capacitor.**
2	4	/RST			I (ST)	**RESET:** /RST pin is a Schmitt trigger input pin for hardware device reset. A "**Low"** on this pin for 768 clock counter of Internal 22.1184 MHz high speed oscillator while the system clock is running will reset the device. /RST pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
26	40	P0.0	CTS1	AD0	D, I/O	**PORT0:** Port 0 is an 8-bit four mode output pin and two mode input. Its multifunction pins are for CTS1, RTS1, CTS0, RTS0, SPISS1, MOSI_1, MISO_1, and SPICLK1. P0 has an alternative function as AD[7:0] while external memory interface (EBI) is enabled. These pins which are SPISS1, MOSI_1, MISO_1, and SPICLK1 for the SPI function used. CTS0/1: Clear to Send input pin for UART0/1
25	39	P0.1	RTS1	AD1	D, I/O	
NC	38	P0.2	CTS0	AD2	D, I/O	
NC	37	P0.3	RTS0	AD3	D, I/O	
24	35	P0.4	SPISS1	AD4	D, I/O	

Pin number		Symbol	Alternate Function		Type[1]	Description
QFN33	LQFP48		1	2		
23	34	P0.5	MOSI_1	AD5	D, I/O	RTS0/1: Request to Send output pin for UART0/1
22	33	P0.6	MISO_1	AD6	D, I/O	
21	32	P0.7	SPICLK1	AD7	D, I/O	
29	43	P1.0	T2	AIN0	I/O	**PORT1:** Port 1 is an 8-bit four mode output pin and two mode input. Its multifunction pins are for T2, T3, RXD1, TXD1, SPISS0, MOSI_0, MISO_0, and SPICLK0. T2: Timer2 external input T3: Timer3 external input These pins which are SPISS0, MOSI_0, MISO_0, and SPICLK0 for the SPI function used. These pins which are AIN0~AIN7for the 12 bits ADC function used. The RXD1/TXD1 pins are for UART1 function used.
NC	44	P1.1	T3	AIN1	I/O	
30	45	P1.2	RXD1	AIN2	I/O	
31	46	P1.3	TXD1	AIN3	I/O	
32	47	P1.4	SPISS0	AIN4	I/O	
1	1	P1.5	MOSI_0	AIN5	I/O	
NC	2	P1.6	MISO_0	AIN6	I/O	
NC	3	P1.7	SPICLK0	AIN7	I/O	
NC	19	P2.0	PWM0	AD8	D, I/O	**PORT2:** Port 2 is an 8-bit four mode output pin and two mode input. It has an alternative function P2 has an alternative function as AD[15:8] while external memory interface (EBI) is enabled. These pins which are PWM0~PWM7 for the PWM function.
NC	20	P2.1	PWM1	AD9	D, I/O	
14	21	P2.2	PWM2	AD10	D, I/O	
15	22	P2.3	PWM3	AD11	D, I/O	
16	23	P2.4	PWM4	AD12	D, I/O	
17	25	P2.5	PWM5	AD13	D, I/O	
18	26	P2.6	PWM6	AD14	D, I/O	
NC	27	P2.7	PWM7	AD15	D, I/O	
3	5	P3.0	RXD		I/O	**PORT3:** Port 3 is an 8-bit four mode output pin and two mode input. Its multifunction pins are for RXD, TXD, $\overline{INT0}$,
5	7	P3.1	TXD		I/O	

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex™-M0 Core

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex-M profile processor. The profile supports two modes -Thread and Handler modes. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return.

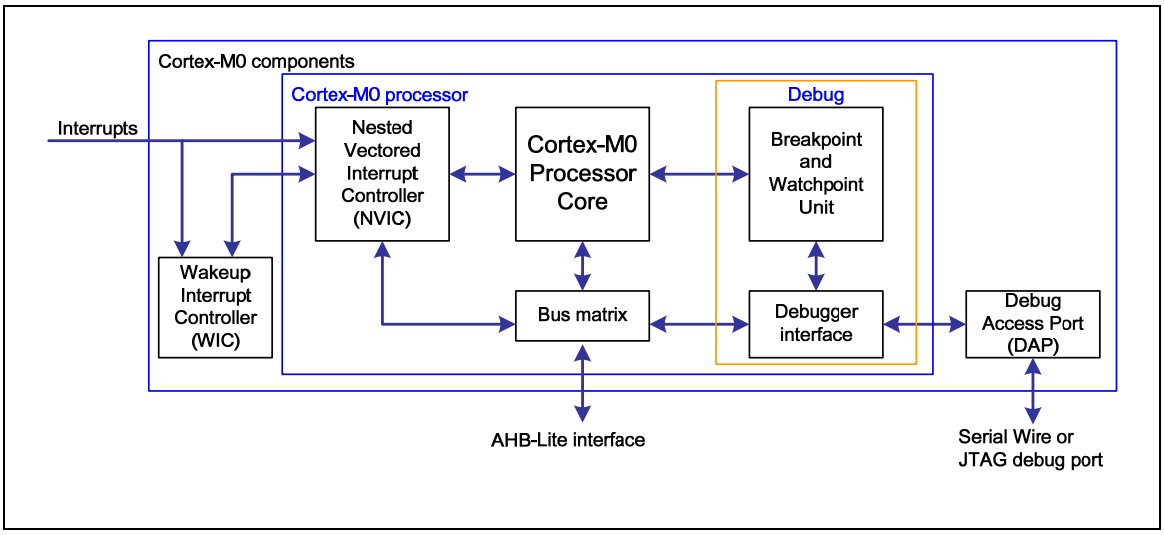

Figure 6-1 Functional Block Diagram

The implemented device provides:

A low gate count processor the features:

- The ARMv6-M Thumb® instruction set.
- Thumb-2 technology.
- ARMv6-M compliant 24-bit SysTick timer.
- A 32-bit hardware multiplier.
- The system interface supports little-endian data accesses.
- The ability to have deterministic, fixed-latency, interrupt handling.

6.2 System Manager

6.2.1 Overview

The following functions are included in system manager section

- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip module reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset includes one of the list below event occurs. For these reset event flags can be read by RSTRC register.

- The Power-On Reset (POR)
- The low level on the /RESET pin
- Watchdog Time Out Reset (WDT)
- Low Voltage Reset (LVR)
- Brown-Out-Detected Reset (BOD)
- CPU Reset
- System Reset

6.2.3 System Power Architecture

In this device, the power architecture is divided into three segments.

- Analog power from AVDD and AVSS provides the power for analog module operation.
- Digital power from VDD and VSS supplies the power to the internal regulator which provides a fixed 2.5V power for digital operation and I/O pins.

The outputs of internal voltage regulator, which is LDO, require an external capacitor which

should be located close to the corresponding pin. The Figure 6-2 shows the power architecture of this device.

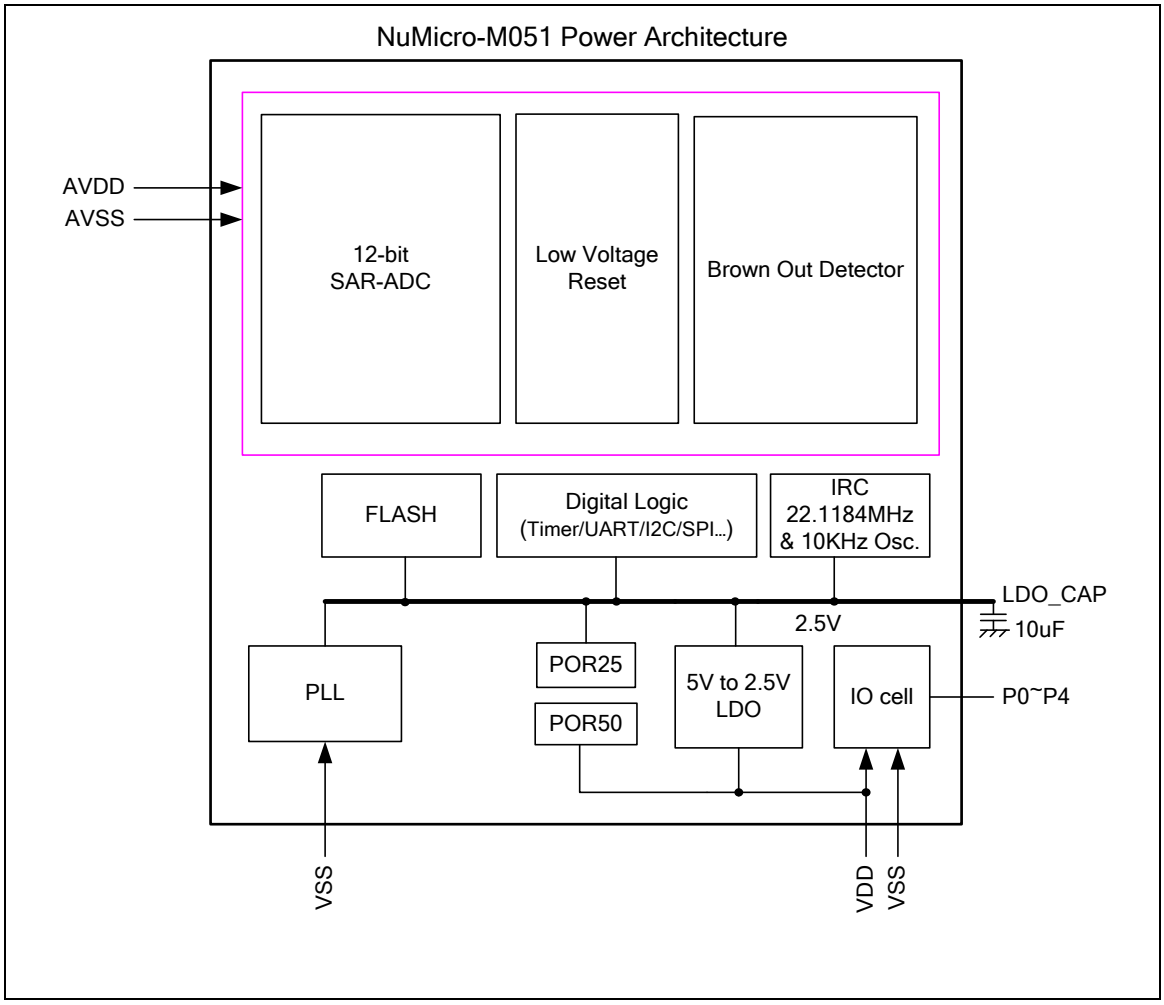

Figure 6-2 NuMicro M051™ Series Power Architecture Diagram

6.2.7 Nested Vectored Interrupt Controller (NVIC)

Cortex-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)". It is closely coupled to the processor kernel and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Dynamic priority changing
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When any interrupts is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the documents "ARM® Cortex™-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

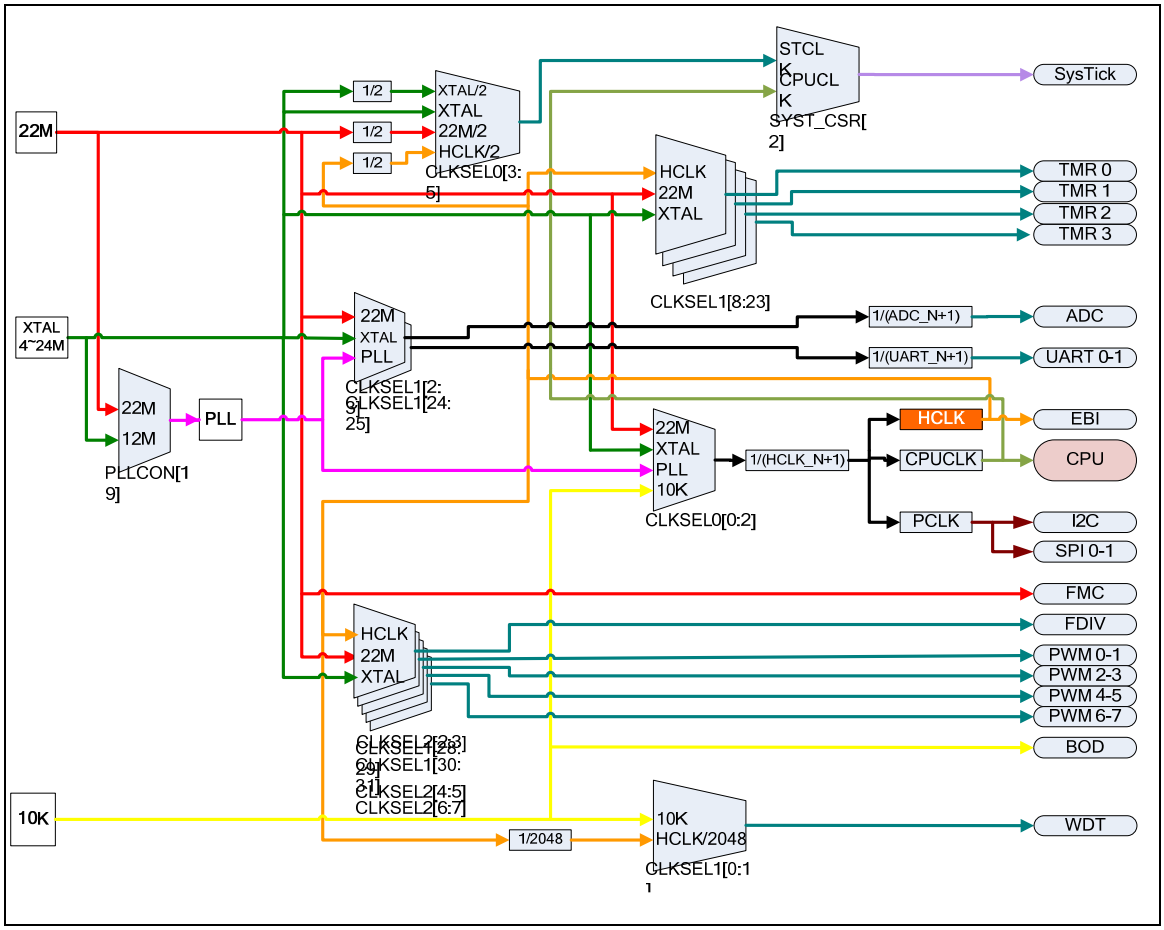

Figure 6-3 Whole Chip Clock generator block diagram

6.3.3 System Clock and SysTick Clock

The system clock has 4 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S(CLKSEL0[2:0]). The block diagram is shown in the Figure 6-5.

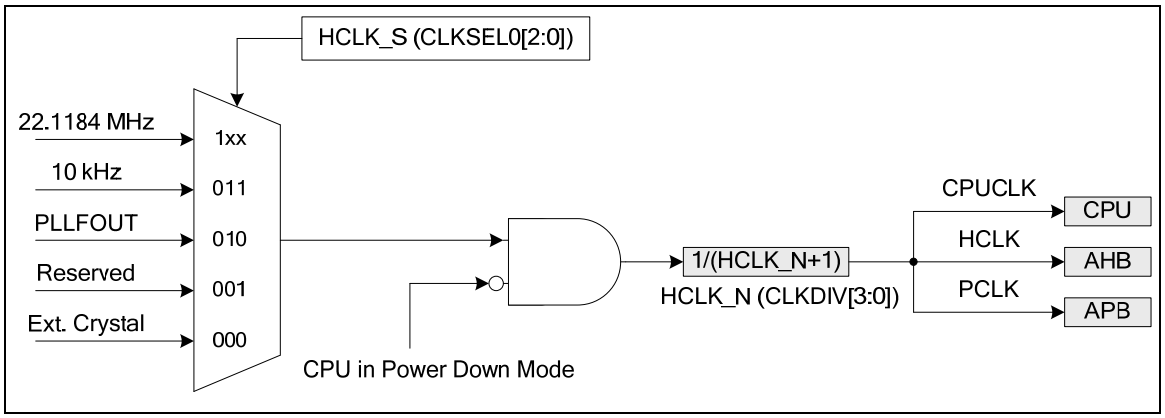

Figure 6-5 System Clock Block Diagram

The clock source of SysTick in Cortex-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]. The block diagram is shown in the Figure 6-6.

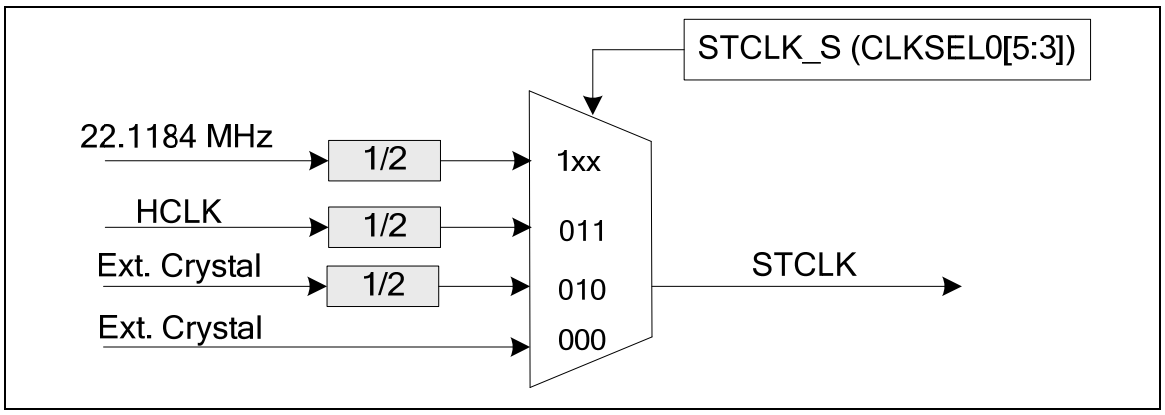

Figure 6-6 SysTick clock Control Block Diagram

6.3.6 Power Down Mode Clock

When chip enter into power down mode, most of clock sources, peripheral clocks and system clock will be disabled. Some of clock sources and peripherals clock are still active in power down mode.

For theses clocks which still keep active list below:

Clock Generator

- Internal 10 kHz low speed oscillator clock

Peripherals Clock (When these IP adopt internal 10 kHz low speed oscillator as clock source)

CCR0.CFL_IE0[2]] (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CCR0.CRL_IE1[17] and CCR0.CFL_IE1[18]. And capture channel 0 to channel 3 on each group have the same feature by setting the corresponding control bits in CCR0 and CCR2. For each group, whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, they are: Read PIIR to get interrupt source and Read CRLRx/CFLRx(x=0 and 3) to get capture value and finally write 1 to clear PIIR. If interrupt latency will take time T0 to finish, the capture signal mustn't transition during this interval (T0). In this case, the maximum capture frequency will be 1/T0. For example:

HCLK = 50 MHz, PWM_CLK = 25 MHz, Interrupt latency is 900 ns

So the maximum capture frequency will is 1/900ns ≈ 1000 kHz

6.6.2 Features

6.6.2.1 PWM function features:

PWM group has two PWM generators. Each PWM generator supports one 8-bit prescaler, one clock divider, two PWM-timers (down counter), one dead-zone generator and two PWM outputs.

- Up to 16 bits resolution
- PWM Interrupt request synchronized with PWM period
- One-shot or Auto-reload mode PWM
- Up to 2 PWM group (PWMA/PWMB) to support 8 PWM channels

6.6.2.2 Capture Function Features:

- Timing control logic shared with PWM Generators
- 8 capture input channels shared with 8 PWM output channels
- Each channel supports one rising latch register (CRLR), one falling latch register (CFLR) and Capture interrupt flag (CAPIFx)

6.8 Timer Controller

6.8.1 Overview

The timer controller includes four 32-bit timers, TIMER0~TIMER3, which allows user to easily implement a timer control for applications. The timer can perform functions like frequency measurement, interval measurement, clock generation, delay timing, and so on. The timer can generates an interrupt signal upon timeout, or provide the current value of count during operation.

6.8.2 Features

- 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Independent clock source for each timer.
- 24-bit timer value is readable through TDR (Timer Data Register)
- Provides one-shot, periodic, toggle and continuous counting operation modes.
- Time out period = (Period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^24), T is the period of timer clock

101	$2^{14} * T_{WDT}$	$1024 * T_{WDT}$	1.6384 s ~ 1.7408 s
110	$2^{16} * T_{WDT}$	$1024 * T_{WDT}$	6.5536 s ~ 6.656 s
111	$2^{18} * T_{WDT}$	$1024 * T_{WDT}$	26.2144 s ~ 26.3168 s

Table 6-2 Watchdog Timeout Interval Selection

6.9.2 Features

- 18-bit free running counter to avoid chip from Watchdog timer reset before the delay time expires.
- Selectable time-out interval (2^4 ~ 2^{18}) and the time out interval is 104 ms ~ 26.3168 s (if WDT_CLK = 10 kHz).
- Reset period = (1 / 10 kHz) * 63, if WDT_CLK = 10 kHz.

control provided by RTS pin or can program GPIO (P0.3 for RTS0 and P0.1 for RTS 1) to implement the function by software. The RS-485 mode is selected by setting the UA_FUN_SEL register to select RS-485 function. The RS-485 driver control is implemented using the RTS control signal from an asynchronous serial port to enable the RS-485 driver. In RS-485 mode, many characteristics of the RX and TX are same as UART.

- Channel 7 supports 2 input sources: external analog voltage and internal bandgap voltage.
- Support Self-calibration to minimize conversion error.

8.3.4 Internal 22.1184 MHz High Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	22.1184		MHz
Calibrated Internal Oscillator Frequency	+25 C; V_{DD} =5V	-1	-	+1	%
	-40 C~+85 C; V_{DD}=2.5V~5.5V	-3	-	+3	%
Accuracy of Un-calibrated Internal Oscillator Frequency	-40 C~+85 C; V_{DD}=2.5V~5.5V	-25	-	+25	%
Operating current	V_{DD} =5V	-	500	-	uA

8.3.5 Internal 10 kHz Low Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25 C; V_{DD} =5V	-30	-	+30	%
	-40 C~+85 C; V_{DD}=2.5V~5.5V	-50	-	+50	%
Operating current	V_{DD} =5V	-	5	-	uA

Notes:

1. Internal operation voltage comes form LDO.

8.5 SPI Dynamic characteristics

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
SPI master mode (VDD = 4.5V ~ 5.5V, 30pF loading Capacitor)					
t_{DS}	Data setup time	26	-	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	-	6	ns
SPI master mode (VDD = 3.0V ~ 3.6V, 30pF loading Capacitor)					
t_{DS}	Data setup time	39	-	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	-	10	ns
SPI slave mode (VDD = 4.5V ~ 5.5V, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+4	-	-	ns
t_V	Data output valid time	-	-	2*PCLK+27	ns
SPI slave mode (VDD = 3.0V ~ 3.6V, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+8	-	-	ns
t_V	Data output valid time	-	-	2*PCLK+40	ns