Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8SX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, IrDA, SCI, SmartCard, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	92
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f61664rd50fpv

Classification	Pin Name	I/O	Description
16-bit timer pulse unit (TPU)	TIOCA5 TIOCB5	Input/ output	Signals for TGRA_5 and TGRB_5. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TCLKE TCLKF TCLKG TCLKH	Input	Input pins for external clock signals.
	TIOCA6 TIOCB6 TIOCC6 TIOCD6	Input/ output	Signals for TGRA_6 to TGRD_6. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA7 TIOCB7	Input/ output	Signals for TGRA_7 and TGRB_7. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA8 TIOCB8	Input/ output	Signals for TGRA_8 and TGRB_8. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA9 TIOCB9 TIOCC9 TIOCD9	Input/ output	Signals for TGRA_9 to TGRD_9. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA10 TIOCB10	Input/ output	Signals for TGRA_10 and TGRB_10. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA11 TIOCB11	Input/ output	Signals for TGRA_11 and TGRB_11. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
Programmable pulse generator (PPG)	PO31 to PO0	Output	Output pins for the pulse signals.
8-bit timer (TMR)	TMO0 to TMO3	Output	Output pins for the compare match signals.
	TMCI0 to TMCI3	Input	Input pins for the external clock signals that drive for the counters.
	TMRI0 to TMRI3	Input	Input pins for the counter-reset signals.
Watchdog timer (WDT)	$\overline{\text{WDTOVF}}$	Output	Output pin for the counter-overflow signal in watchdog-timer mode.

6.5 Address Error

6.5.1 Address Error Source

Instruction fetch, stack operation, or data read/write shown in table 6.5 may cause an address error.

Table 6.5 Bus Cycle and Address Error

	Bus Cycle		
Type	**Bus Master**	**Description**	**Address Error**
Instruction fetch	CPU	Fetches instructions from even addresses	No (normal)
		Fetches instructions from odd addresses	Occurs
		Fetches instructions from areas other than on-chip peripheral module space*[1]	No (normal)
		Fetches instructions from on-chip peripheral module space*[1]	Occurs
		Fetches instructions from external memory space in single-chip mode	Occurs
		Fetches instructions from access prohibited area.*[2]	Occurs
Stack operation	CPU	Accesses stack when the stack pointer value is even address	No (normal)
		Accesses stack when the stack pointer value is odd address	Occurs
Data read/write	CPU	Accesses word data from even addresses	No (normal)
		Accesses word data from odd addresses	No (normal)
		Accesses external memory space in single-chip mode	Occurs
		Accesses to access prohibited area*[2]	Occurs
Data read/write	DTC or DMAC	Accesses word data from even addresses	No (normal)
		Accesses word data from odd addresses	No (normal)
		Accesses external memory space in single-chip mode	Occurs
		Accesses to access prohibited area*[2]	Occurs

6.8 Stack Status after Exception Handling

Figure 6.3 shows the stack after completion of exception handling.

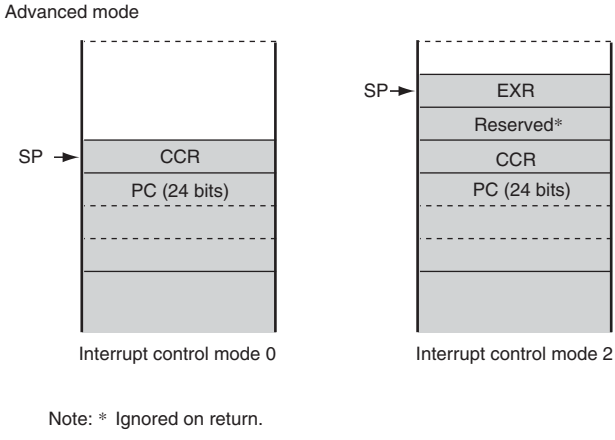


Figure 6.3 Stack Status after Exception Handling

(2) RAS Down Mode and RAS Up Mode

Even if the fast-page mode is selected, the DRAM space is not consecutively accessed and other spaces may be accessed. The $\overline{RAS}$ signal can be held low during other space accesses. The fast-page mode access can be resumed (burst access) when the same row address in the DRAM space is accessed.

(a) RAS Down Mode

Set the RCDM and BE bits in DRAMCR to 1 to make a transition to the RAS down mode.

The RCDM bit is enabled only when the BE bit is set to 1.

The fast-page mode access (burst access) is resumed when the row addresses of the current cycle and previous cycle are the same. While other spaces are accessed when the DRAM space access is halted, the $\overline{RAS}$ signal must be low. Figure 9.50 shows a timing example of RAS down mode.

The $\overline{RAS}$ signal goes high under the following conditions.

- When a refresh cycle is performed during RAS down mode
- When a self-refresh is performed
- When a transition to software standby mode is made
- When the external bus requested by the BREQ signal is released
- When either the RCDM or BE bit is cleared to 0

If a transition to the all-module clock-stop mode is made during RAS down mode, clocks are stopped with the $\overline{RAS}$ signal driven low. To make a transition with the $\overline{RAS}$ signal driven high, clear the RCDM bit to 0 before execution of the SLEEP instruction.

Clear the RCDM bit to 0 for write access to SCKCR to set the clock frequencies. For SCKCR, see section 27, Clock Pulse Generator.

(1) When DDS = 1 or EDDS = 1

A fast-page access is performed regardless of the bus master, only according to the address. The $\overline{\text{DACK}}$ and $\overline{\text{EDACK}}$ signals are asserted within the Tc1 cycle in both read and write accesses.

Figures 9.83 and 9.84 show the output timing example of the $\overline{\text{DACK}}$ and $\overline{\text{EDACK}}$ signals when DDS = 1 or EDDS = 1.

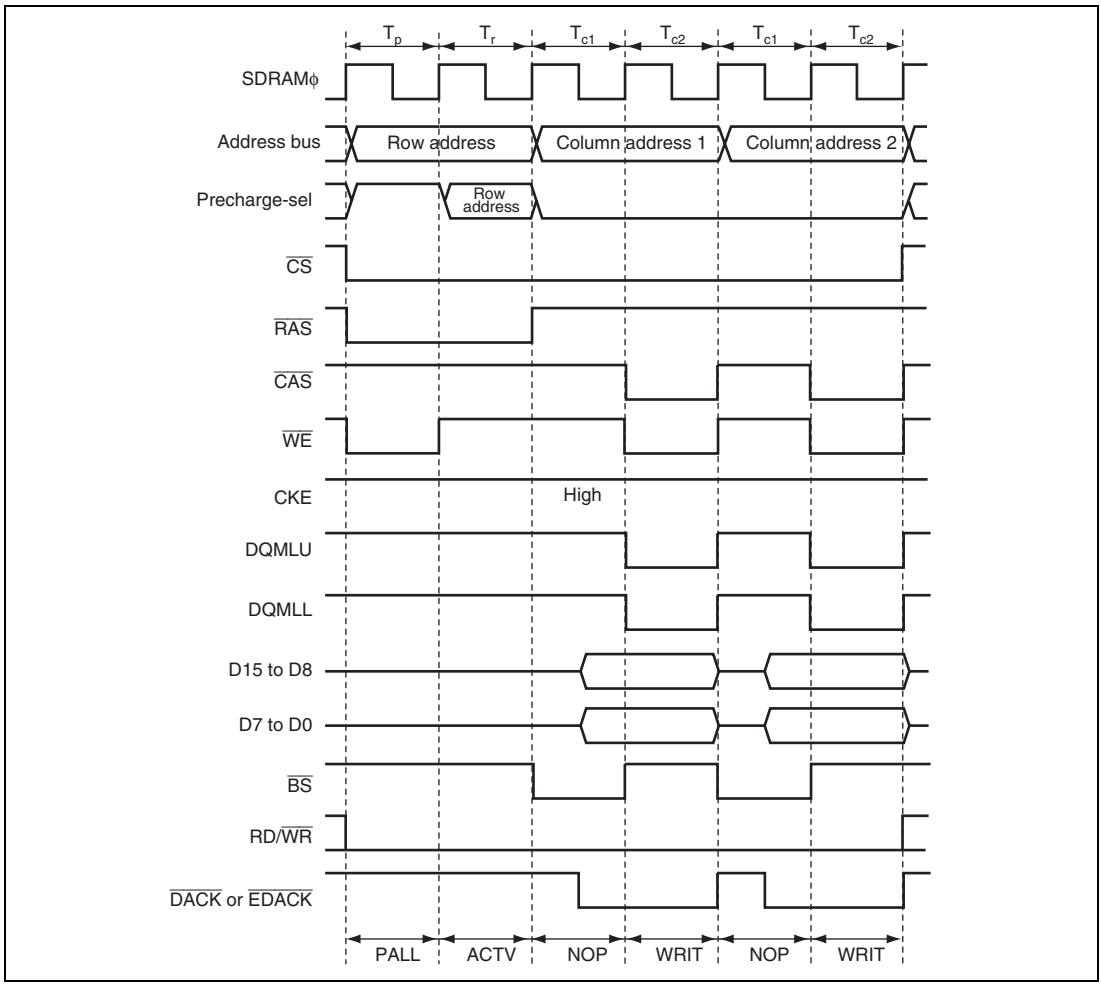


Figure 9.83 Output Timing Example of $\overline{\text{DACK}}$ and $\overline{\text{EDACK}}$ when DDS = 1 or EDDS = 1 (Write)

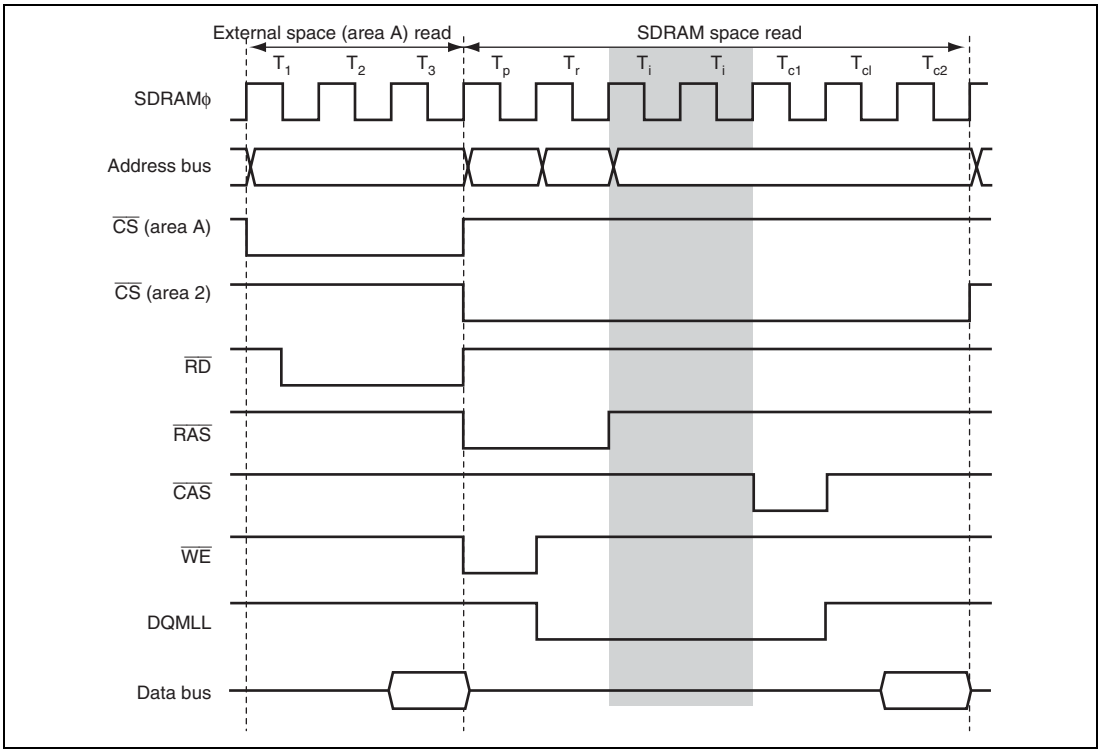


Figure 9.100 Example of SDRAM Full Access after External Read (CAS Latency = 2)

Channel 3:

- DMA source address register_3 (DSAR_3)
- DMA destination address register_3 (DDAR_3)
- DMA offset register_3 (DOFR_3)
- DMA transfer count register_3 (DTCR_3)
- DMA block size register_3 (DBSR_3)
- DMA mode control register_3 (DMDR_3)
- DMA address control register_3 (DACR_3)
- DMA module request select register_3 (DMRSR_3)

10.3.1 DMA Source Address Register (DSAR)

DSAR is a 32-bit readable/writable register that specifies the transfer source address. DSAR updates the transfer source address every time data is transferred. When DDAR is specified as the destination address (the DIRS bit in DACR is 1) in single address mode, DSAR is ignored.

Although DSAR can always be read from by the CPU, it must be read from in longwords and must not be written to while data for the channel is being transferred.

Bit	31	30	29	28	27	26	25	24
Bit Name								
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	23	22	21	20	19	18	17	16
Bit Name								
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8
Bit Name								
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Bit Name								
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	DTF1	0	R/W	Data Transfer Factor 1 and 0
6	DTF0	0	R/W	Select a DMAC activation source. When the on-chip peripheral module setting is selected, the interrupt source should be selected by DMRSR. When the external request setting is selected, the sampling method should be selected by the DREQS bit. 00: Auto request (cycle stealing) 01: Auto request (burst access) 10: On-chip module interrupt 11: External request
5	DTA	0	R/W	Data Transfer Acknowledge This bit is valid in DMA transfer by the on-chip module interrupt source. This bit enables or disables to clear the source flag selected by DMRSR. 0: To clear the source in DMA transfer is disabled. Since the on-chip module interrupt source is not cleared in DMA transfer, it should be cleared by the CPU or DTC transfer. 1: To clear the source in DMA transfer is enabled. Since the on-chip module interrupt source is cleared in DMA transfer, it does not require an interrupt by the CPU or DTC transfer.
4, 3	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.

(5) DTE Bit in DMDR

Although the DTE bit in DMDR enables or disables data transfer by the CPU write access, it is automatically cleared to 0 according to the DMA transfer state by the DMAC.

The conditions for clearing the DTE bit by the DMAC are as follows:

- When the total size of transfers is completed
- When a transfer is completed by a transfer size error interrupt
- When a transfer is completed by a repeat size end interrupt
- When a transfer is completed by an extended repeat area overflow interrupt
- When a transfer is stopped by an NMI interrupt
- When a transfer is stopped by and address error
- Reset state
- Hardware standby mode
- When a transfer is stopped by writing 0 to the DTE bit

Writing to the registers for the channels when the corresponding DTE bit is set to 1 is prohibited (except for the DTE bit). When changing the register settings after writing 0 to the DTE bit, confirm that the DTE bit has been cleared to 0.

Figure 10.21 show the procedure for changing the register settings for the channel being transferred.

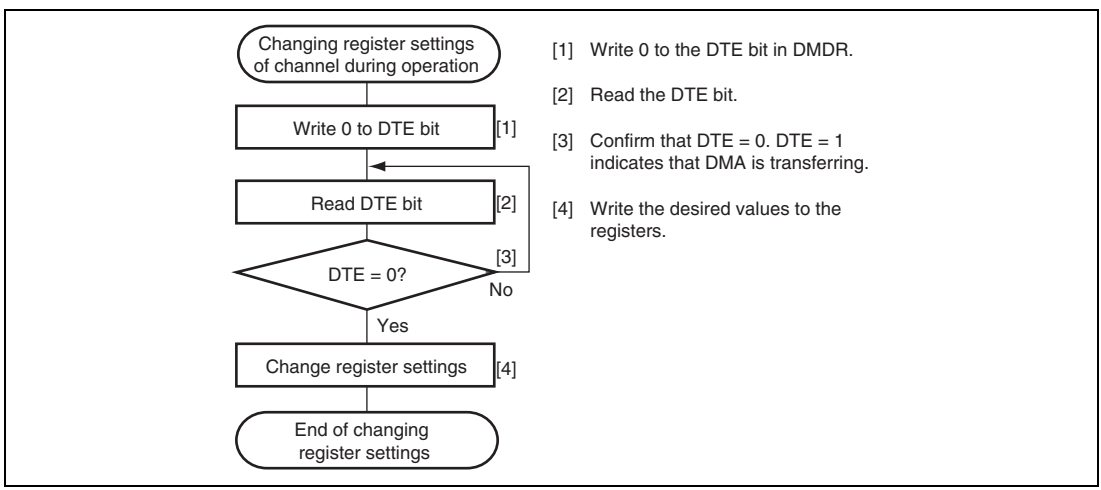


Figure 10.21 Procedure for Changing Register Setting For Channel being Transferred

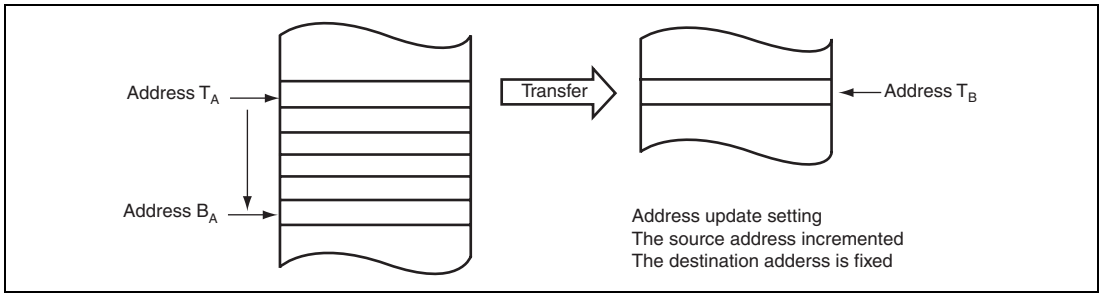


Figure 11.3 Dual Address Mode Operation

(2) Single Address Mode

In single address mode, the $\overline{\text{EDACK}}$ pin is used instead of EDSAR or EDDAR to transfer data directly between an external device and external memory. One transfer operation is executed in one bus cycle.

In this mode, the data bus width must be the same as the data access size. For details on the data bus width, see section 9, Bus Controller (BSC).

In this mode, the EXDMAC accesses the transfer source or transfer destination external device by outputting the strobe signal ($\overline{\text{EDACK}}$) for the external device with $\overline{\text{DACK}}$, and at the same time accesses the other external device in the transfer by outputting an address. In this way, EXDMA transfer can be executed in one bus cycle. In the example of transfer between external memory and an external device with $\overline{\text{DACK}}$ shown in figure 11.4, data is output to the data bus by the external device and written to external memory in the same bus cycle.

The transfer direction, that is whether the external device with $\overline{\text{DACK}}$ is the transfer source or transfer destination, can be specified with the DIRS bit in EDACR. Transfer is performed from the external memory (EDSAR) to the external device with $\overline{\text{DACK}}$ when DIRS = 0, and from the external device with $\overline{\text{DACK}}$ to the external memory (EDDAR) when DIRS = 1. The setting in the source or destination address register not used in the transfer is ignored.

The $\overline{\text{EDACK}}$ pin output is valid by the setting of EDACKE bit in EDMDR when single address mode is selected. The $\overline{\text{EDACK}}$ pin output is active-low.

$\overline{\text{ETEND}}$ pin output can be enabled or disabled by means of the ETENDE bit in EDMDR. $\overline{\text{ETEND}}$ is output for one bus cycle. When an idle cycle is inserted before the bus cycle, the $\overline{\text{ETEND}}$ signal is also output in the idle cycle.

Figure 11.5 shows an example of the timing in single address mode and figure 11.6 shows the single address mode operation.

12.9.9 Points for Caution when Overwriting DTCER

When overwriting of the DTC-transfer enable register (DTCER) and the generation of an interrupt that is a source for DTC activation are in competition, activation of the DTC and interrupt exception processing by the CPU will both proceed at the same time. Depending on the conditions at this time, doubling of interrupts may occur. If there is a possibility of competition between overwriting of the DTCER and generation of an interrupt that is a source for DTC activation, proceed with overwriting of the DTCER according to the relevant procedure given below.

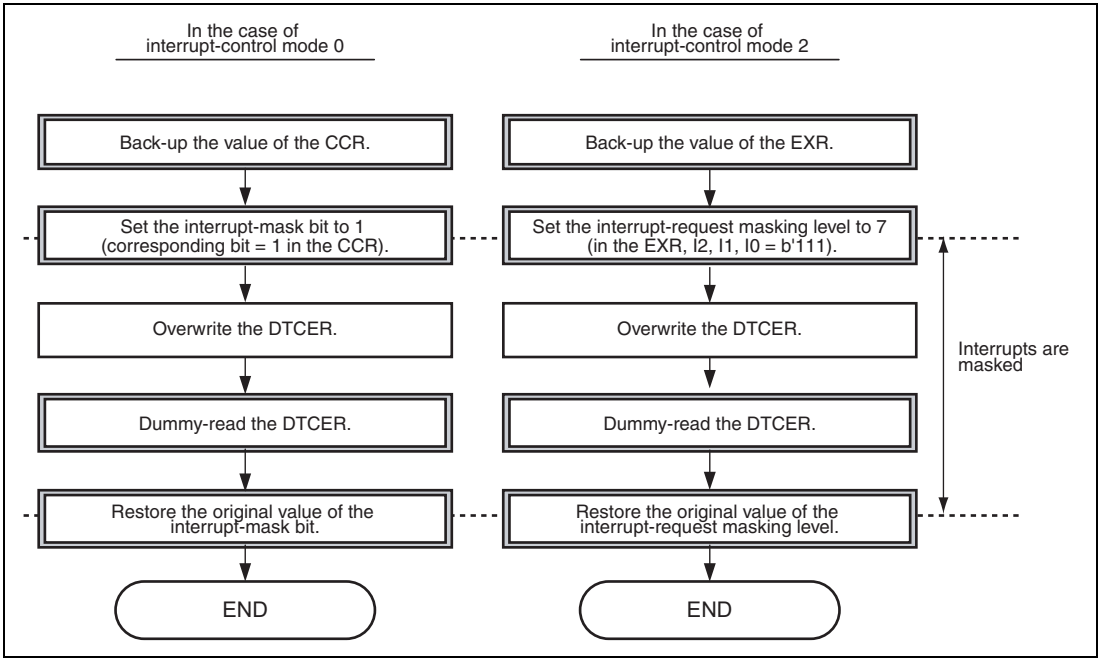


Figure 12.17 Example of Procedures for Overwriting the DTCER

Port		Output Specification Signal Name	Output Signal Name	Signal Selection Register Settings	Peripheral Module Settings
PJ	7	TIOCB8_OE	TIOCB8		TPU.TIOR_8.IOB3 = 0, TPU.TIOR_8.IOB[1,0] = 01/10/11
		PO 23_OE	PO23		NDERL_1.NDER23 = 1
	6	TIOCA8_OE	TIOCA8		TPU.TIOR_8.IOA3 = 0, TPU.TIOR_8.IOA[1,0] = 01/10/11
		PO 22_OE	PO22		NDERL_1.NDER22 = 1
	5	TIOCB7_OE	TIOCB7		TPU.TIOR_7.IOB3 = 0, TPU.TIOR_7.IOB[1,0] = 01/10/11
		PO 21_OE	PO21		NDERL_1.NDER21 = 1
	4	TIOCA7_OE	TIOCA7		TPU.TIOR_7.IOA3 = 0, TPU.TIOR_7.IOA[1,0] = 01/10/11
		PO 20_OE	PO20		NDERL_1.NDER20 = 1
	3	TIOCD6_OE	TIOCD6		TPU.TMDR_6.BFB = 0, TPU.TIORL_6.IOD3 = 0 TPU.TIORL_6.IOD[1,0] = 01/10/11
		PO 19_OE	PO19		NDERL_1.NDER19 = 1
	2	TIOCC6_OE	TIOCC6		TPU.TMDR_6.BFA = 0, TPU.TIORL_6.IOC3 = 0 TPU.TIORL_6.IOC[1,0] = 01/10/11
		PO 18_OE	PO18		NDERL_1.NDER18 = 1
	1	TIOCB6_OE	TIOCB6		TPU.TIORH_6.IOB3 = 0, TPU.TIORH_6.IOB[1,0] = 01/10/11
		PO 17_OE	PO17		NDERL_1.NDER17 = 1
	0	TIOCA6_OE	TIOCA6		TPU.TIORH_6.IOA3 = 0, TPU.TIORH_6.IOA[1,0] = 01/10/11
		PO 16_OE	PO16		NDERL_1.NDER16 = 1

Bit	Bit Name	Initial Value	R/W	Description
3	TPUMS2	0	R/W	TPU I/O Pin Multiplex Function Select Selects TIOCA2 function 0: Specifies P36 as output compare output and input capture 1: Specifies P37 as input capture input and P36 as output compare
2	TPUMS1	0	R/W	TPU I/O Pin Multiplex Function Select Selects TIOCA1 function 0: Specifies P34 as output compare output and input capture 1: Specifies P35 as input capture input and P34 as output compare
1	TPUMS0A	0	R/W	TPU I/O Pin Multiplex Function Select Selects TIOCA0 function 0: Specifies P30 as output compare output and input capture 1: Specifies P31 as input capture input and P30 as output compare
0	TPUMS0B	0	R/W	TPU I/O Pin Multiplex Function Select Selects TIOCC0 function 0: Specifies P32 as output compare output and input capture 1: Specifies P33 as input capture input and P32 as output compare

17.5 Usage Notes

17.5.1 Changing Values of Bits EXCKSN, CKS1, and CKS0

If bits EXCKSN, CKS1, and CKS0 in TCR32K are written to while the TM32K is operating, errors could occur in the incrementation. The TM32K must be stopped (the TME bit is set to 0) before the values of bits EXCKSN, CKS1, and CKS0 are changed.

Note that when the EXCKSN bit is 0, the CKS1 bit can be changed even though the TME bit is 1 (see section 17.3.3, EXCKSN=0 Operation).

17.5.2 Note on Register Initialization

TCR32K, TCNT32K1, TCNT32K2, and TCNT32K3 of the 32K timer are initialized in hardware standby mode or in the pin reset state. A reset from the watchdog timer or deep-software-standby reset does not initialize these registers.

17.5.3 Usage Notes on 32K Timer

- The 32K timer does not operate when the OSC32STP bit is set to 1. Always set the OSC32STP bit to 0 when starting the 32K timer.
- When the OSC32STP bit has been changed from 1 to 0, allow enough time to ensure settling of the oscillation by the subclock oscillator.
- Before stopping the TM32K, clear the TME bit to 0 for one clock (30 μs) or longer by the 32 subclock.
- When switching between subclock and main clock operation, wait for 500 μs or more (until the timer counter is updated next time) before reading the timer counter.

19.4.3 Clock

Either an internal clock generated by the on-chip baud rate generator or an external clock input to the SCK pin can be selected as the SCI's transfer clock, according to the setting of the C/$\overline{A}$ bit in SMR and the CKE1 and CKE0 bits in SCR. When an external clock is input to the SCK pin, the clock frequency should be 16 times the bit rate (when ABCS = 0) and 8 times the bit rate (when ABCS = 1).

In addition, when an external clock is specified, the average transfer rate or the base clock of TMR_4 to TMR_7 can be selected by the ACS3 to ACS0 bits in SEMR_5 and SEMR_6.

When the SCI is operated on an internal clock, the clock can be output from the SCK pin. The frequency of the clock output in this case is equal to the bit rate, and the phase is such that the rising edge of the clock is in the middle of the transmit data, as shown in figure 19.7.

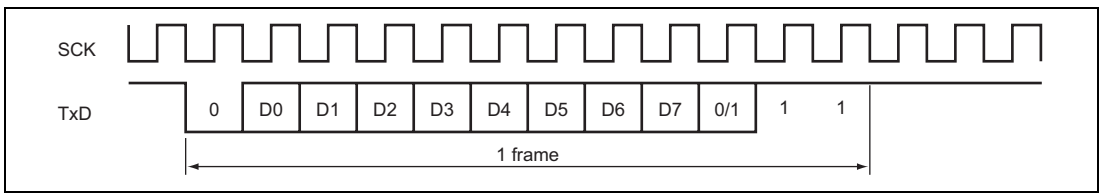


Figure 19.7 Phase Relation between Output Clock and Transmit Data (Asynchronous Mode)

20.3.11 EP0o Data Register (EPDR0o)

EPDR0o is an 8-byte receive FIFO buffer for endpoint 0. EPDR0o holds endpoint 0 receive data other than setup commands. When data is received successfully, EP0oTS in interrupt flag register 0 is set, and the number of receive bytes is indicated in the EP0o receive data size register. After the data has been read, setting EP0oRDFN in the trigger register enables the next packet to be received. This FIFO buffer can be initialized by means of BP0oCLR in the FCLR register.

Bit	7	6	5	4	3	2	1	0
Bit Name	D7	D6	D5	D4	D3	D2	D1	D0
Initial Value	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	D7 to D0	All 0	R	Data register for control-out transfer

20.3.12 EP0s Data Register (EPDR0s)

EPDR0s is an 8-byte FIFO buffer specifically for receiving endpoint 0 setup commands. Only the setup command to be processed by the application is received. When command data is received successfully, the SETUPTS bit in interrupt flag register 0 is set.

As a latest setup command must be received in high priority, if data is left in this buffer, it will be overwritten with new data. If reception of the next command is started while the current command is being read, command reception has priority, the read by the application is forcibly stopped, and the read data is invalid.

Bit	7	6	5	4	3	2	1	0
Bit Name	D7	D6	D5	D4	D3	D2	D1	D0
Initial Value	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	D7 to D0	All 0	R	Data register for storing the setup command at the control-out transfer

Bit	Bit Name	Initial Value	R/W	Description
1	EP2DMAE	0	R/W	Endpoint 2 DMA Transfer Enable When this bit is set, DMA transfer is enabled from memory to the endpoint 2 transmit FIFO buffer. If there is at least one byte of open space in the FIFO buffer, a DMAC start interrupt signal (USBINTN1) is asserted. In DMA transfer, when 64 bytes are written to the FIFO buffer the EP2 packet enable bit is set automatically, allowing 64 bytes of data to be transferred, and if there is still space in the other side of the two FIFOs, the DMAC start interrupt signal (USBINTN1) is asserted again. However, if the size of the data packet to be transmitted is less than 64 bytes, the EP2 packet enable bit is not set automatically, and so should be set by the CPU with a DMA transfer end interrupt. As EP2-related interrupt requests to the CPU are not automatically masked, interrupt requests should be masked as necessary in the interrupt enable register. • Operating procedure 1. Write of 1 to the EP2 DMAE bit in DMAR 2. Set the DMAC to activate through USBINTN1 3. Transfer count setting in the DMAC 4. DMAC activation 5. DMA transfer 6. DMA transfer end interrupt generated See section 20.8.3, DMA Transfer for Endpoint 2.

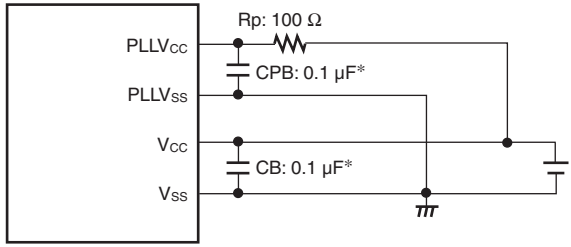
20.3.26 Transceiver Test Register 0 (TRNTREG0)

TRNTREG0 controls the on-chip transceiver output signals. Setting the PTSTE bit to 1 specifies the transceiver output signals (USD+ and USD-) arbitrarily. Table 20.4 shows the relationship between TRNTREG0 setting and pin output.

Bit	7	6	5	4	3	2	1	0
Bit Name	PTSTE	—	—	—	SUSPEND	txenl	txse0	txdata
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R	R	R	R/W	R/W	R/W	R/W

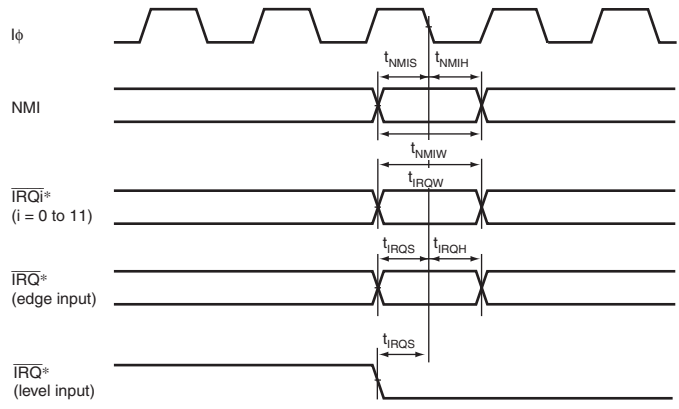
Bit	Bit Name	Initial Value	R/W	Description
7	PTSTE	0	R/W	Pin Test Enable Enables the test control for the on-chip transceiver output pins (USD+ and USD-).
6 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	SUSPEND	0	R/W	On-Chip Transceiver Output Signal Setting
2	txenl	0	R/W	SUSPEND: Sets the (SUSPEND) signal of the on-chip transceiver.
1	txse0	0	R/W	
0	txdata	0	R/W	txenl: Sets the output enable (txenl) signal of the on-chip transceiver. txse0: Sets the Signal-ended 0 (txse0) signal of the on-chip transceiver. txdata: Sets the (txdata) signal of the on-chip transceiver.

Figure 27.11 shows the external circuitry recommended for the PLL circuit. Separate PLLVcc and PLLVss from the other Vcc and Vss lines at the board power supply source, and be sure to insert bypass capacitors CPB and CB close to the pins.



Note: * CB and CPB are laminated ceramic capacitors.

Figure 27.11 Recommended External Circuitry for PLL Circuit



Note: * SSIER must be set to cancel software standby mode.

Figure 30.7 Interrupt Input Timing

30.4.3 Bus Timing

Table 30.8 Bus Timing (1)

Conditions: V_{CC} = $PLLV_{CC}$ = DrV_{CC} = 3.0 V to 3.6 V*, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = DrV_{SS} = AV_{SS} = 0 V, Bϕ = 8 MHz to 50 MHz,
T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	15	ns	Figures 30.8 to 30.36
Address setup time 1	t_{AS1}	$0.5 \times t_{cyc} - 8$	—	ns	
Address setup time 2	t_{AS2}	$1.0 \times t_{cyc} - 8$	—	ns	
Address setup time 3	t_{AS3}	$1.5 \times t_{cyc} - 8$	—	ns	
Address setup time 4	t_{AS4}	$2.0 \times t_{cyc} - 8$	—	ns	
Address hold time 1	t_{AH1}	$0.5 \times t_{cyc} - 8$	—	ns	
Address hold time 2	t_{AH2}	$1.0 \times t_{cyc} - 8$	—	ns	
Address hold time 3	t_{AH3}	$1.5 \times t_{cyc} - 8$	—	ns	